PostLayout Corners

	ADC delay							
Corner	**0**	**1**	**2**	**3**	**4**	**5**	**6**	**7**
Nominal	5.78	5.75	5.75	5.73	5.73	5.79	5.84	5.87
Best Case	5.82	5.85	5.85	5.85	5.87	5.87	5.87	5.87
Best Case Ext_0	5.96	5.93	5.95	5.92	5.95	5.95	5.94	5.93
Best Case Ext_1	5.89	5.89	5.88	5.90	5.90	5.90	5.93	5.93
Low Temp	5.84	5.82	5.79	5.82	5.82	5.74	5.81	5.80
Low Temp Ext_0	5.99	5.97	5.97	5.97	5.92	5.92	5.94	5.93
Low Temp Ext_1	5.81	5.91	5.86	5.91	5.89	5.92	5.92	5.92
Max Leakage	5.95	5.95	5.95	5.97	5.92	5.94	5.97	5.95
Typical	5.74	5.76	5.76	5.74	5.72	5.79	5.82	5.87
UT_0	5.80	5.78	5.75	5.83	5.85	5.84	5.83	5.76
UT_1	5.84	5.82	5.86	5.86	5.86	5.91	5.87	5.91
UT_2	5.64	5.57	5.82	5.68	5.38	-1.55	-3.13	-1.37
Worst Case	5.70	5.72	5.54	5.31	-3.05	-1.55	-2.45	4.83
Worst Case Ext_0	5.75	5.81	5.79	5.71	5.78	5.63	5.67	5.38
Worst Case Ext_1	5.66	5.71	5.86	5.82	5.74	5.81	5.60	5.70
			Default for SALT v3					

Schematic Corners

	ADC delay							
Corner	**0**	**1**	**2**	**3**	**4**	**5**	**6**	**7**
Nominal	5.96	5.97	5.98	5.93	5.96	5.95	5.96	5.95
Best Case	5.86	5.87	5.85	5.85	5.89	5.90	5.87	5.88
Best Case Ext_0	5.80	5.80	5.80	5.80	5.81	5.80	5.80	5.81
Best Case Ext_1	5.87	5.89	5.88	5.87	5.89	5.88	5.88	5.88
Low Temp	5.91	5.90	5.89	5.90	5.88	5.91	5.90	5.88
Low Temp Ext_0	5.91	5.89	5.89	5.91	5.89	5.89	5.89	5.91
Low Temp Ext_1	5.83	5.86	5.88	5.87	5.88	5.86	5.88	5.88
Max Leakage	5.82	5.82	5.82	5.82	5.82	5.82	5.83	5.82
Typical	5.98	5.97	5.96	5.96	5.97	5.99	5.95	5.95
UT_0	5.96	5.97	5.98	5.98	5.97	5.98	5.98	5.97
UT_1	6.01	6.01	6.02	5.92	5.95	5.98	6.01	6.03
UT_2	5.88	5.87	5.84	5.88	5.83	5.85	5.83	5.84
Worst Case	5.86	5.88	5.89	5.88	5.97	5.92	5.88	6.00
Worst Case Ext_0	5.90	5.90	5.90	5.91	5.90	5.89	5.89	5.89
Worst Case Ext_1	5.83	5.83	5.85	5.81	5.83	5.82	5.79	5.81