SALT ver 4.5 measurement loogbook

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Contents

Contents **1**

1 Measurements setup **7**
1.1 SALT registers configuration 7
1.2 DLL dll_vcdl_cfg register optimal value for different ASICs 8
1.3 Input capacitance assembly 8

2 Board 0 with ASIC 0 **10**
2.1 Before input pads bonded 10
2.2 Cap-PCB bonded, 12 pF capacitors assembled 11
2.3 Cap-PCB bonded, capacitors removed 12
2.4 Cap-PCB bonded, 12 pF capacitors re-assembled 13
2.4.1 Channel -1, krum_cfg='h00 15
2.5 Input bonds completely removed 16

3 Board 1 with ASIC 1 **17**
3.1 Before input pads bonded 17
3.2 Dummy bond on input pads 18
3.3 Cap-PCB bonded, no capacitors assembled 19
3.3.1 Default ASIC configuration 19
3.3.2 Optimized test pulse and ADC delay 20
3.4 Cap-PCB bonded, 2.2 pF capacitors assembled 22
3.4.1 Default ASIC configuration 22
3.4.2 Optimized test pulse and ADC delay 23
3.5 Cap-PCB bonded, 12 pF capacitors assembled 25
3.5.1 Default ASIC configuration 25
3.5.2 Optimized test pulse and ADC delay 26

3.6 Cap-PCB bonded, 12 pF capacitors + 620 kΩ resistors assembled 28
3.6.1 Default ASIC configuration 28
3.6.2 Optimized test pulse and ADC delay 28
3.7 Cap-PCB bonded, 12 pF capacitors + 620 kΩ resistors assembled; Ibuf current maximized 30
3.7.1 Default ASIC configuration 30
3.7.2 Optimized test pulse and ADC delay 30
3.8 Cap-PCB bonded, 12 pF capacitors + 820 kΩ resistors assembled; Ibuf current maximized 31
3.8.1 Default ASIC configuration 31
3.8.2 Optimized test pulse and ADC delay 32
3.9 Cap-PCB bonded, 12 pF capacitors + 820 kΩ resistors assembled; Ibuf current maximized; Preamp GND configuration – input + backside . . . 34
3.9.1 Default ASIC configuration 34
3.9.2 Optimized test pulse and ADC delay 35
3.10 DLL and PLL stability monitoring 37

4 Board 0 with ASIC 2 **41**
4.1 Input bonds completely removed from channel -1 41
4.1.1 Default ASIC configuration 41
4.1.2 Optimized test pulse and ADC delay 41
4.2 Cap-PCB bonded, 12 pF capacitors assembled; Ibuf current maximized . 43
4.2.1 Default ASIC configuration 43
4.2.2 Optimized test pulse and ADC delay 43
4.3 Cap-PCB bonded, 12 pF capacitors + 820 kΩ resistors assembled; Ibuf current maximized 45
4.3.1 Default ASIC configuration 45
4.3.2 Optimized test pulse and ADC delay 45
4.4 Cap-PCB bonded, 12 pF capacitors + 820 kΩ resistors assembled; Ibuf current maximized; ADC power supply with 2.2 Ω series resistor 47
4.4.1 Default ASIC configuration 47
4.4.2 Optimized test pulse and ADC delay 47
4.5 Cap-PCB bonded, 12 pF capacitors + 820 kΩ resistors assembled; Ibuf current maximized; ADC power supply with 1 μH series inductor 49
4.5.1 Default ASIC configuration 49
4.5.2 Optimized test pulse and ADC delay 49
4.6 Cap-PCB bonded, no capacitors assembled; Ibuf current maximized; ADC power supply with 1 μH series inductor 51
4.6.1 Default ASIC configuration 51
4.6.2 Optimized test pulse and ADC delay 51
4.7 Cap-PCB bonded, no capacitors assembled; Ibuf current maximized; ADC power supply with 1 μH series inductor; floating copper foil on ASIC . . 53
4.7.1 Default ASIC configuration 53
4.7.2 Optimized test pulse and ADC delay 53

4.8 Cap-PCB bonded, 12 pF capacitors assembled; Ibuf current maximized; ADC power supply with 1 μH series inductor; floating copper foil on ASIC 55
4.8.1 Default ASIC configuration 55
4.8.2 Optimized test pulse and ADC delay 55
4.9 Cap-PCB bonded, 12 pF capacitors assembled; Ibuf current maximized; ADC power supply with 1 μH series inductor; floating copper foil on ASIC; Preamp GND configuration – input + backside 57
4.9.1 Default ASIC configuration 57
4.9.2 Optimized test pulse and ADC delay 57
4.10 Cap-PCB bonded, 12 pF capacitors assembled; Ibuf current maximized; ADC power supply with 1 μH series inductor; grounded copper foil on ASIC; Preamp GND configuration – input + backside 59
4.10.1 Default ASIC configuration 59
4.10.2 Optimized test pulse and ADC delay 59
4.11 Cap-PCB bonded, 12 pF capacitors assembled; Ibuf current maximized; ALL power supply with 1 μH series inductor; grounded copper foil on ASIC; Preamp GND configuration – input + backside 61
4.11.1 Default ASIC configuration 61
4.11.2 Optimized test pulse and ADC delay 61
4.11.3 ASIC response for EMI source 62
4.12 Cap-PCB bonded, 12 pF capacitors assembled; Ibuf current maximized; ALL power supply with 1 μH series inductor; grounded copper foil on ASIC; Preamp GND configuration – only backside 64
4.12.1 ASIC response for EMI source 64
4.13 S2D response for different sampling frequencies 65
4.13.1 Response at 1 MHz at full activity with 12 pF + 820 kΩ at input 65
4.13.2 Response at 1 MHz at full activity with 0 pF; floating copper foil on ASIC 67
4.13.3 Response at 1 MHz at full activity with 12 pF; grounded copper foil on ASIC; Preamp GND configuration – input + backside. . . 70

5 Board 1 with ASIC 4 72
5.1 S2D response for different sampling frequencies 72
5.1.1 Response at 1 MHz at full activity without input pads bonded . . 72
5.1.2 Response at 1 MHz at full activity with 12 pF at input 75
5.1.3 Response at 1 MHz at full activity with 12 pF at input; preamp GND configuration – input + backside 78
5.1.4 Response vs main clock frequency without input pads bonded . . 81
5.1.5 Response at 1 MHz vs activity without input pads bonded 81
5.2 Before input pads bonded 82
5.2.1 Default ASIC configuration 82
5.2.2 Optimized test pulse and ADC delay 83
5.3 Cap-PCB bonded, 12 pF capacitors assembled; Ibuf current maximized . 84
5.3.1 Default ASIC configuration 84

5.3.2 Optimized test pulse and ADC delay 85
5.4 Cap-PCB bonded, 12 pF capacitors assembled; Ibuf current maximized; Fsmp=33 MHz 87
5.4.1 Default ASIC configuration 87
5.4.2 Optimized test pulse and ADC delay 87
5.5 Cap-PCB bonded, 12 pF capacitors assembled; Ibuf current maximized; Preamp GND configuration – input + backside 89
5.5.1 Default ASIC configuration 89
5.5.2 Optimized test pulse and ADC delay 90
5.6 Cap-PCB bonded, 12 pF capacitors assembled; Ibuf current maximized; Preamp GND configuration – only input 92
5.6.1 Default ASIC configuration 92
5.6.2 Optimized test pulse and ADC delay 93
5.7 Cap-PCB bonded, 12 pF capacitors assembled; Ibuf current maximized; floating copper foil on ASIC; Preamp GND configuration – only input . . 95
5.7.1 Default ASIC configuration 95
5.7.2 Optimized test pulse and ADC delay 96
5.8 Cap-PCB bonded, 12 pF capacitors assembled; Ibuf current maximized; floating copper foil on ASIC; Preamp GND configuration – input + backside 98
5.8.1 Default ASIC configuration 98
5.8.2 Optimized test pulse and ADC delay 99
5.9 Cap-PCB bonded, 12 pF capacitors assembled; Ibuf current maximized; floating copper foil on ASIC; Preamp GND configuration – only backside 101
5.9.1 Default ASIC configuration 101
5.9.2 Optimized test pulse and ADC delay 101
5.10 Cap-PCB bonded, 12 pF capacitors assembled; Ibuf current maximized; floating copper foil on ASIC; All inputs grounded; Preamp GND configuration – only backside 103
5.10.1 Default ASIC configuration 103
5.10.2 Optimized test pulse and ADC delay 104
5.11 Cap-PCB bonded, 12 pF capacitors assembled; Ibuf current maximized; floating small horizontal copper foil on ASIC; All inputs grounded; Preamp GND configuration – only backside 106
5.11.1 Default ASIC configuration 106
5.11.2 Optimized test pulse and ADC delay 107
5.12 Cap-PCB bonded, 12 pF capacitors assembled; Ibuf current maximized; floating small horizontal copper foil on ASIC; Preamp GND configuration – only backside 109
5.12.1 Default ASIC configuration 109
5.12.2 Optimized test pulse and ADC delay 110
5.13 Cap-PCB bonded, 12 pF capacitors assembled; Ibuf current maximized; Results comparison 112

6 Board 1 with ASIC 5 **114**
6.1 Cap-PCB bonded, 12 pF capacitors assembled; Ibuf current maximized . 114
6.1.1 Default ASIC configuration 114
6.1.2 Optimized test pulse and ADC delay 115
6.1.3 ASIC response for EMI source 117
6.2 Cap-PCB bonded, 12 pF capacitors assembled; Ibuf current maximized; Preamp GND configuration – input + backside 122
6.2.1 ASIC response for EMI source 122
6.3 Cap-PCB bonded, 12 pF capacitors assembled; Ibuf current maximized; Preamp GND configuration – only input 124
6.3.1 ASIC response for EMI source 124

7 ASICs history **126**

8 Various issues **128**
8.1 Bonding issue at AGH-UST 128
8.2 Copper foil on ASIC B0A2 and 1 μH inductor assembly 131
8.3 Copper foil on ASIC B1A4 132
8.4 EMI source over ASIC B0A2 135

List of Figures **136**

Documentation Conventions

To aid the readers understanding, a consistent formatting style has been used throughout this manual.

- Internal signals are written using *italic* font.
- External connections names (pads) like supplies use CAPITAL LETTERS only.
- External signals names, however, are in capital letters but using *ITALIC* font also.
- Configuration elements like register names are written in sans serif font.
- Signals controlled by configuration bits use *slanted sans serif* font.

For numbers the Verilog prefix style is used:

- **'b** for binary numbers e.g 'b1010,
- **'h** for hexadecimal numbers e.g 'hA7,
- **'d** for decimal numbers e.g 'd72,
- no prefix means that the number is in decimal notation.

Some C style prefixes **0x** for hexadecimal numbers may also appear in this document.

1 Measurements setup

1.1 SALT registers configuration

Table 1: Base configuration (from JC); DLL VCDL setting is different in each chip

Addr	Value	Comment
'h004	'h8C	PLL on
'h006	'h12	PLL VCO='h12
'h004	'hCC	PLL connected
'h000	'h22	pattern register to output
'h001	'hF0	pattern value='hF0
'h008	'h00	ser_byte_start=0
'h300	'h0C	DLL not connected and started, HLP inactive; test and monitors off
'h301	??	DLL VCDL=?? (see table 4)
'h300	'h4C	DLL not connected, started, HLP inactive; test and monitors off
'h300	'h6C	DLL connected, started, HLP inactive; test and monitors off
'h002	'h1F	deser_cfg: deser_byte_start=7; data_clk_sel[1:0]=2'b11
'h003	'h3B	pll_clk_cfg: sel[1]=3; sel[0]='hB
'h507	'h01	idle group size=1

Table 2: Test pulse configuration (from JC)

Addr	Value	Comment
'h300	'hE4	DLL active, test channels on
'h305	'h9F	Calib inverted, pulse_len 'h1F='d31 (max)
'h306	'h3F	Calib volt='h3F
'h007	'h07	tfc_fifo_len='h07
'h303	'h63	adc_clk_sel='h23
'h104	'h80	adc_sync_sel=1 (DSP input synchronization)
'h203	'h0C	shaper_dac='h0C
'h201	'h0F	preamp_dac='h0F
'h31B	'h15	vcm_cur='h15

Table 3: Calibration and ADC delay optimizations

Addr	Value	Comment
'h305	'hE4	Calib not inverted, pulse_len 'h1F='d31 (max)
'h306	'h9F	Calib volt='h00
'h200	'h07	ADC delay='d7

1.2 DLL dll_vcdl_cfg register optimal value for different ASICs

Optimum value of dll_vcdl_cfg was obtained from DLL configuration procedure described in the SALT documentation. The procedure have to be repeated for each particular ASIC.

Table 4: Optimal dll_vcdl_cfg register value

ASIC version	dll_vcdl_cfg
ASIC 0	–
ASIC 1	'h31
ASIC 2	'h2F
ASIC 3	–
ASIC 4	'h28
ASIC 5	'h2B

For ASIC 0 a suboptimal value 'h23 was used, which caused some DLL instabilities.

1.3 Input capacitance assembly

Input capacitance assembly is shown on Figure 1 – small PCB (hereinafter referred as cap-PCB) glued in front of SALT ASIC. The cap-PCB contains two signal bondpads (top right and bottom right), the center bondpad, common for both capacitors, bonded directly to the ASIC ground pad on main PCB, and two capacitors soldered (on the left). The signal bondpads of cap-PCB are boned to the inputs 0 and 127 on SALT ASIC (connected to the test channels 0 and 1, referred hereinafter as channels -1 and 128).

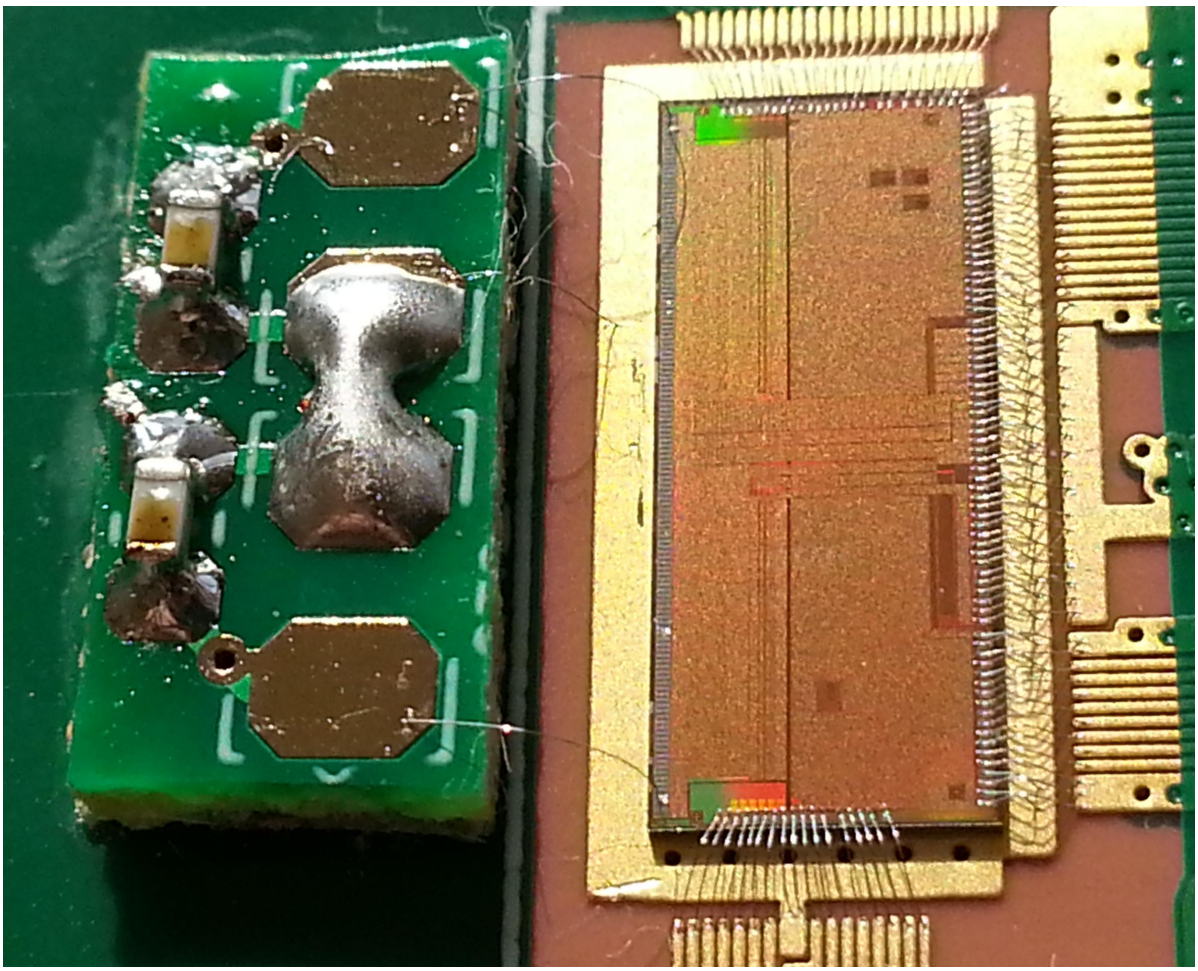

Figure 1: Input capacitance assembly

2 Board 0 with ASIC 0

No quantitative measurements done, only some result which may be partial or incomplete.

2.1 Before input pads bonded

ASIC configuration: default values after reset.
No results for channel 128 before bonding.

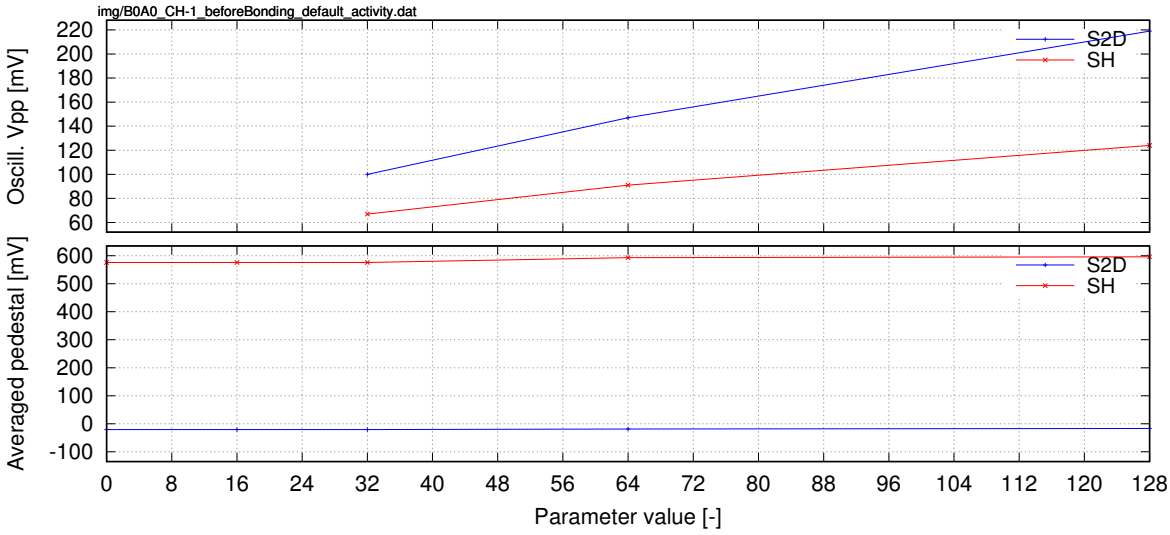

Figure 2: B0A0, channel -1, before bonding. Parameter=no. of active ADCs

2.2 Cap-PCB bonded, 12 pF capacitors assembled

ASIC configuration: default values after reset.
Cap-PCB assembled, bonded to SALT input pads 0 and 127, two 12 pF capacitors soldered to the cap-PCB.

Short on cap-PCB found, this result is irrelevant.

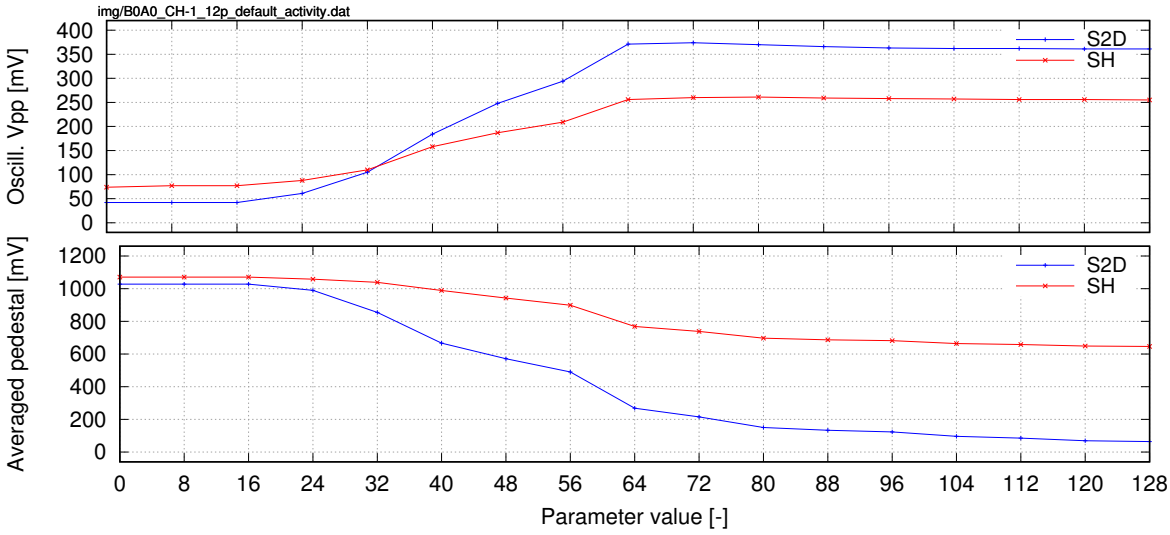

Figure 3: B0A0, channel -1, cap-PCB bonded, 12 pF capacitors assembled. Parameter=no. of active ADCs

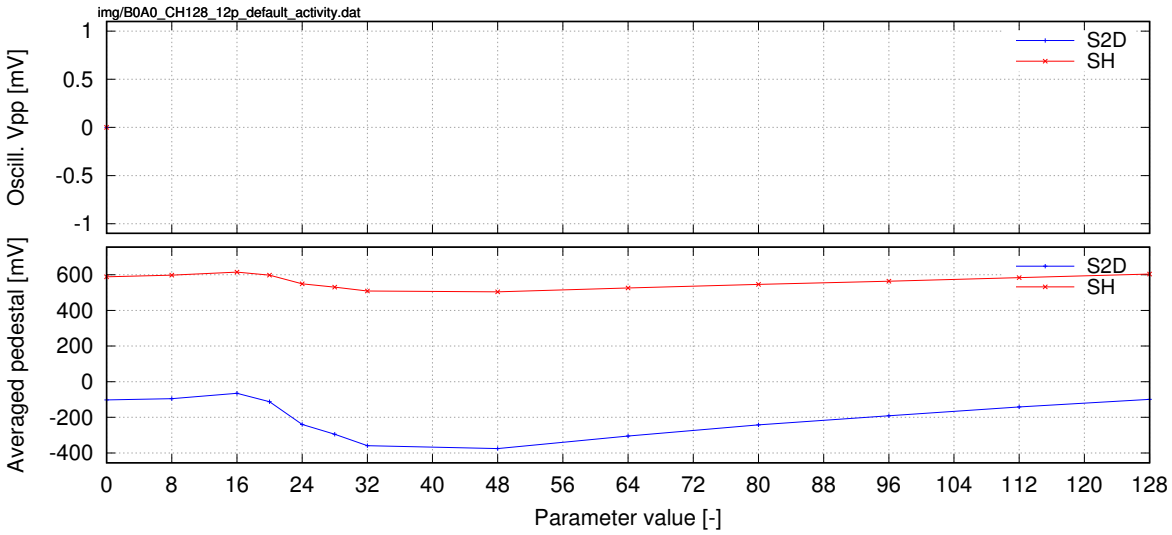

Figure 4: B0A0, channel 128, cap-PCB bonded, 12 pF capacitors assembled, **no data for oscillations**. Parameter=no. of active ADCs

2.3 Cap-PCB bonded, capacitors removed

ASIC configuration: default values after reset.
Cap-PCB assembled, bonded to SALT input pads 0 and 127. Capacitors removed from cap-PCB.

Short on cap-PCB found, this result is irrelevant.

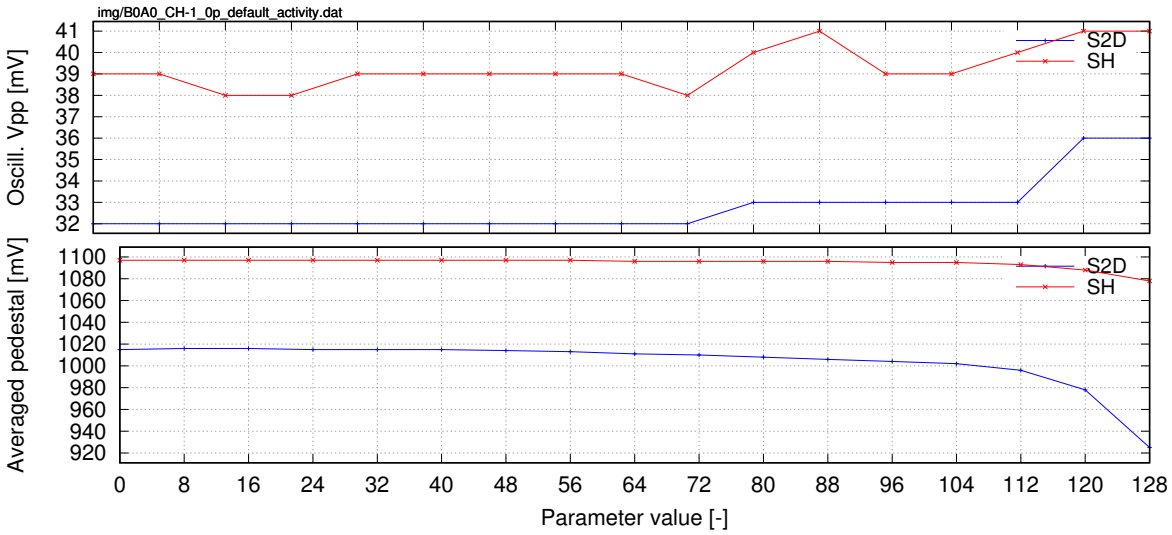

Figure 5: B0A0, channel -1, cap-PCB bonded, capacitors removed. Parameter=no. of active ADCs

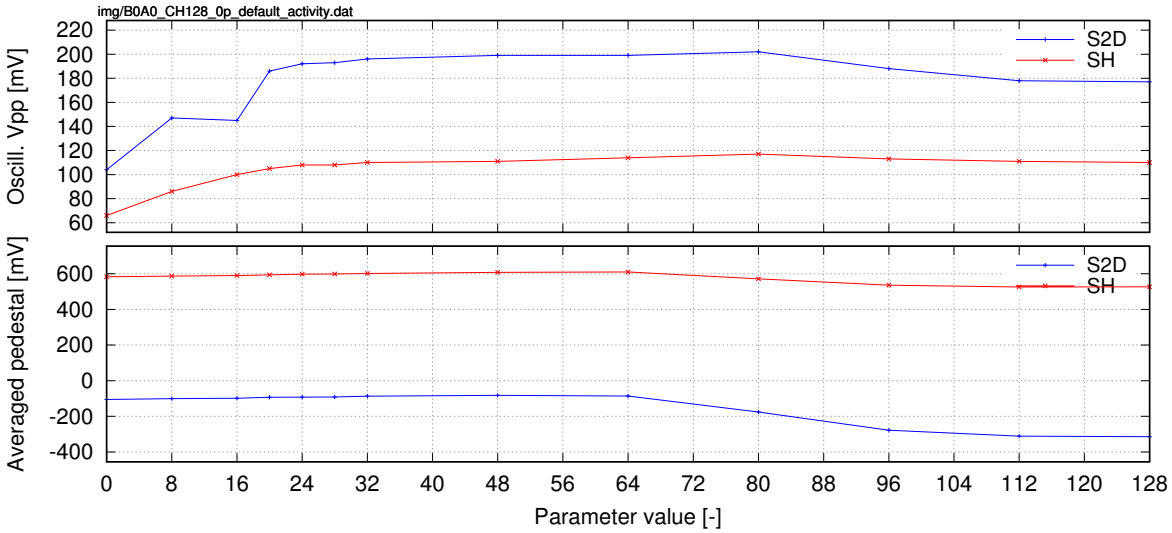

Figure 6: B0A0, channel 128, cap-PCB bonded, capacitors removed. Parameter=no. of active ADCs

2.4 Cap-PCB bonded, 12 pF capacitors re-assembled

ASIC configuration: default values after reset.
Cap-PCB assembled, bonded to SALT input pads 0 and 127, two 12 pF capacitors re-assembled to the cap-PCB.

Short on cap-PCB found, this result is irrelevant.

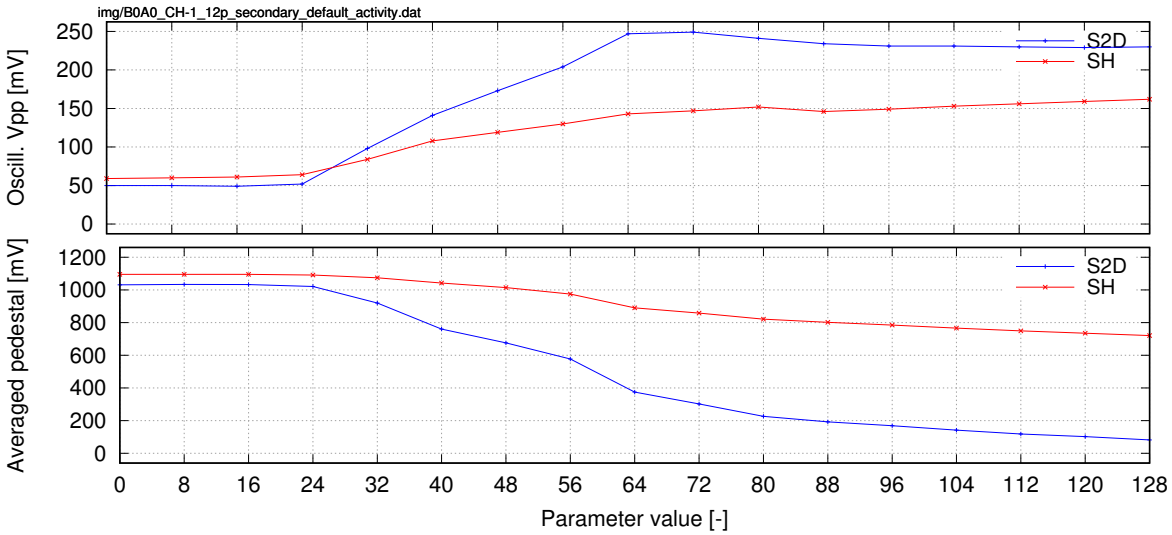

Figure 7: B0A0, channel -1, cap-PCB bonded, 12 pF capacitors re-assembled. Parameter=no. of active ADCs

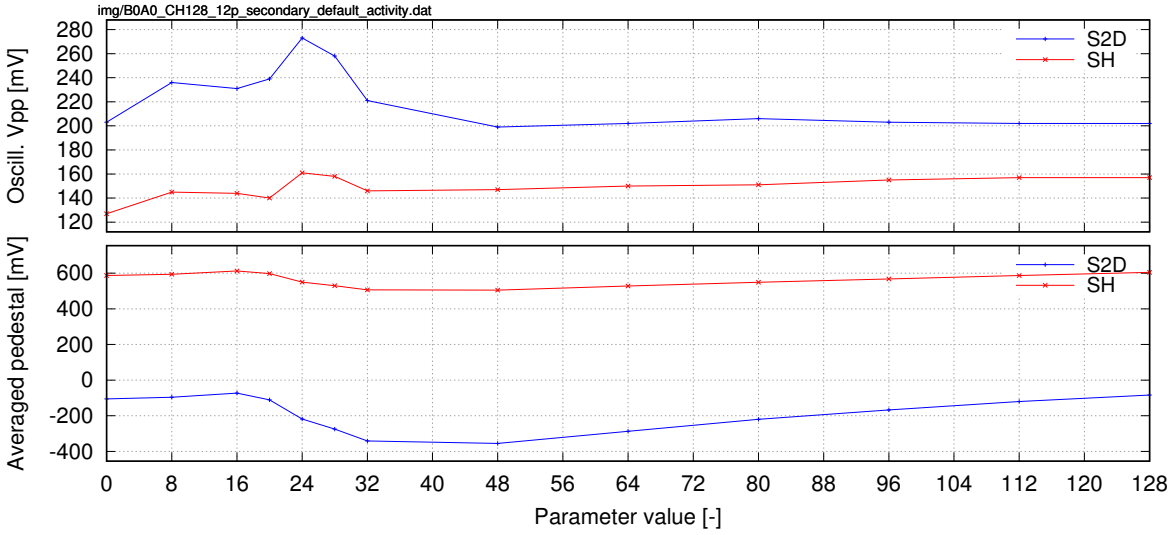

Figure 8: B0A0, channel 128, cap-PCB bonded, 12 pF capacitors re-assembled. Parameter=no. of active ADCs

2.4.1 Channel -1, krum_cfg='h00

ASIC configuration: default values after reset + Krummenacher DAC set to zero (see table 5). Only channel -1 measured.

Table 5: Krummenacher current set to zero

Addr	Value	Comment
'h202	'h80	Low gain=1, krum_cfg=0

Short on cap-PCB found, this result is irrelevant.

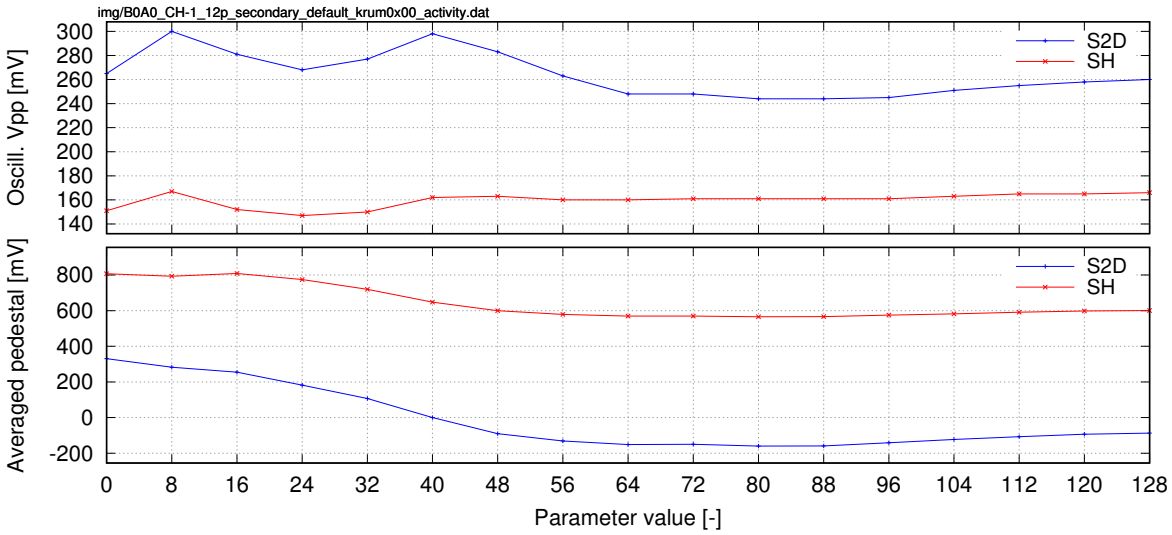

Figure 9: B0A0, channel -1, cap-PCB bonded, 12 pF capacitors re-assembled, krum_cfg='h00. Parameter=no. of active ADCs

2.5 Input bonds completely removed

ASIC configuration: default values after reset.
Cap-PCB assembled, bonds between cap-PCB and SALT inputs removed.

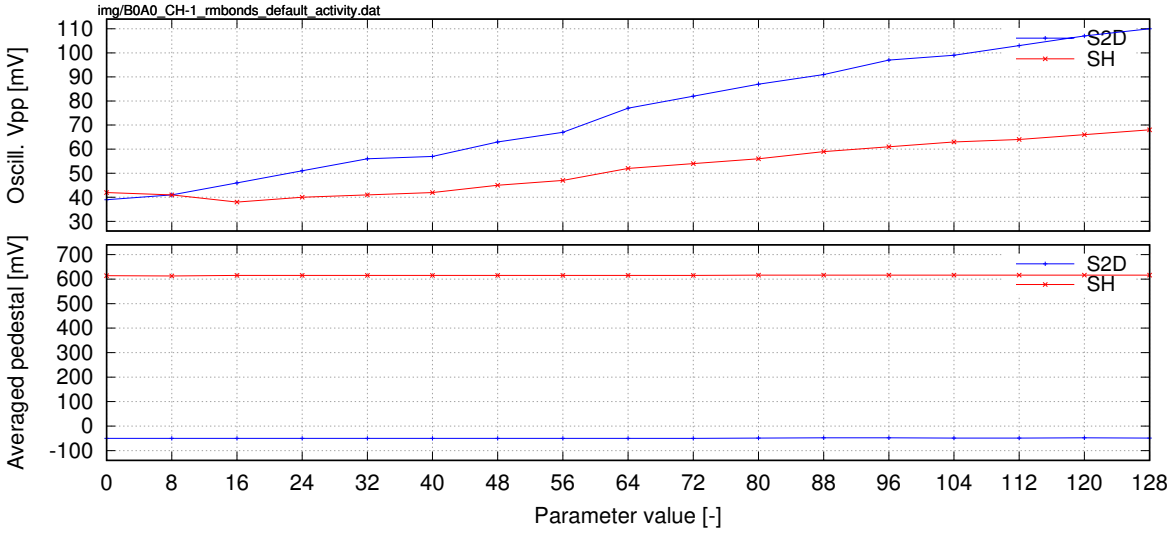

Figure 10: B0A0, channel -1, input bonds completely removed. Parameter=no. of active ADCs

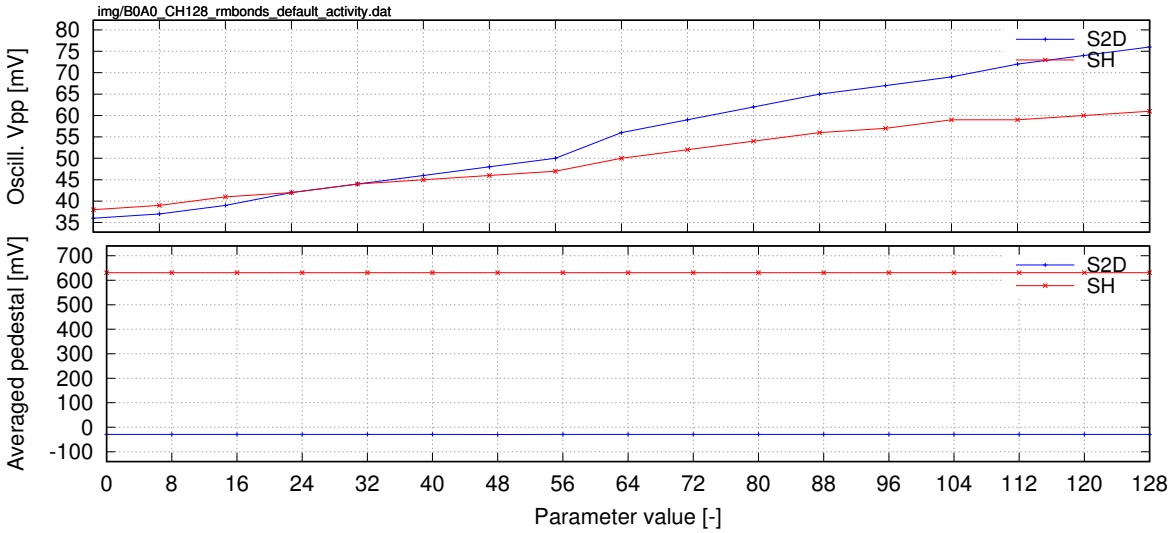

Figure 11: B0A0, channel 128, input bonds completely removed. Parameter=no. of active ADCs

3 Board 1 with ASIC 1

3.1 Before input pads bonded

ASIC configuration: JC configuration (tables 1 & 2).

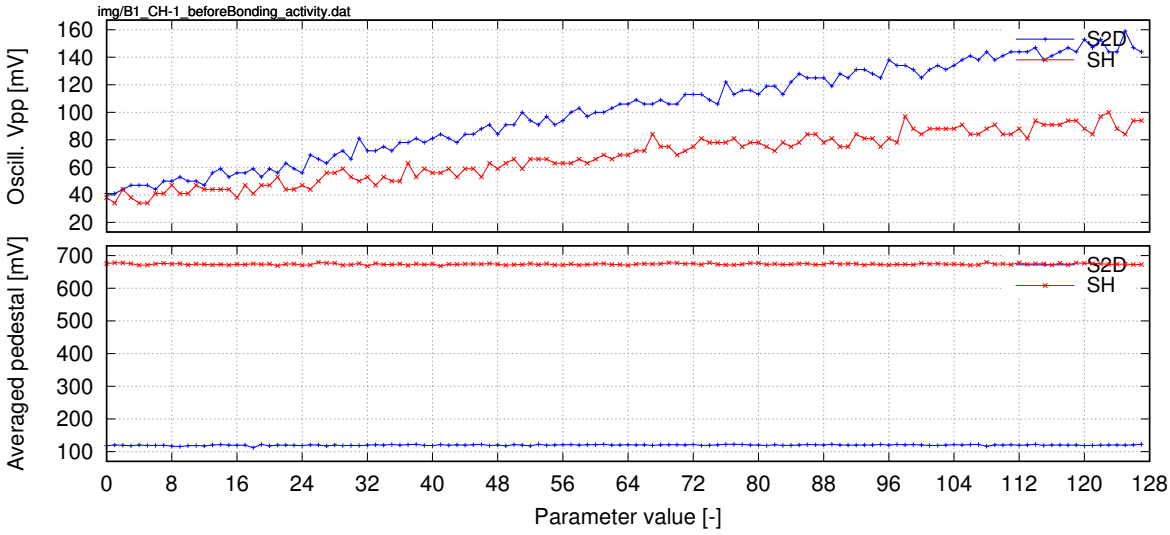

Figure 12: B1A1, channel -1, before bonding. Parameter=no. of active ADCs

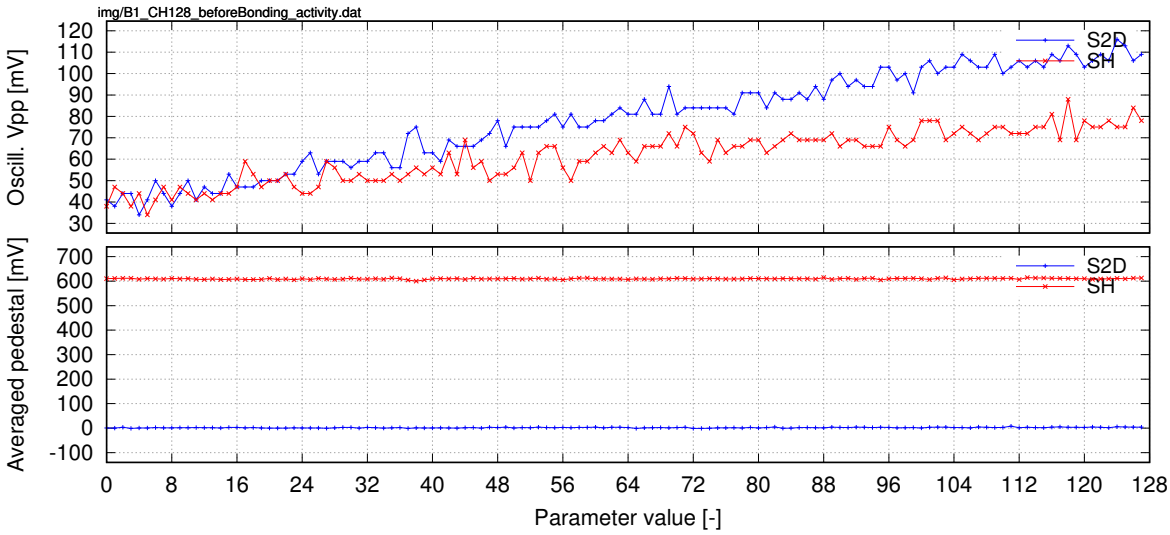

Figure 13: B1A1, channel 128, before bonding. Parameter=no. of active ADCs

3.2 Dummy bond on input pads

ASIC configuration: JC configuration (tables 1 & 2).
Wirebonds bonded to the SALT input pads 0 and 128 and cut off (second side not bonded anywhere). As a result each pad has dangling wirebond connected to it.

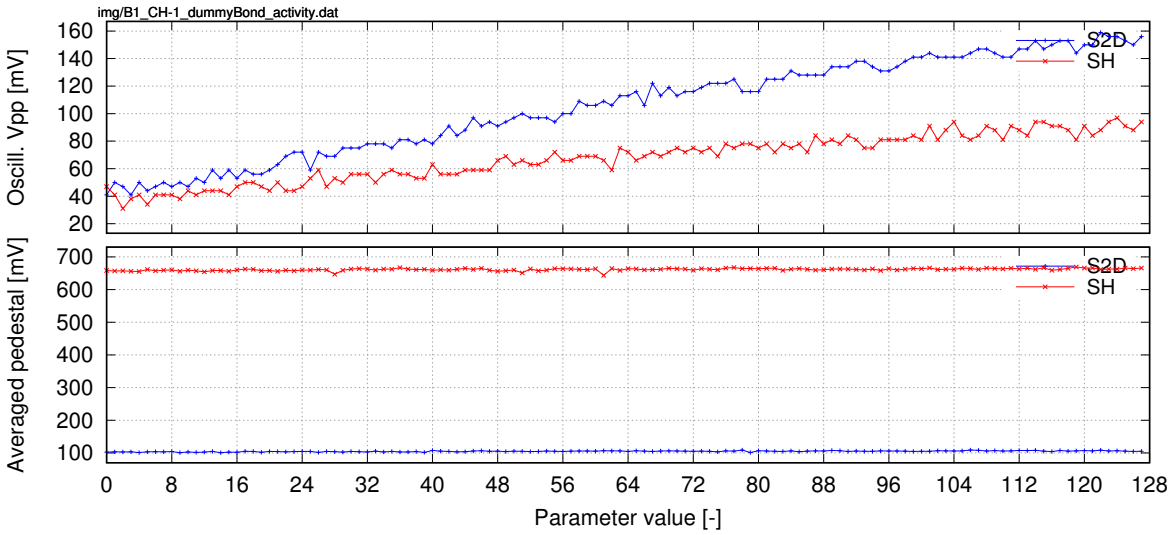

Figure 14: B1A1, channel -1, dummy bond. Parameter=no. of active ADCs

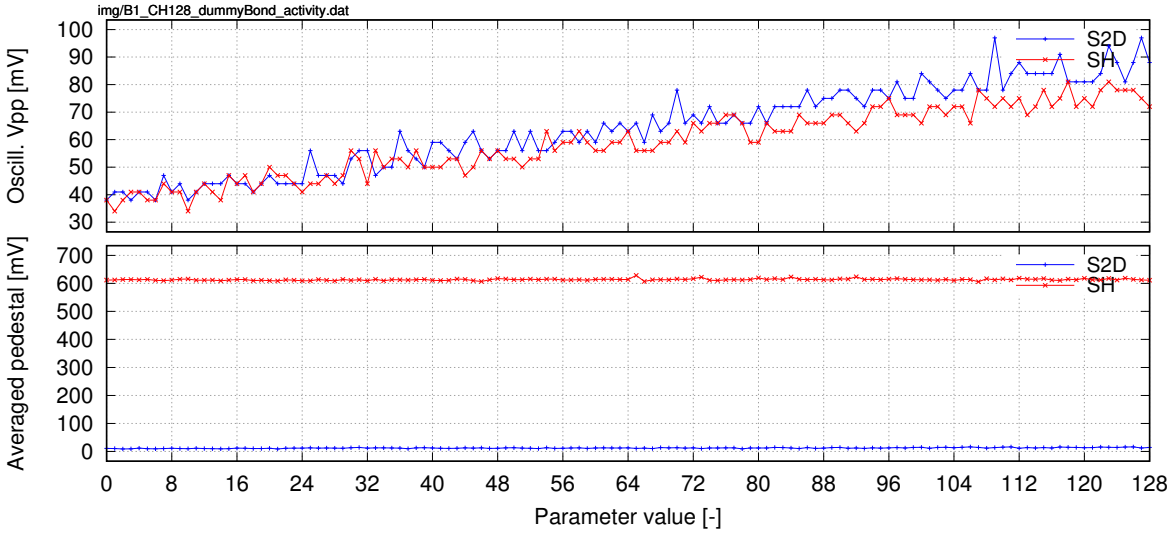

Figure 15: B1A1, channel 128, dummy bond. Parameter=no. of active ADCs

3.3 Cap-PCB bonded, no capacitors assembled

Empty Cap-PCB assembled, bonded to SALT input pads 0 and 127 (no capacitors assembled to the cap-PCB).

3.3.1 Default ASIC configuration

ASIC configuration: JC configuration (tables 1 & 2).

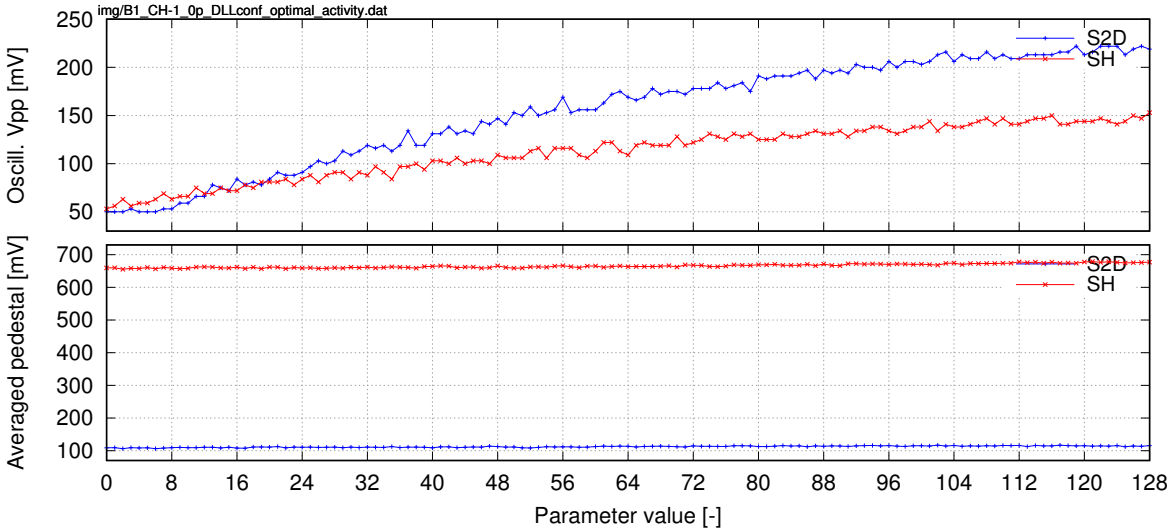

Figure 16: B1A1, channel -1, Empty cap-PCB bonded. Parameter=no. of active ADCs

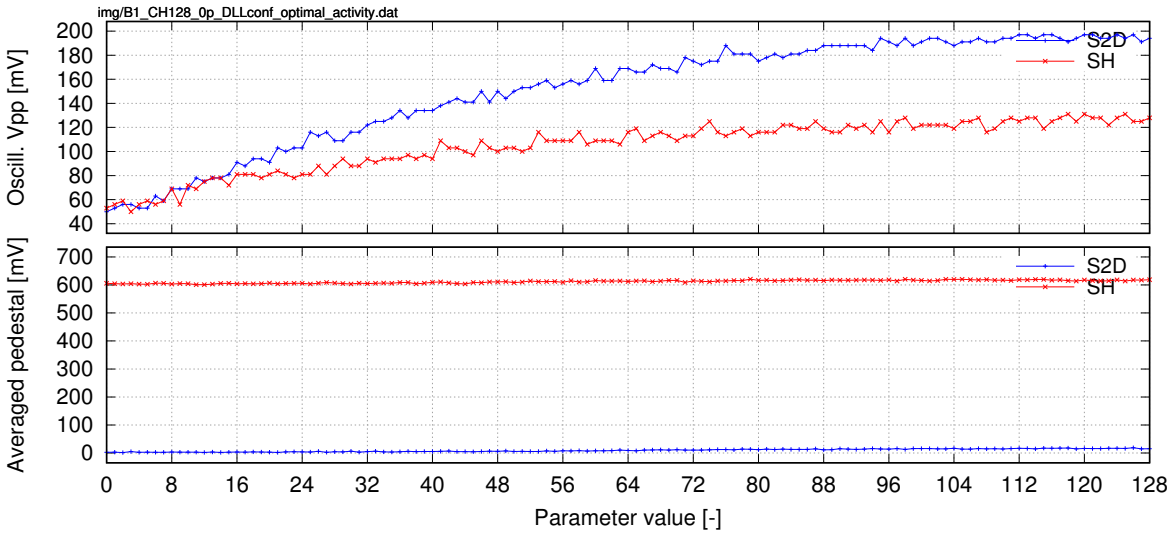

Figure 17: B1A1, channel 128, Empty cap-PCB bonded. Parameter=no. of active ADCs

3.3.2 Optimized test pulse and ADC delay

ASIC configuration: JC configuration (tables 1 & 2) + test pulse and ADC delay optimizations (table 3).

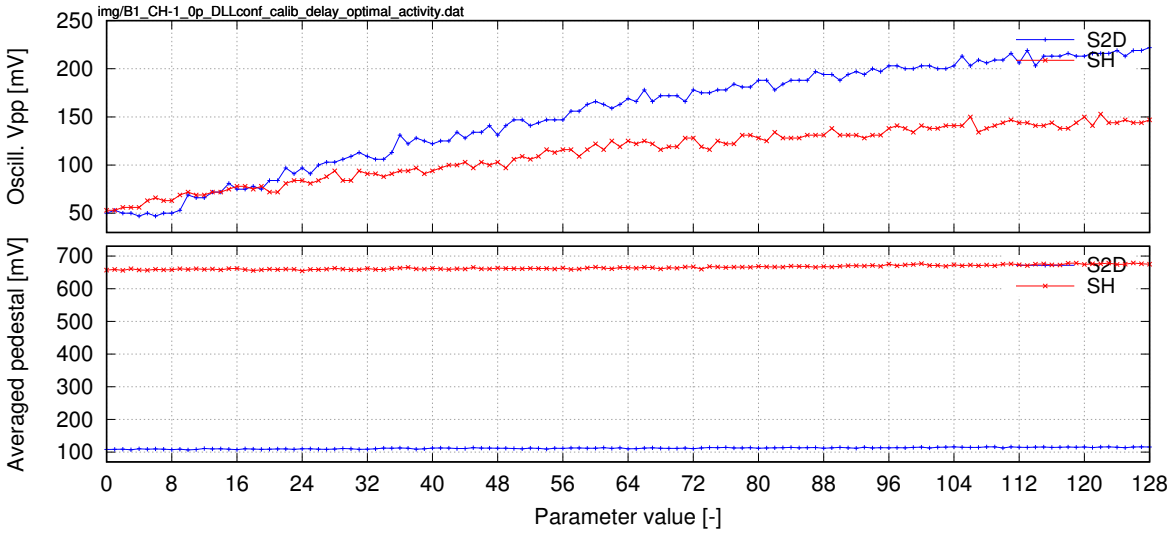

Figure 18: B1A1, channel -1, Empty cap-PCB bonded. Optimized test pulse and ADC delay. Parameter=no. of active ADCs

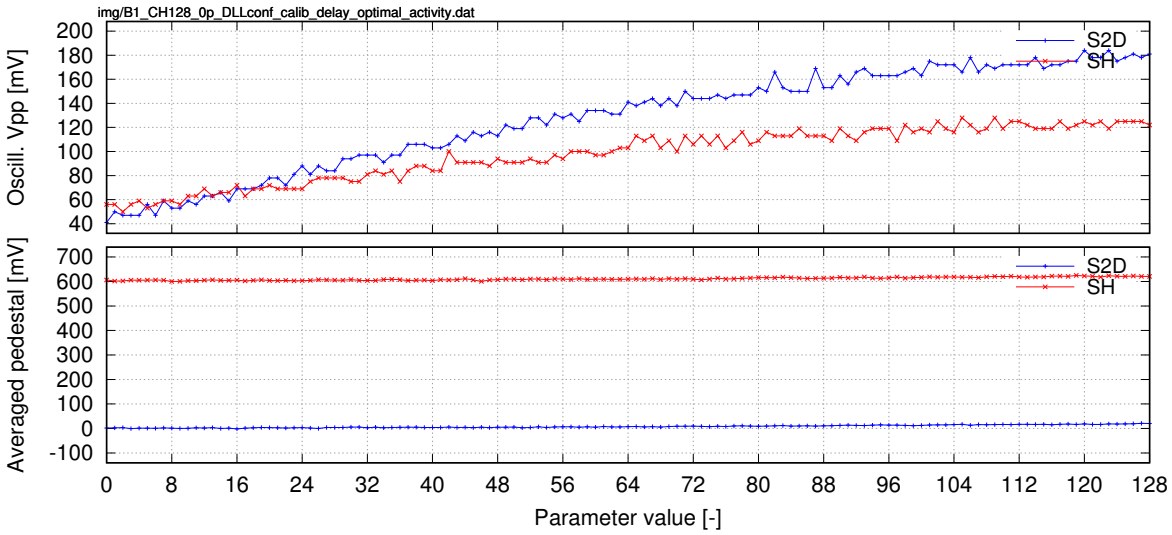

Figure 19: B1A1, channel 128, Empty cap-PCB bonded. Optimized test pulse and ADC delay. Parameter=no. of active ADCs

3.4 Cap-PCB bonded, 2.2 pF capacitors assembled

Cap-PCB assembled, bonded to SALT input pads 0 and 127, two 2.2 pF capacitors assembled to the cap-PCB.

3.4.1 Default ASIC configuration

ASIC configuration: JC configuration (tables 1 & 2).

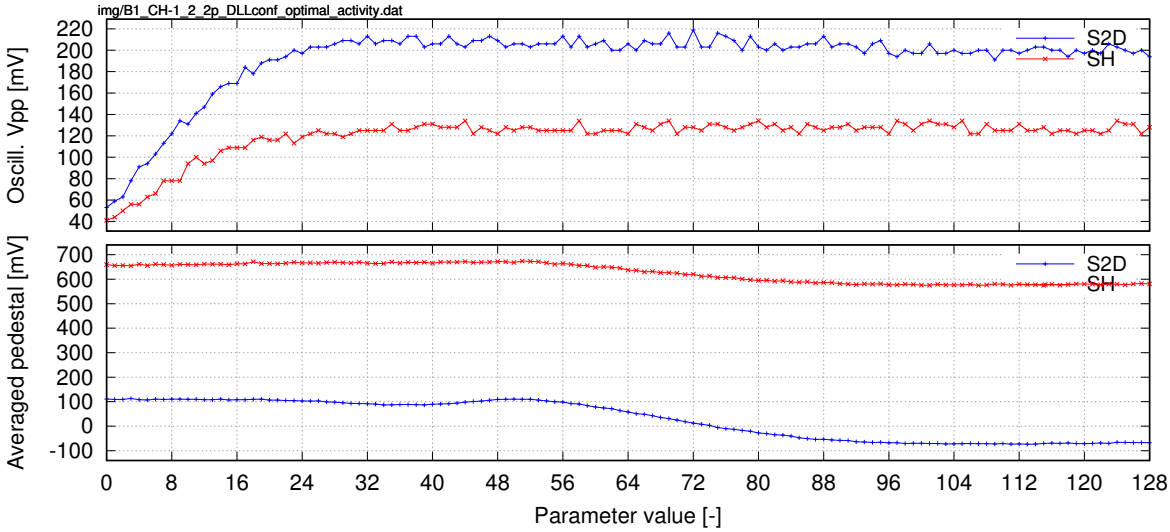

Figure 20: B1A1, channel -1, cap-PCB bonded, 2.2 pF capacitors assembled. Parameter=no. of active ADCs

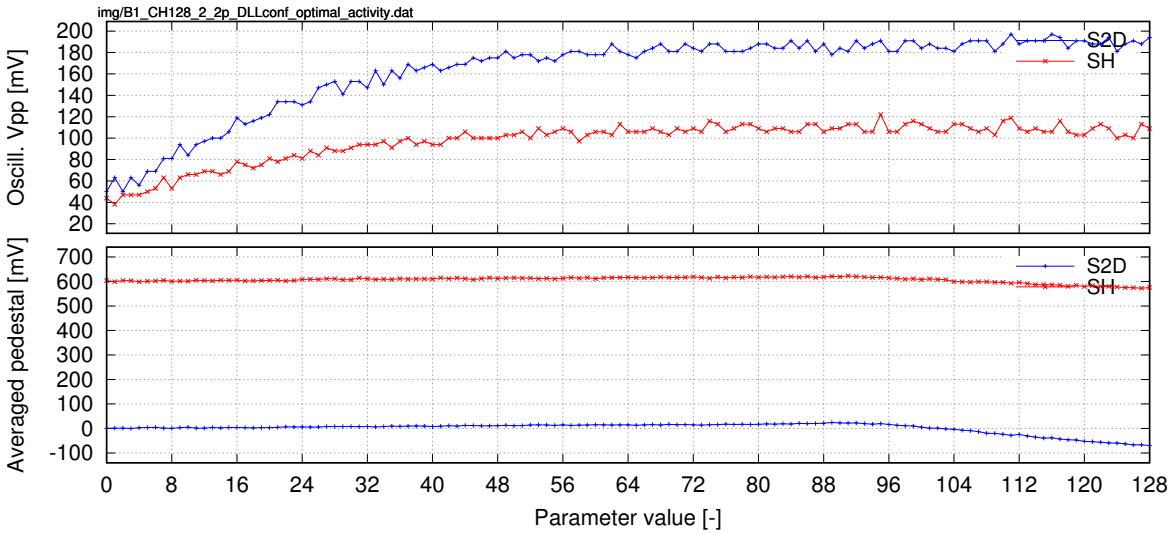

Figure 21: B1A1, channel 128, cap-PCB bonded, 2.2 pF capacitors assembled. Parameter=no. of active ADCs

3.4.2 Optimized test pulse and ADC delay

ASIC configuration: JC configuration (tables 1 & 2) + test pulse and ADC delay optimizations (table 3).

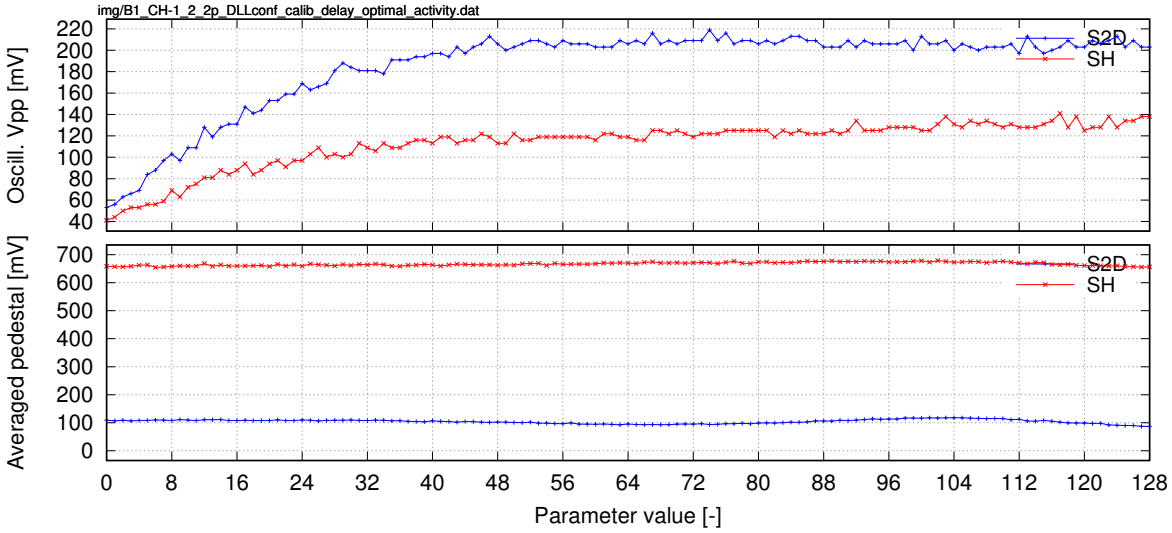

Figure 22: B1A1, channel -1, cap-PCB bonded, 2.2 pF capacitors assembled. Optimized test pulse and ADC delay. Parameter=no. of active ADCs

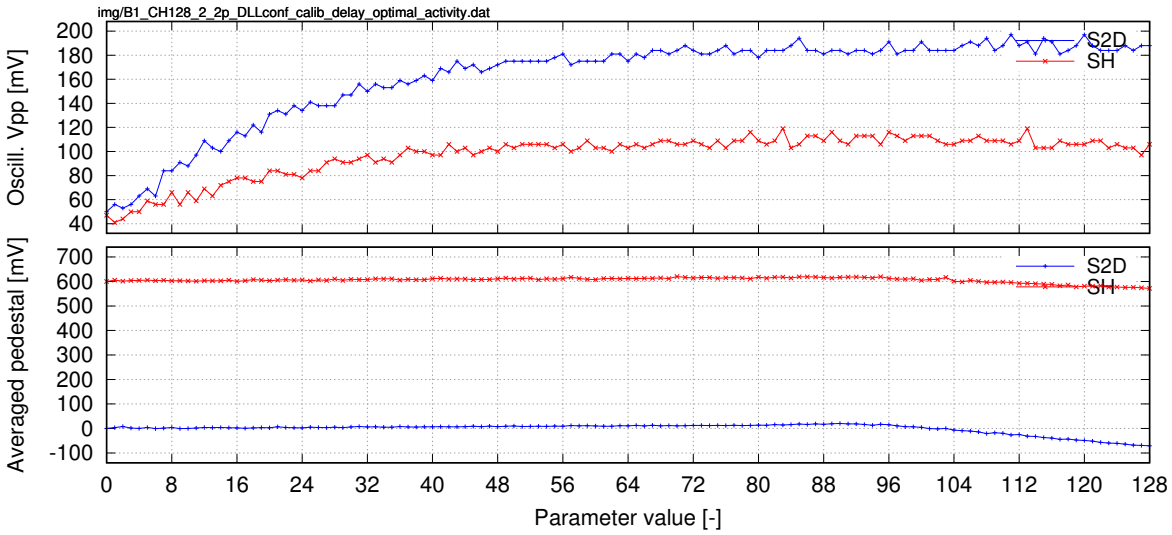

Figure 23: B1A1, channel 128, cap-PCB bonded, 2.2 pF capacitors assembled. Optimized test pulse and ADC delay. Parameter=no. of active ADCs

3.5 Cap-PCB bonded, 12 pF capacitors assembled

Cap-PCB assembled, bonded to SALT input pads 0 and 127, two 12 pF capacitors assembled to the cap-PCB.

3.5.1 Default ASIC configuration

ASIC configuration: JC configuration (tables 1 & 2).

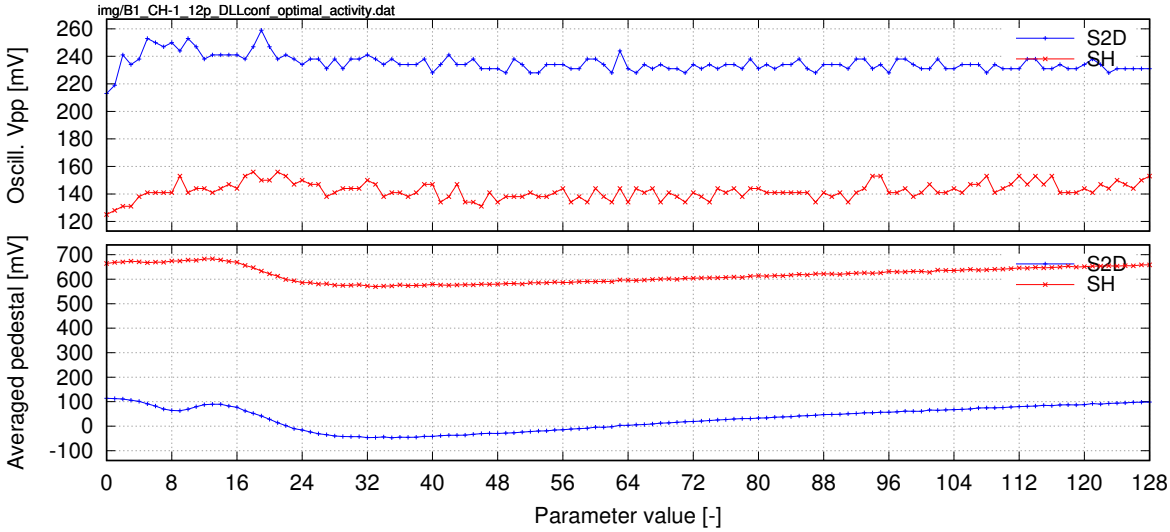

Figure 24: B1A1, channel -1, cap-PCB bonded, 12 pF capacitors assembled. Parameter=no. of active ADCs

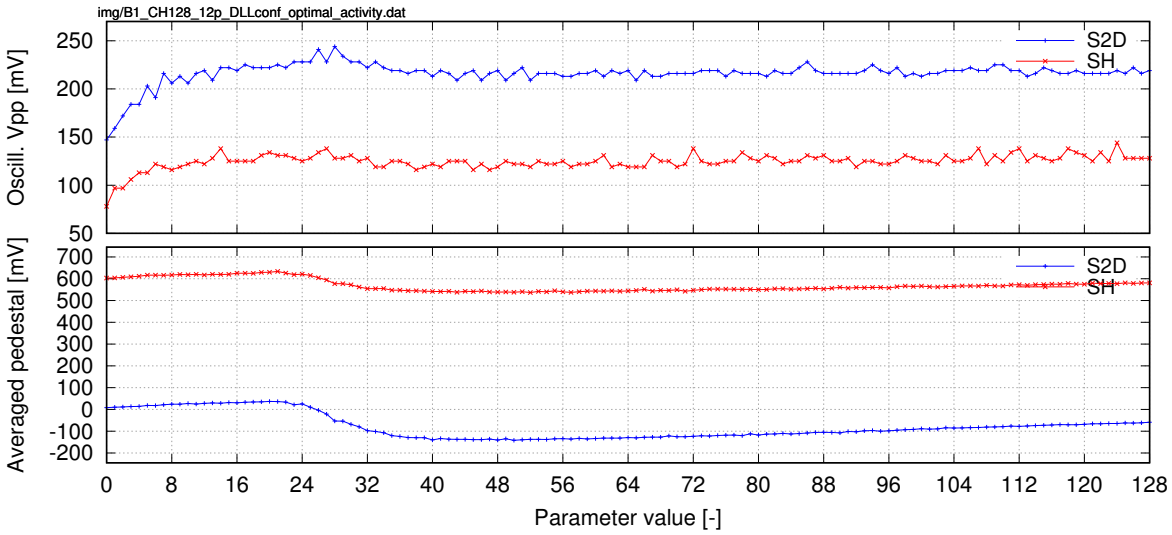

Figure 25: B1A1, channel 128, cap-PCB bonded, 12 pF capacitors assembled. Parameter=no. of active ADCs

3.5.2 Optimized test pulse and ADC delay

ASIC configuration: JC configuration (tables 1 & 2) + test pulse and ADC delay optimizations (table 3).

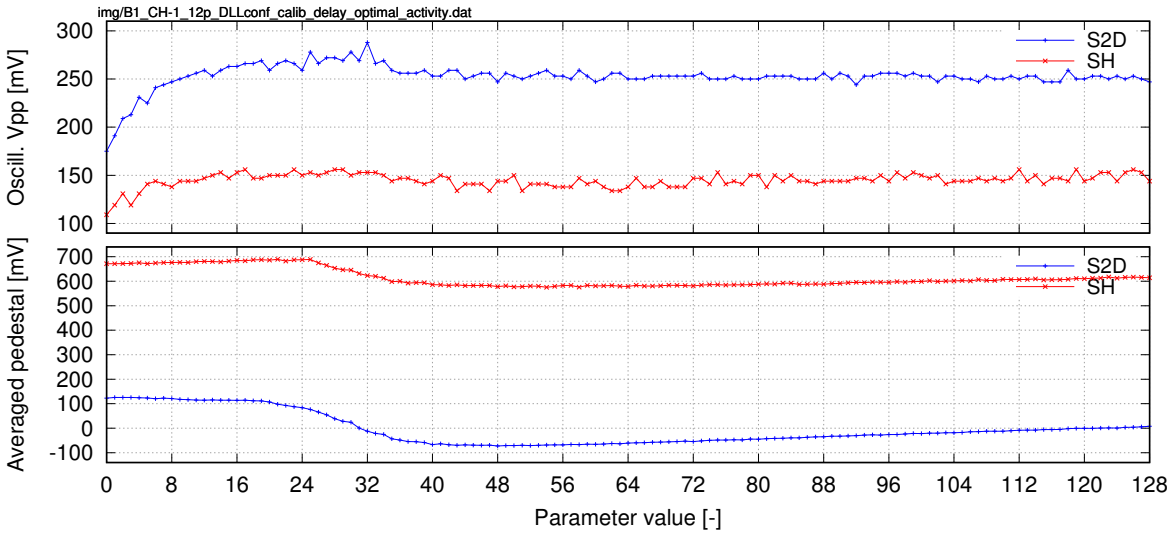

Figure 26: B1A1, channel -1, cap-PCB bonded, 12 pF capacitors assembled. Optimized test pulse and ADC delay. Parameter=no. of active ADCs

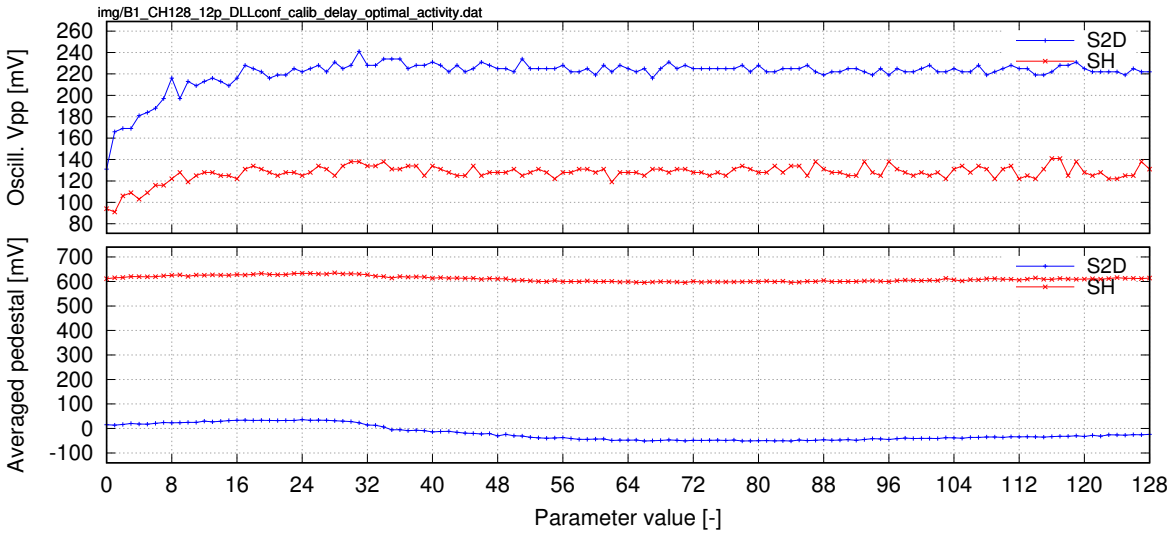

Figure 27: B1A1, channel 128, cap-PCB bonded, 12 pF capacitors assembled. Optimized test pulse and ADC delay. Parameter=no. of active ADCs

3.6 Cap-PCB bonded, 12 pF capacitors + 620 kΩ resistors assembled

Cap-PCB assembled, bonded to SALT input pads 0 and 127, two 12 pF capacitors assembled to the cap-PCB, 620 kΩ resistors soldered in parallel to the capacitors. Only channel -1 measured.

3.6.1 Default ASIC configuration

ASIC configuration: JC configuration (tables 1 & 2).

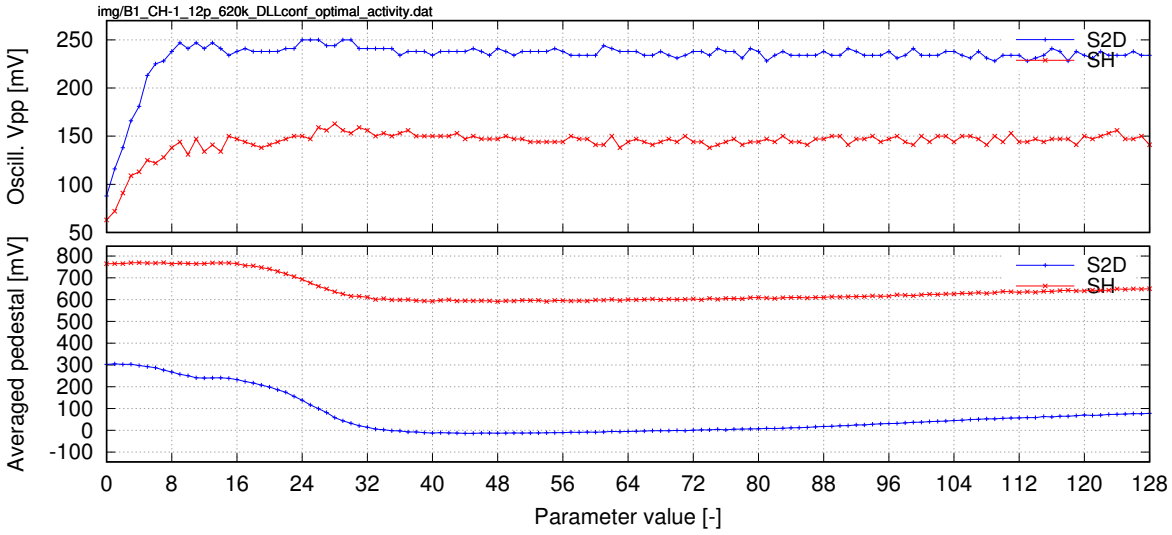

Figure 28: B1A1, channel -1, cap-PCB bonded, 12 pF capacitors + 620 kΩ resistors assembled. Parameter=no. of active ADCs

3.6.2 Optimized test pulse and ADC delay

ASIC configuration: JC configuration (tables 1 & 2) + test pulse and ADC delay optimizations (table 3).

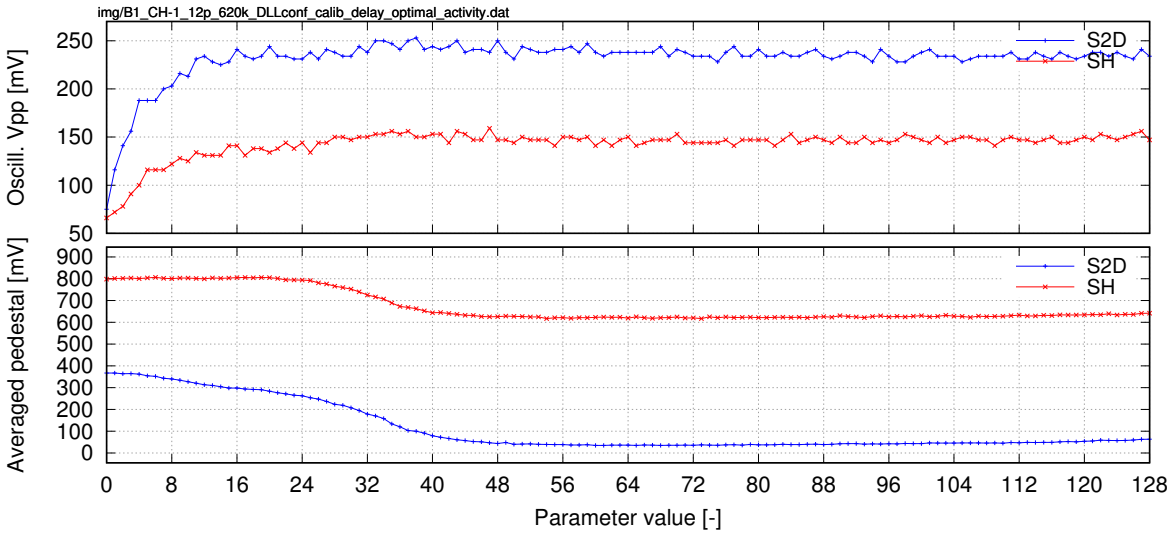

Figure 29: B1A1, channel -1, cap-PCB bonded, 12 pF capacitors + 620 kΩ resistors assembled. Optimized test pulse and ADC delay. Parameter=no. of active ADCs

3.7 Cap-PCB bonded, 12 pF capacitors + 620 kΩ resistors assembled; Ibuf current maximized

Cap-PCB assembled, bonded to SALT input pads 0 and 127, two 12 pF capacitors assembled to the cap-PCB, 620 kΩ resistors soldered in parallel to the capacitors.
Ibuf current maximized – 1 kΩ resistor between VDDA and Ibuf pad.
Only channel -1 measured.

3.7.1 Default ASIC configuration

ASIC configuration: JC configuration (tables 1 & 2).

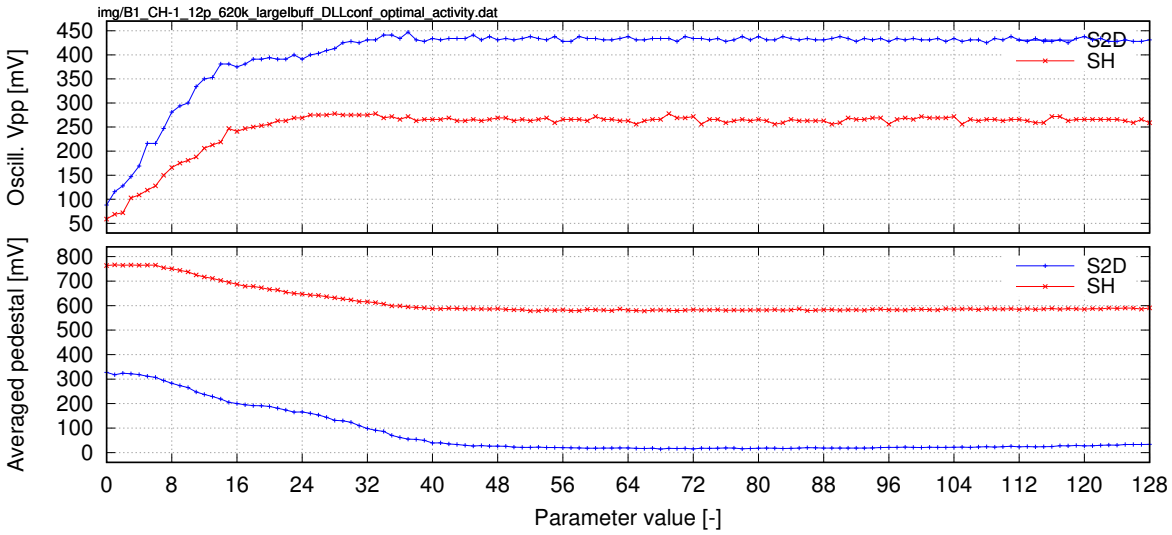

Figure 30: B1A1, channel -1, cap-PCB bonded, 12 pF capacitors + 620 kΩ resistors assembled; Ibuf current maximized. Parameter=no. of active ADCs

3.7.2 Optimized test pulse and ADC delay

ASIC configuration: JC configuration (tables 1 & 2) + test pulse and ADC delay optimizations (table 3).

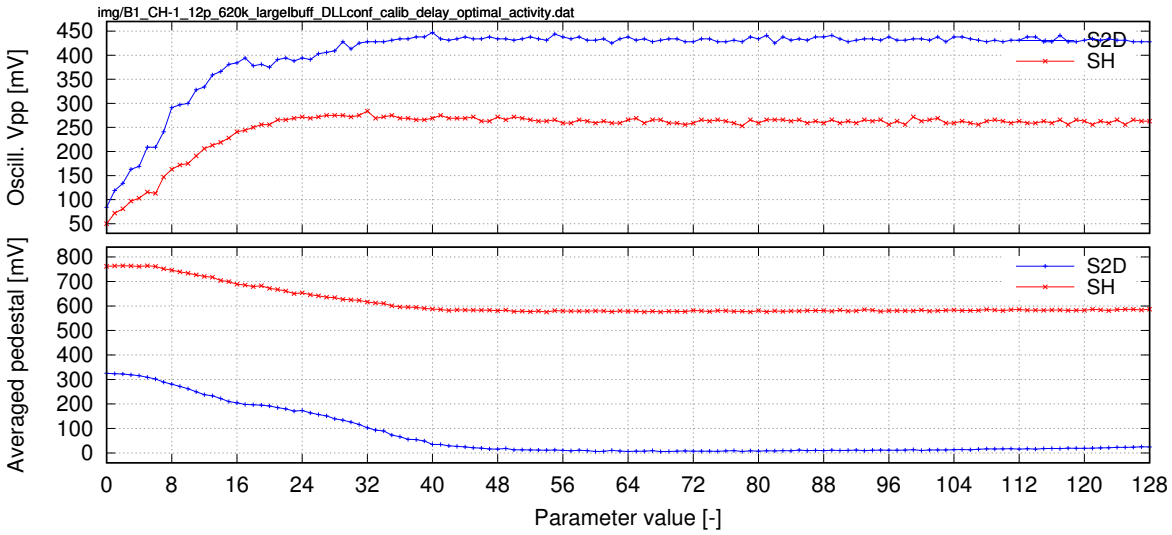

Figure 31: B1A1, channel -1, cap-PCB bonded, 12 pF capacitors + 620 kΩ resistors assembled; Ibuf current maximized. Optimized test pulse and ADC delay. Parameter=no. of active ADCs

3.8 Cap-PCB bonded, 12 pF capacitors + 820 kΩ resistors assembled; Ibuf current maximized

Cap-PCB assembled, bonded to SALT input pads 0 and 127, two 12 pF capacitors assembled to the cap-PCB, 820 kΩ resistors soldered in parallel to the capacitors.
Ibuf current maximized – 1 kΩ resistor between VDDA and Ibuf pad.
Only channel -1 measured.

3.8.1 Default ASIC configuration

ASIC configuration: JC configuration (tables 1 & 2).

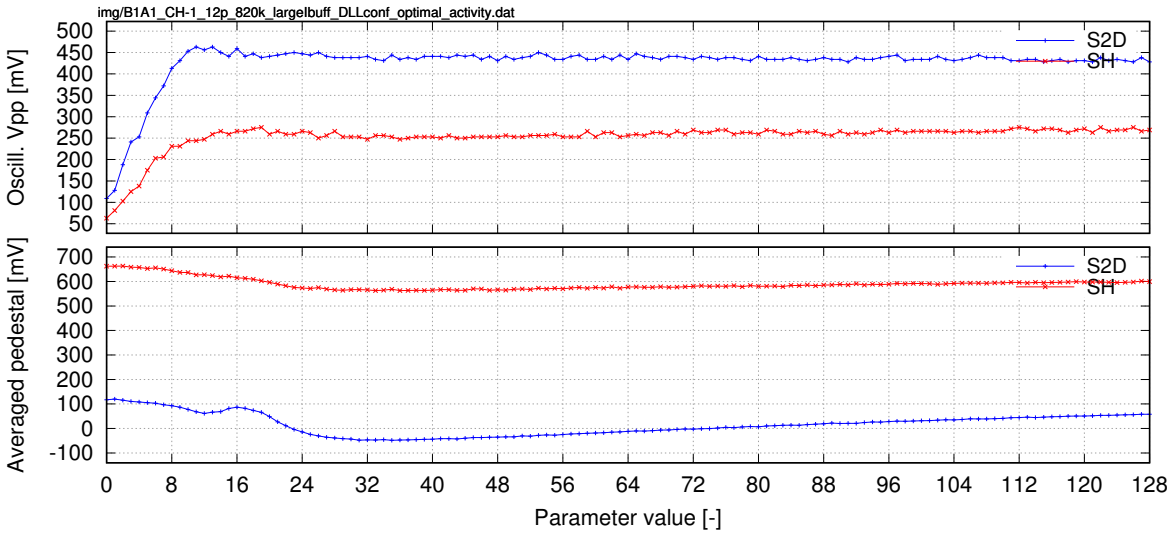

Figure 32: B1A1, channel -1, cap-PCB bonded, 12 pF capacitors + 820 kΩ resistors assembled; Ibuf current maximized. Parameter=no. of active ADCs

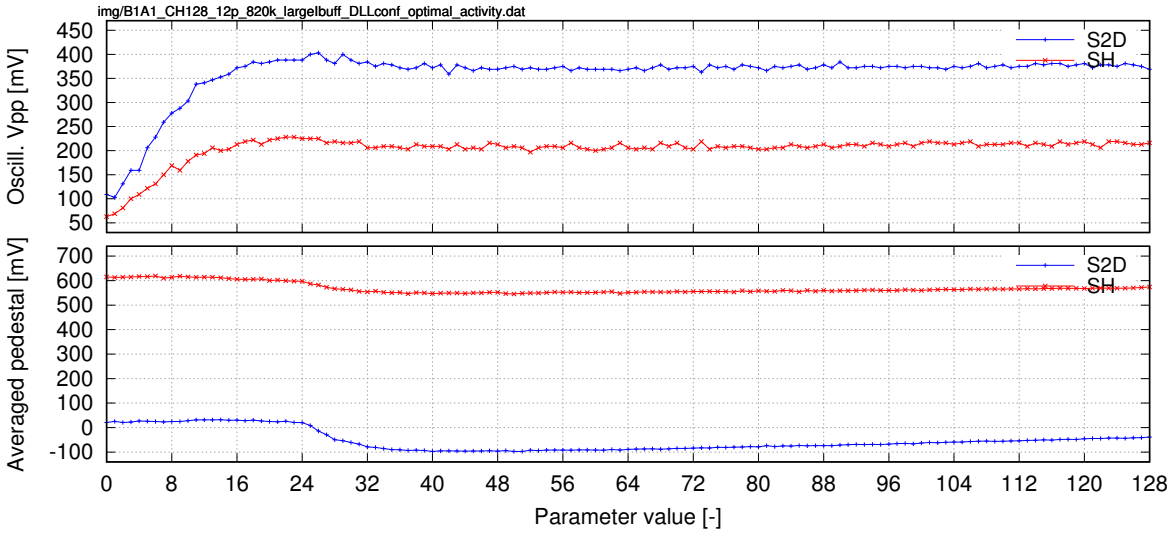

Figure 33: B1A1, channel 128, cap-PCB bonded, 12 pF capacitors + 820 kΩ resistors assembled; Ibuf current maximized. Parameter=no. of active ADCs

3.8.2 Optimized test pulse and ADC delay

ASIC configuration: JC configuration (tables 1 & 2) + test pulse and ADC delay optimizations (table 3).

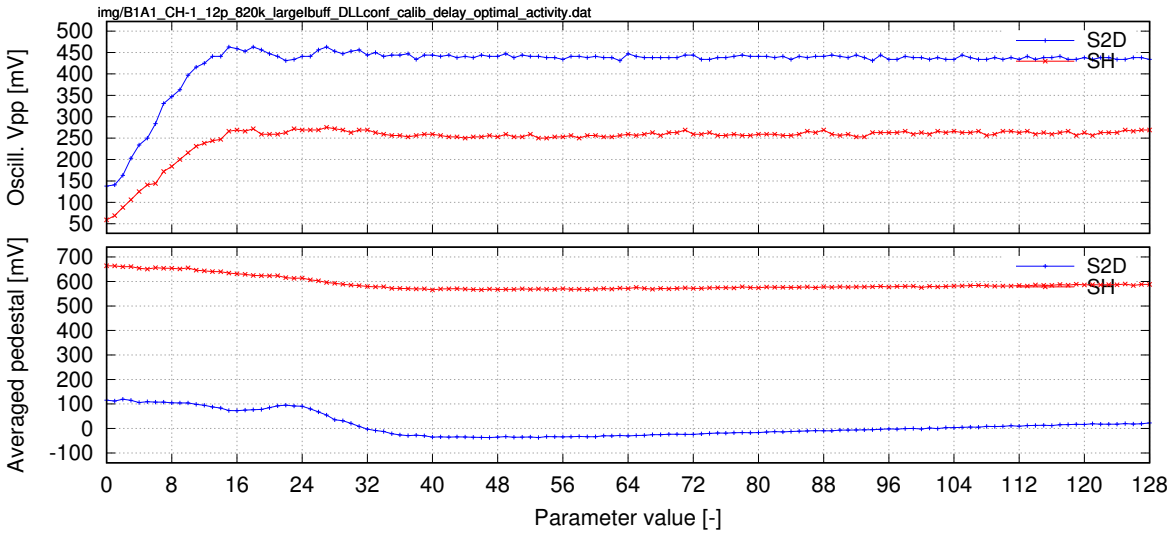

Figure 34: B1A1, channel -1, cap-PCB bonded, 12 pF capacitors + 820 kΩ resistors assembled; Ibuf current maximized. Optimized test pulse and ADC delay. Parameter=no. of active ADCs

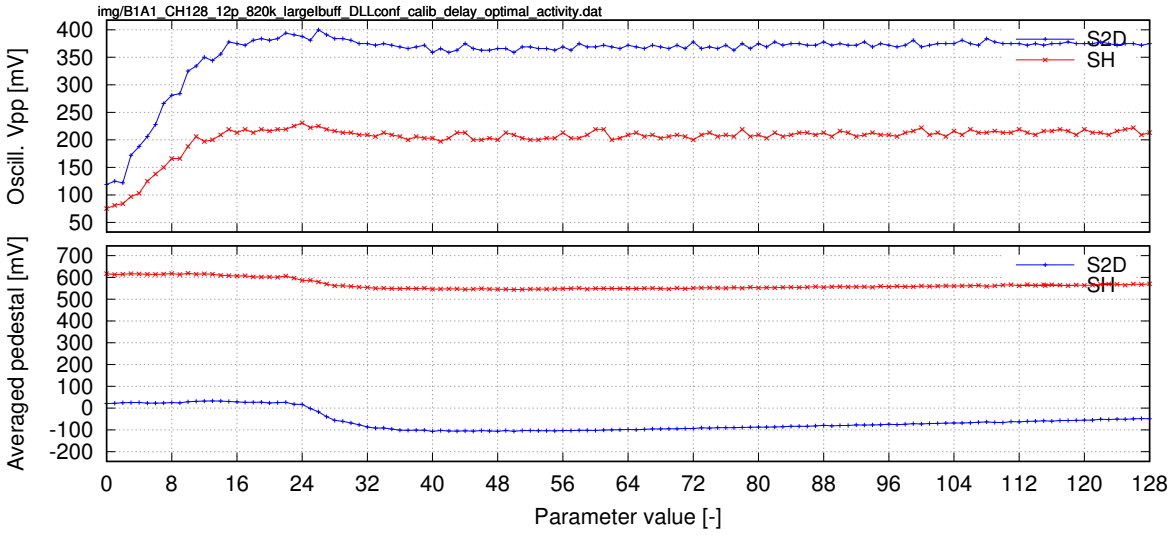

Figure 35: B1A1, channel 128, cap-PCB bonded, 12 pF capacitors + 820 kΩ resistors assembled; Ibuf current maximized. Optimized test pulse and ADC delay. Parameter=no. of active ADCs

3.9 Cap-PCB bonded, 12 pF capacitors + 820 kΩ resistors assembled; Ibuf current maximized; Preamp GND configuration – input + backside

Cap-PCB assembled, bonded to SALT input pads 0 and 127, two 12 pF capacitors assembled to the cap-PCB, 820 kΩ resistors soldered in parallel to the capacitors.
Ibuf current maximized – 1 kΩ resistor between VDDA and Ibuf pad.
Preamp GND bonded from both sides - input pads + backside (default) pads. Only channel -1 measured.

3.9.1 Default ASIC configuration

ASIC configuration: JC configuration (tables 1 & 2).

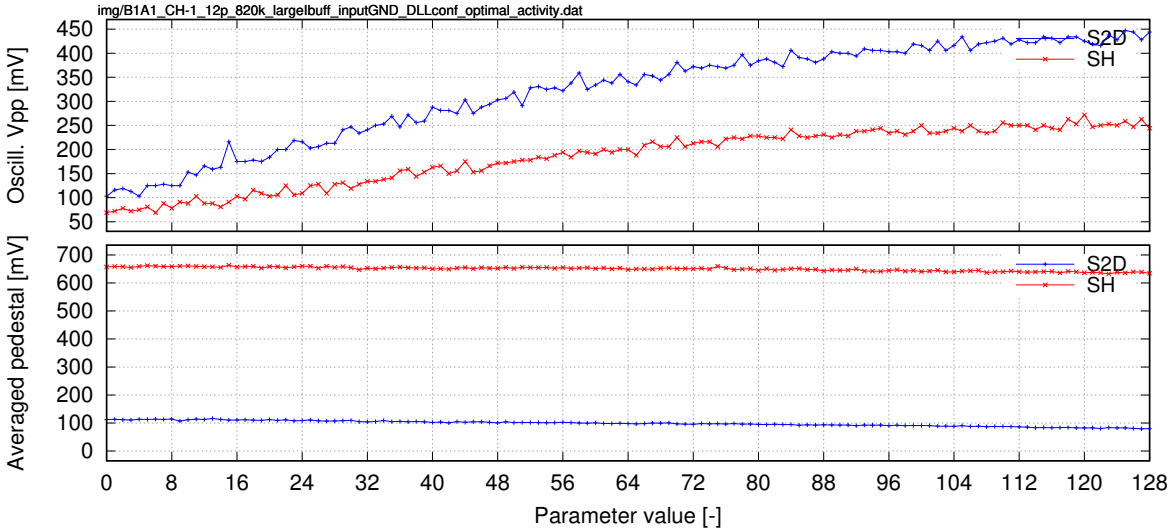

Figure 36: B1A1, channel -1, cap-PCB bonded, 12 pF capacitors + 820 kΩ resistors assembled; Ibuf current maximized; Preamp GND configuration – input + backside. Parameter=no. of active ADCs

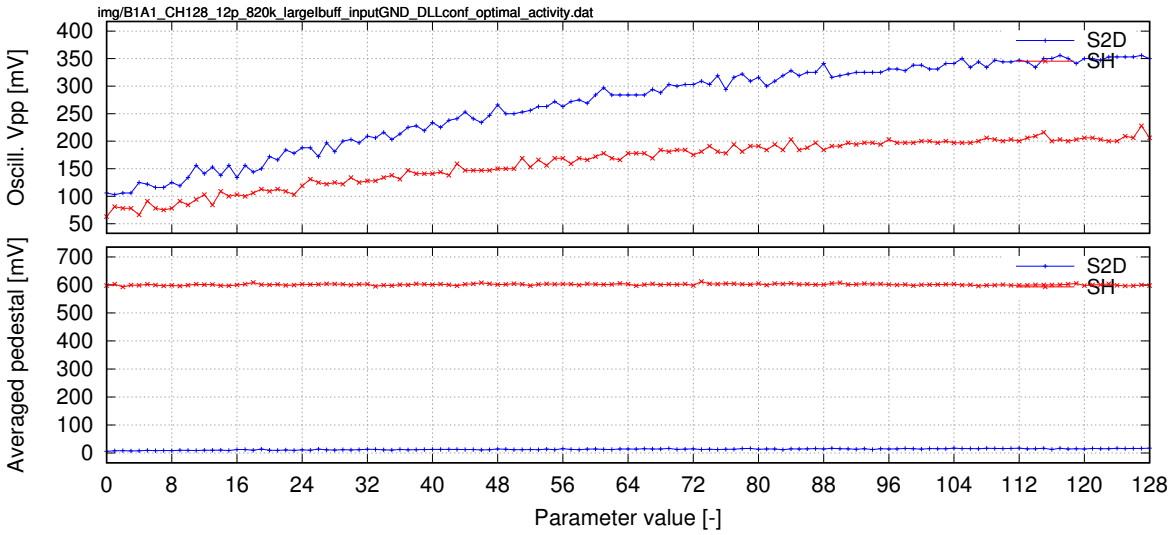

Figure 37: B1A1, channel 128, cap-PCB bonded, 12 pF capacitors + 820 kΩ resistors assembled; Ibuf current maximized; Preamp GND configuration – input + backside. Parameter=no. of active ADCs

3.9.2 Optimized test pulse and ADC delay

ASIC configuration: JC configuration (tables 1 & 2) + test pulse and ADC delay optimizations (table 3).

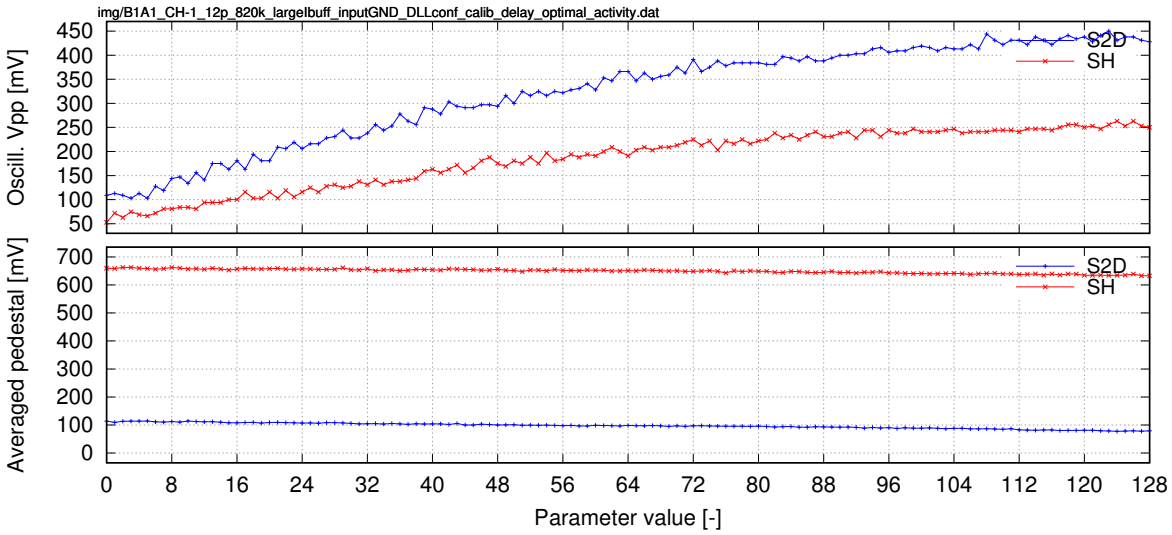

Figure 38: B1A1, channel -1, cap-PCB bonded, 12 pF capacitors + 820 kΩ resistors assembled; Ibuf current maximized; Preamp GND configuration – input + backside. Optimized test pulse and ADC delay. Parameter=no. of active ADCs

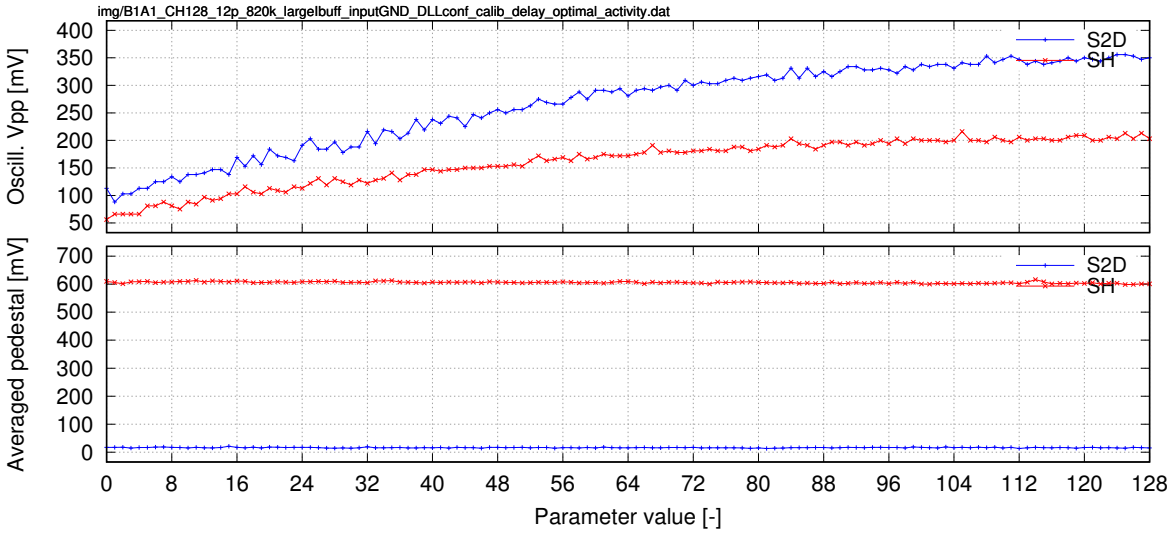

Figure 39: B1A1, channel 128, cap-PCB bonded, 12 pF capacitors + 820 kΩ resistors assembled; Ibuf current maximized; Preamp GND configuration – input + backside. Optimized test pulse and ADC delay. Parameter=no. of active ADCs

3.10 DLL and PLL stability monitoring

ASIC configuration: JC configuration (tables 1 & 2).

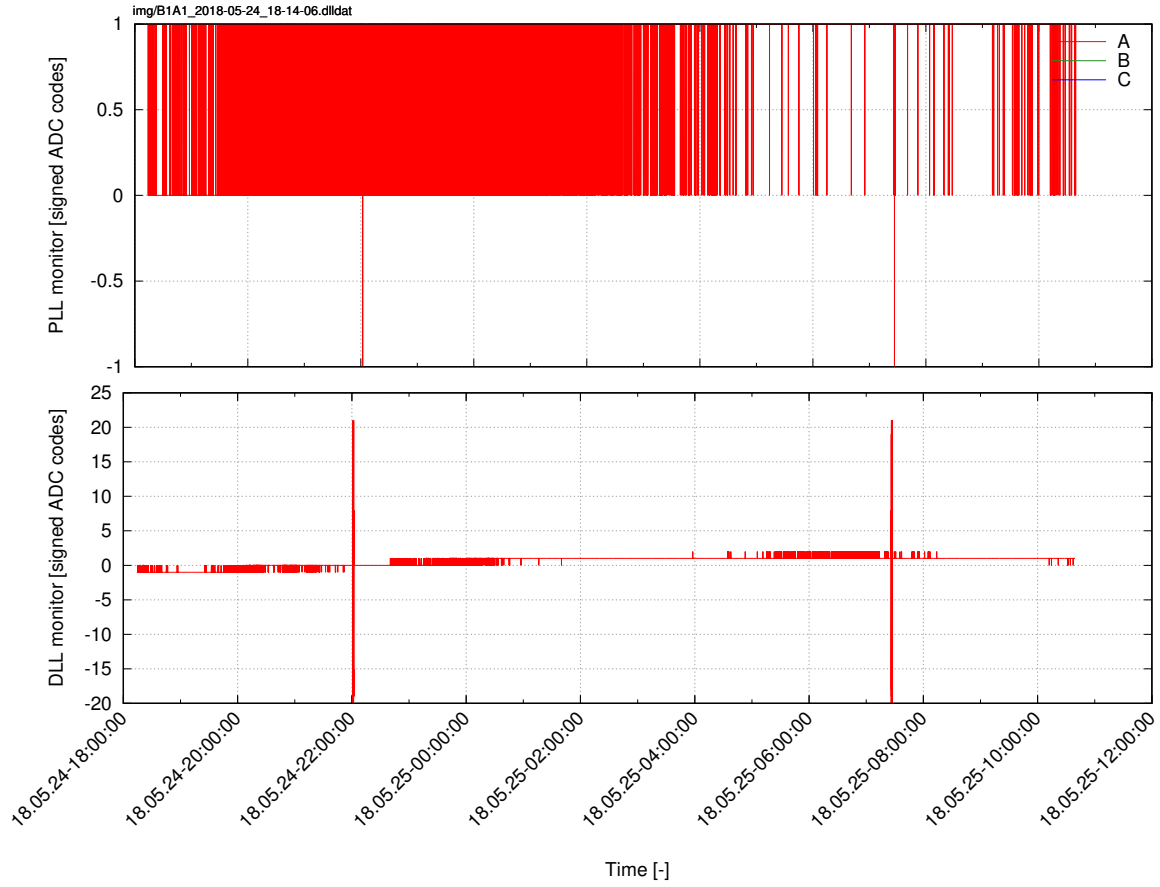

Figure 40: B1A1, DLL & PLL stability monitoring (one night); HLP active; only one PLL monitor red

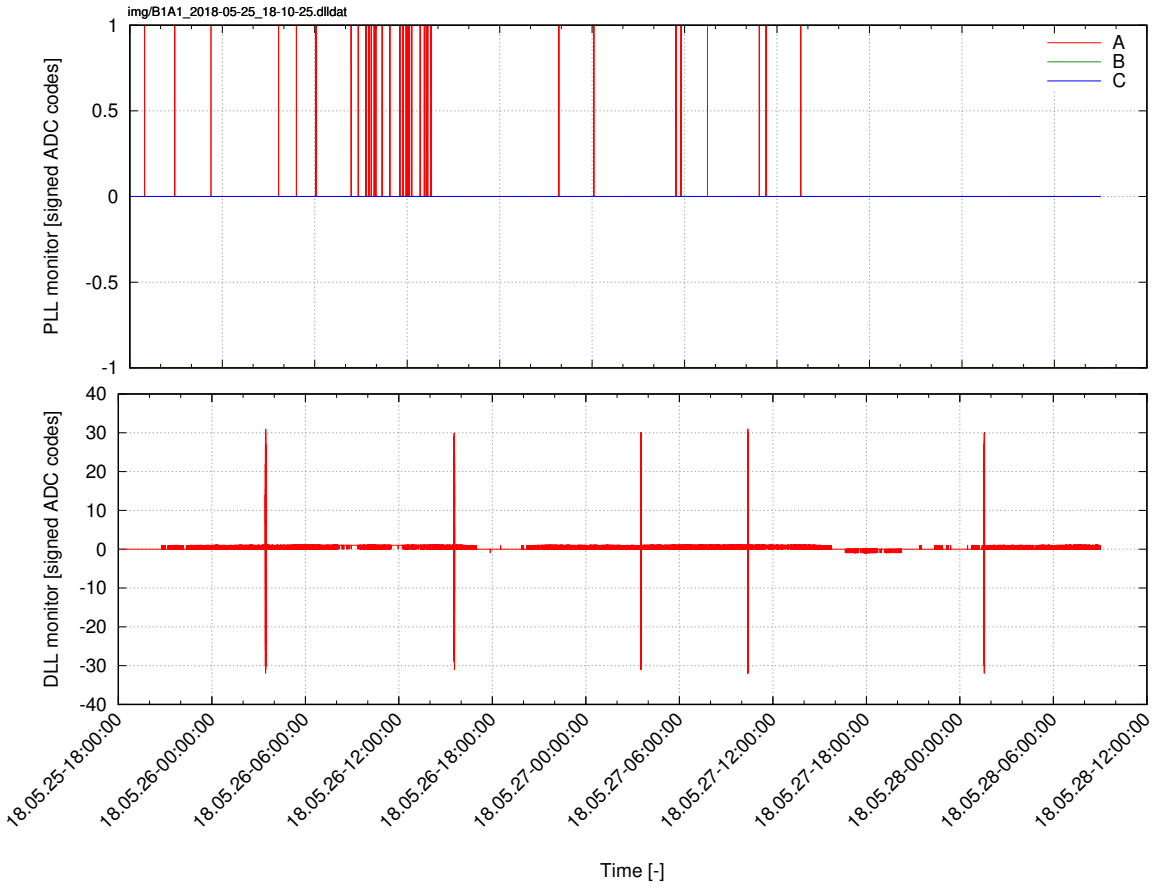

Figure 41: B1A1, DLL & PLL stability monitoring (a weekend); HLP active

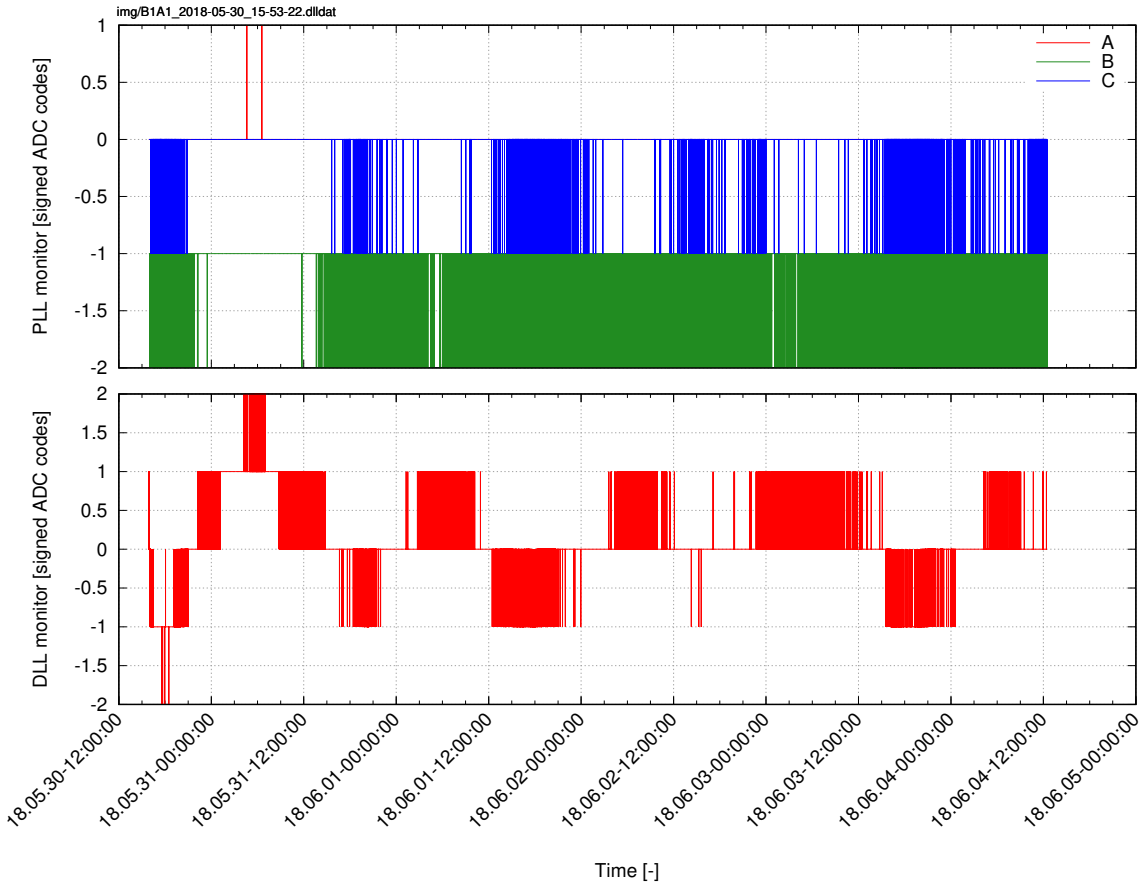

Figure 42: B1A1, DLL & PLL stability monitoring (four days); HLP inactive

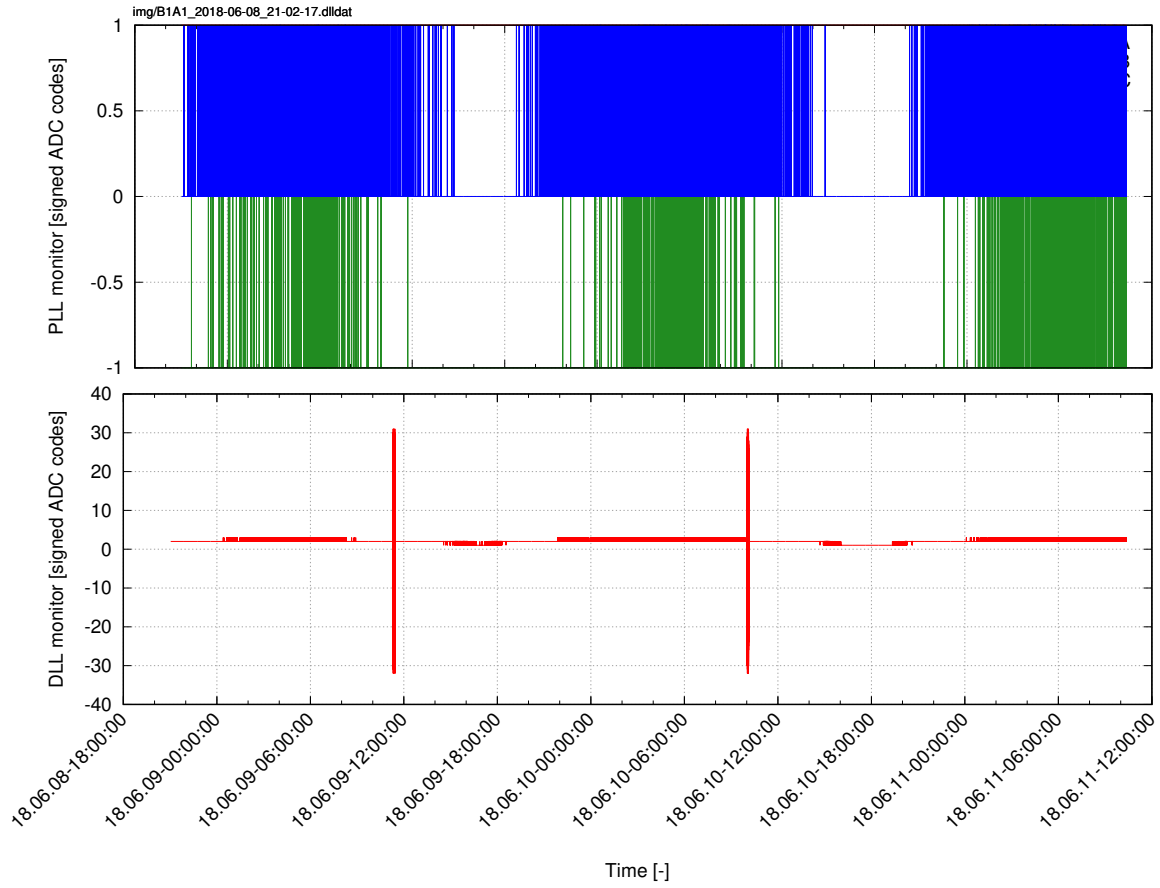

Figure 43: B1A1, DLL & PLL stability monitoring (two days); HLP active, DLL CP current lowered to 'h4

4 Board 0 with ASIC 2

Cap-PCB initially bonded with 12 pF, however a short was found on cap-PCB by removing bond from channel -1. Therefore the first results are done for channel -1 with bond removed.

4.1 Input bonds completely removed from channel -1

Cap-PCB assembled, bond to SALT input pad 0 removed, two 12 pF capacitors assembled to the cap-PCB.

4.1.1 Default ASIC configuration

ASIC configuration: JC configuration (tables 1 & 2).

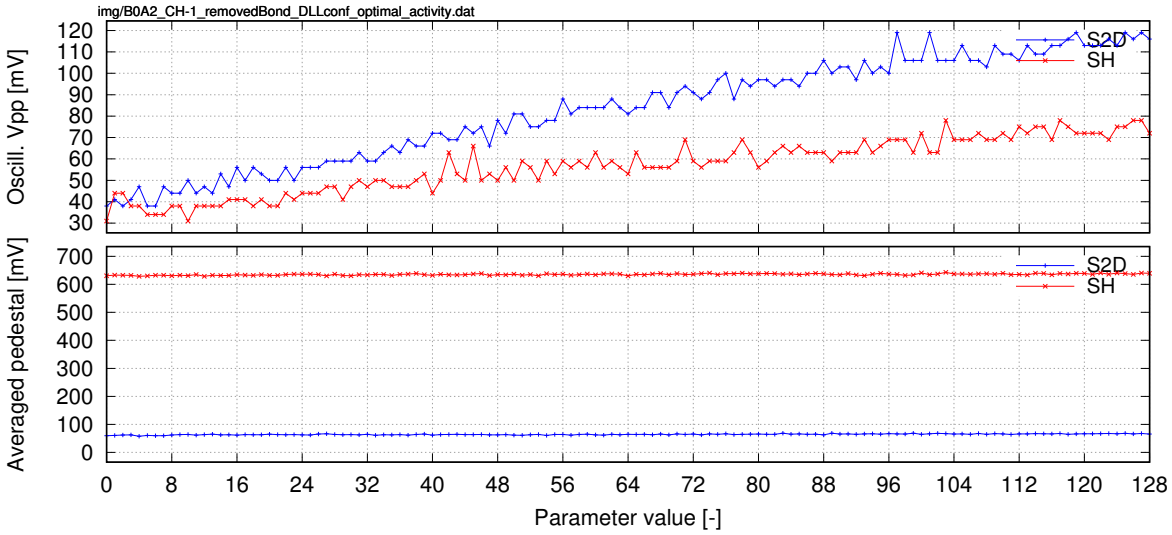

Figure 44: B0A2, channel -1, input bond removed from channel -1. Parameter=no. of active ADCs

4.1.2 Optimized test pulse and ADC delay

ASIC configuration: JC configuration (tables 1 & 2) + test pulse and ADC delay optimizations (table 3).

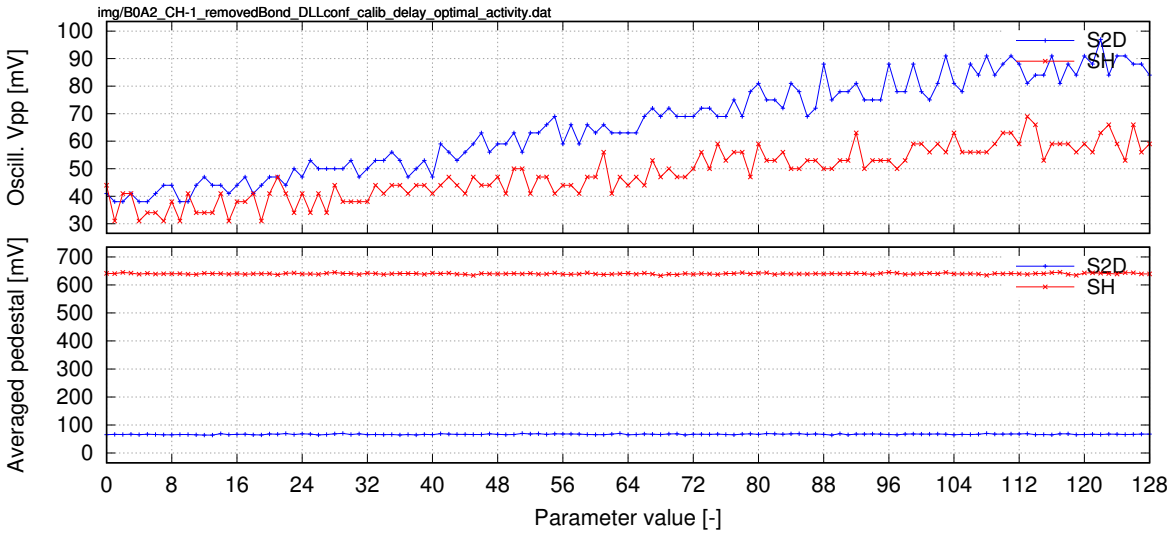

Figure 45: B0A2, channel -1, input bond removed from channel -1. Optimized test pulse and ADC delay. Parameter=no. of active ADCs

4.2 Cap-PCB bonded, 12 pF capacitors assembled; Ibuf current maximized

Cap-PCB assembled, bonded to SALT input pads 0 and 127, two 12 pF capacitors assembled to the cap-PCB.
Ibuf current maximized – 1 kΩ resistor between VDDA and Ibuf pad.
Channel 128 have damaged input.

4.2.1 Default ASIC configuration

ASIC configuration: JC configuration (tables 1 & 2).

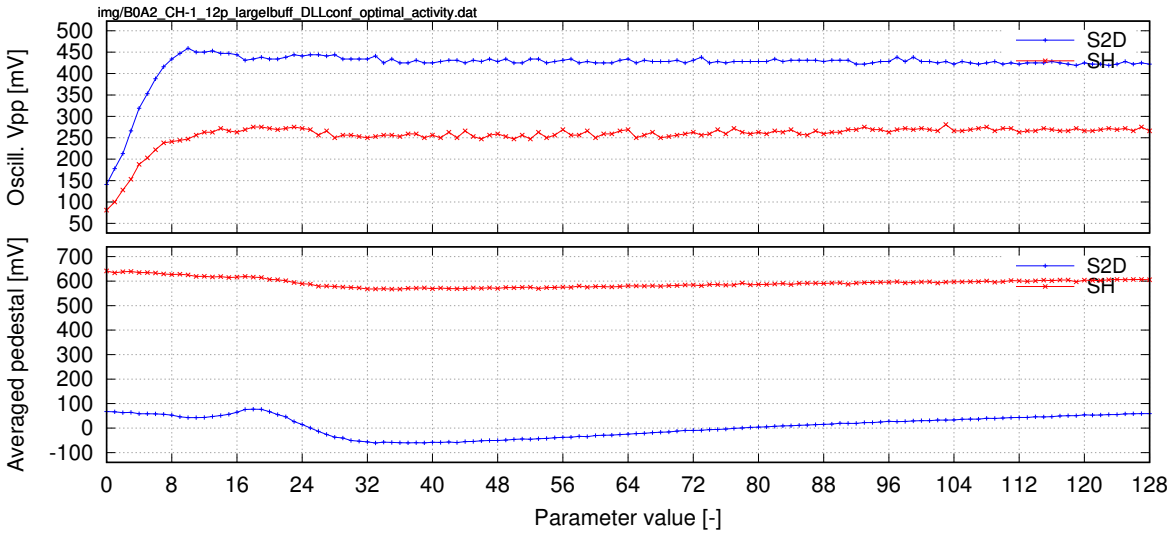

Figure 46: B0A2, channel -1, cap-PCB bonded, 12 pF capacitors; Ibuf current maximized. Parameter=no. of active ADCs

4.2.2 Optimized test pulse and ADC delay

ASIC configuration: JC configuration (tables 1 & 2) + test pulse and ADC delay optimizations (table 3).

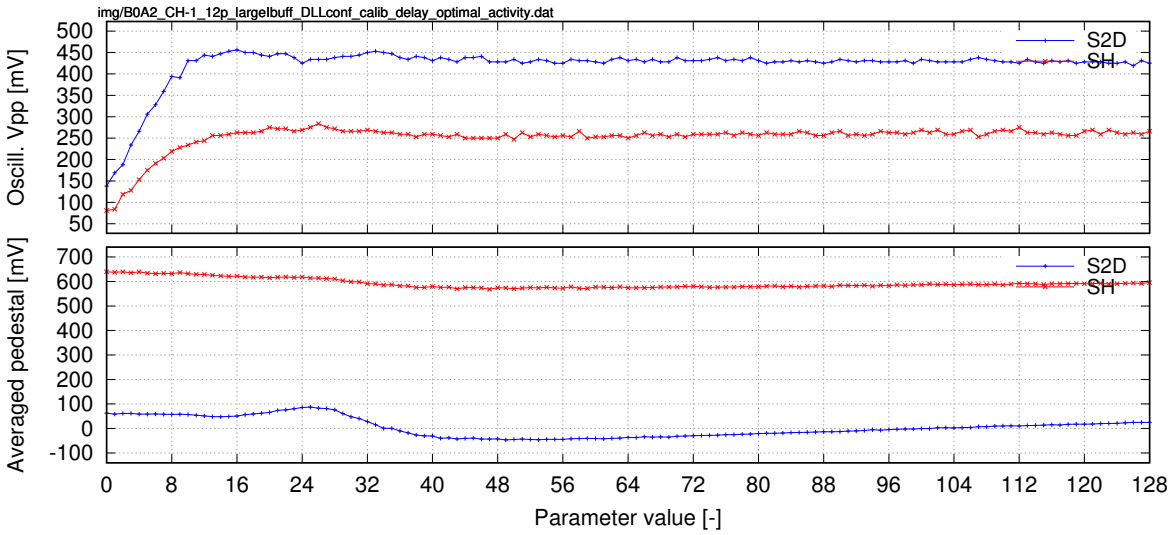

Figure 47: B0A2, channel -1, cap-PCB bonded, 12 pF capacitors; Ibuf current maximized. Optimized test pulse and ADC delay. Parameter=no. of active ADCs

4.3 Cap-PCB bonded, 12 pF capacitors + 820 kΩ resistors assembled; Ibuf current maximized

Cap-PCB assembled, bonded to SALT input pads 0 and 127, two 12 pF capacitors assembled to the cap-PCB, 820 kΩ resistors soldered in parallel to the capacitors.
Ibuf current maximized – 1 kΩ resistor between VDDA and Ibuf pad.
Channel 128 have damaged input.

4.3.1 Default ASIC configuration

ASIC configuration: JC configuration (tables 1 & 2).

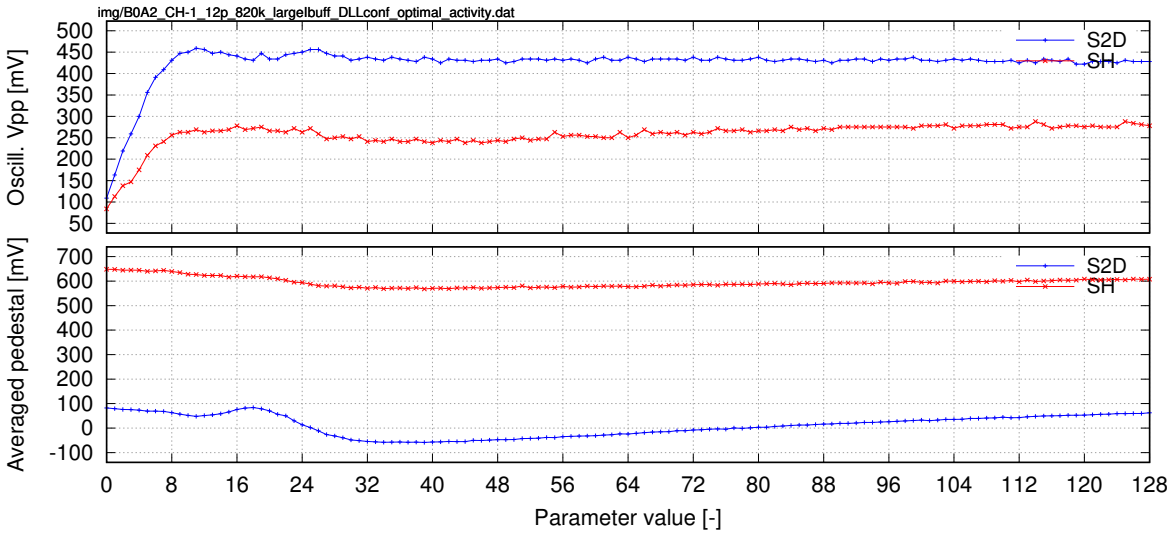

Figure 48: B0A2, channel -1, cap-PCB bonded, 12 pF capacitors + 820 kΩ resistor assembled; Ibuf current maximized. Parameter=no. of active ADCs

4.3.2 Optimized test pulse and ADC delay

ASIC configuration: JC configuration (tables 1 & 2) + test pulse and ADC delay optimizations (table 3).

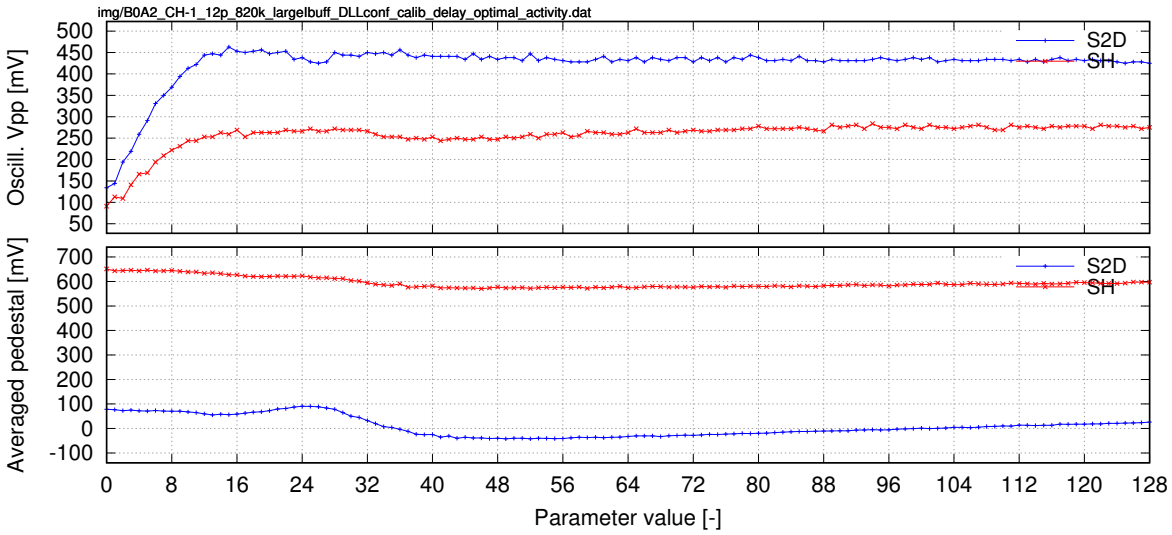

Figure 49: B0A2, channel -1, cap-PCB bonded, 12 pF capacitors + 820 kΩ resistor assembled; Ibuf current maximized. Optimized test pulse and ADC delay. Parameter=no. of active ADCs

4.4 Cap-PCB bonded, 12 pF capacitors + 820 kΩ resistors assembled; Ibuf current maximized; ADC power supply with 2.2 Ω series resistor

Cap-PCB assembled, bonded to SALT input pads 0 and 127, two 12 pF capacitors assembled to the cap-PCB, 820 kΩ resistors soldered in parallel to the capacitors.
Ibuf current maximized – 1 kΩ resistor between VDDA and Ibuf pad.
2.2 Ω resistor assembled in series between onboard decoupling power supply capacitors and VDDADC + VREFD bonds.
Channel 128 have damaged input.

4.4.1 Default ASIC configuration

ASIC configuration: JC configuration (tables 1 & 2).

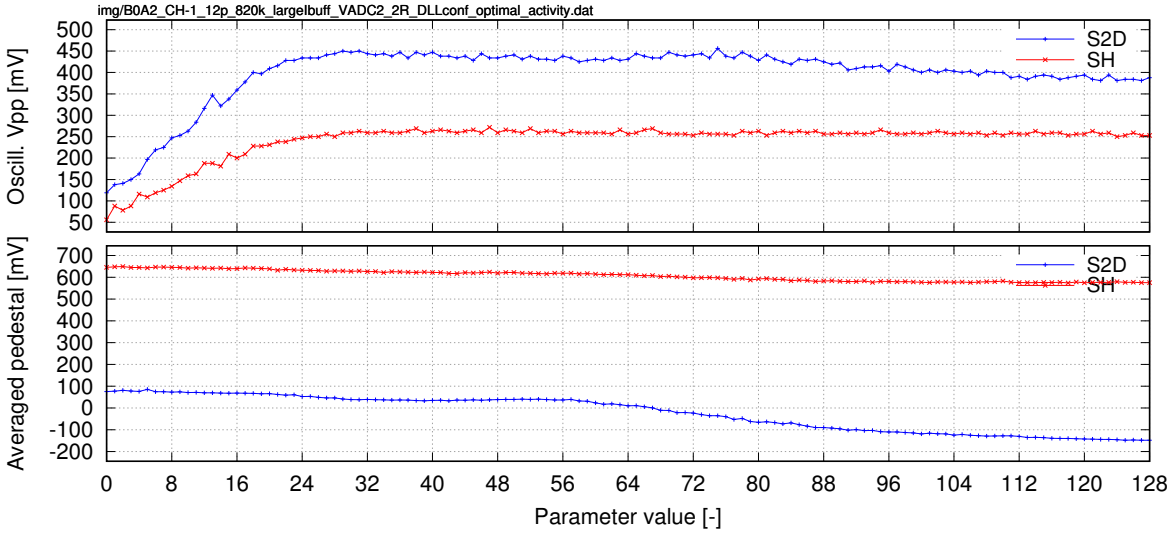

Figure 50: B0A2, channel -1, cap-PCB bonded, 12 pF capacitors + 820 kΩ resistor assembled; Ibuf current maximized; ADC power supply with 2.2 Ω series resistor. Parameter=no. of active ADCs

4.4.2 Optimized test pulse and ADC delay

ASIC configuration: JC configuration (tables 1 & 2) + test pulse and ADC delay optimizations (table 3).

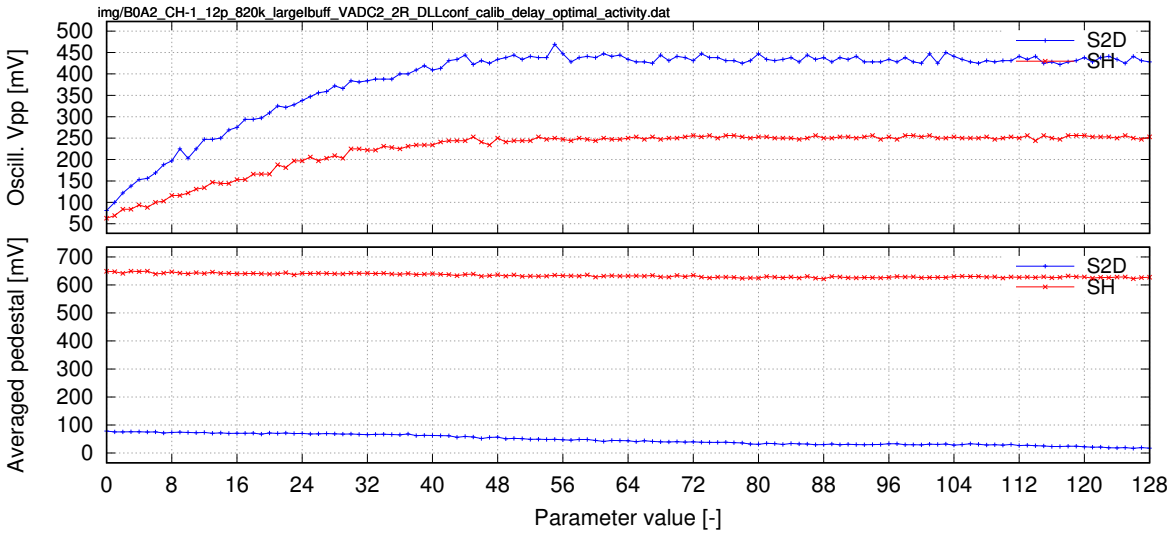

Figure 51: B0A2, channel -1, cap-PCB bonded, 12 pF capacitors + 820 kΩ resistor assembled; Ibuf current maximized; ADC power supply with 2.2 Ω series resistor. Optimized test pulse and ADC delay. Parameter=no. of active ADCs

4.5 Cap-PCB bonded, 12 pF capacitors + 820 kΩ resistors assembled; Ibuf current maximized; ADC power supply with 1 μH series inductor

Cap-PCB assembled, bonded to SALT input pads 0 and 127, two 12 pF capacitors assembled to the cap-PCB, 820 kΩ resistors soldered in parallel to the capacitors.
Ibuf current maximized – 1 kΩ resistor between VDDA and Ibuf pad.
1 μH inductor assembled in series between onboard decoupling power supply capacitors and VDDADC + VREFD bonds.
Channel 128 have damaged input.

4.5.1 Default ASIC configuration

ASIC configuration: JC configuration (tables 1 & 2).

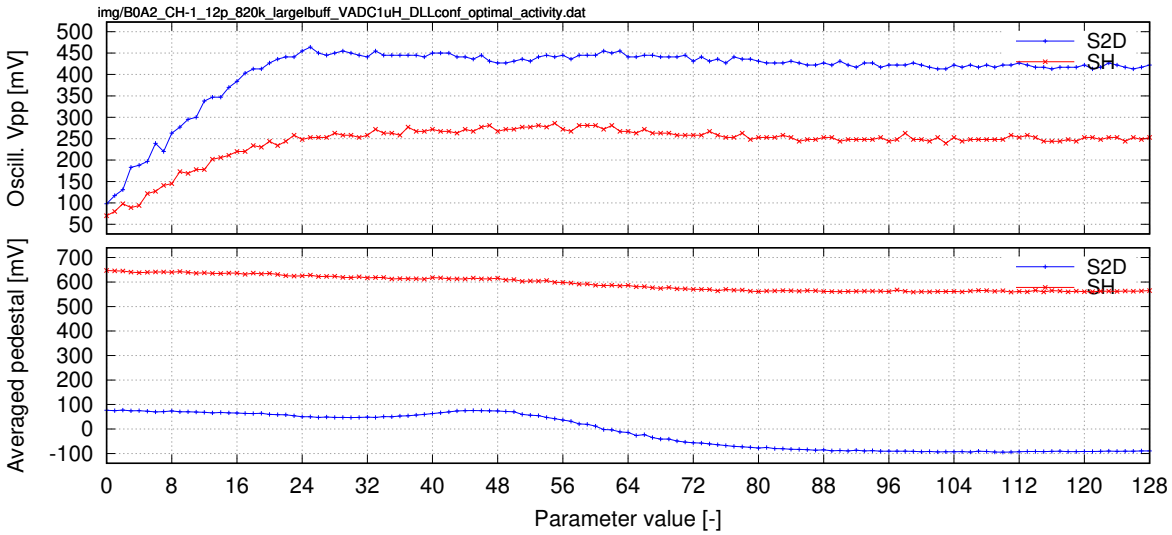

Figure 52: B0A2, channel -1, cap-PCB bonded, 12 pF capacitors + 820 kΩ resistor assembled; Ibuf current maximized; ADC power supply with 1 μH series inductor. Parameter=no. of active ADCs

4.5.2 Optimized test pulse and ADC delay

ASIC configuration: JC configuration (tables 1 & 2) + test pulse and ADC delay optimizations (table 3).

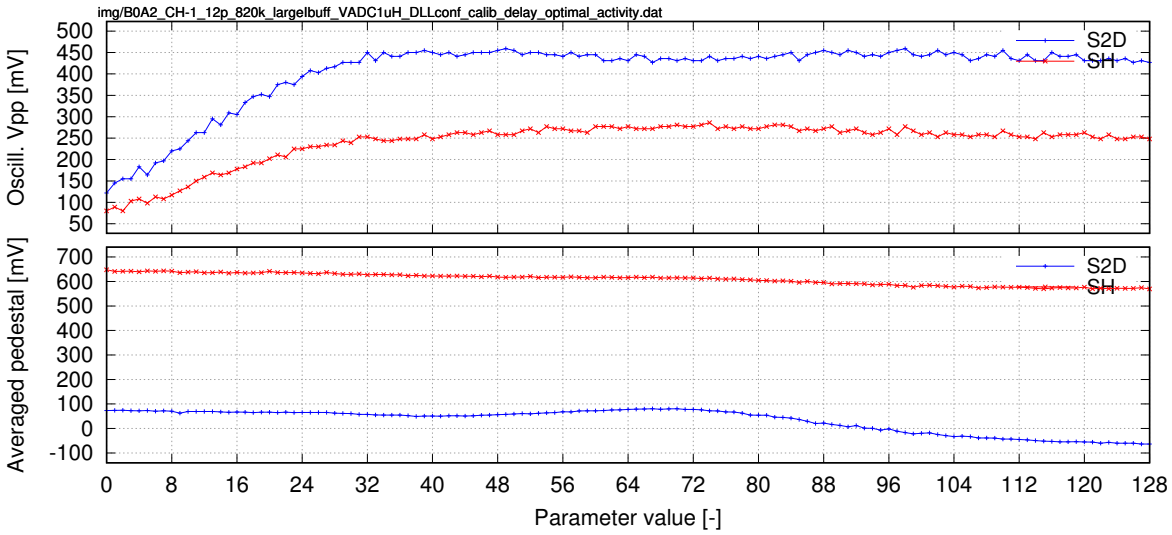

Figure 53: B0A2, channel -1, cap-PCB bonded, 12 pF capacitors + 820 kΩ resistor assembled; Ibuf current maximized; ADC power supply with 1 μH series inductor. Optimized test pulse and ADC delay. Parameter=no. of active ADCs

4.6 Cap-PCB bonded, no capacitors assembled; Ibuf current maximized; ADC power supply with 1 μH series inductor

Cap-PCB assembled, bonded to SALT input pads 0 and 127, no capacitors assembled to the cap-PCB.
Ibuf current maximized – 1 kΩ resistor between VDDA and Ibuf pad.
1 μH inductor assembled in series between onboard decoupling power supply capacitors and VDDADC + VREFD bonds.
Channel 128 have damaged input.

4.6.1 Default ASIC configuration

ASIC configuration: JC configuration (tables 1 & 2).

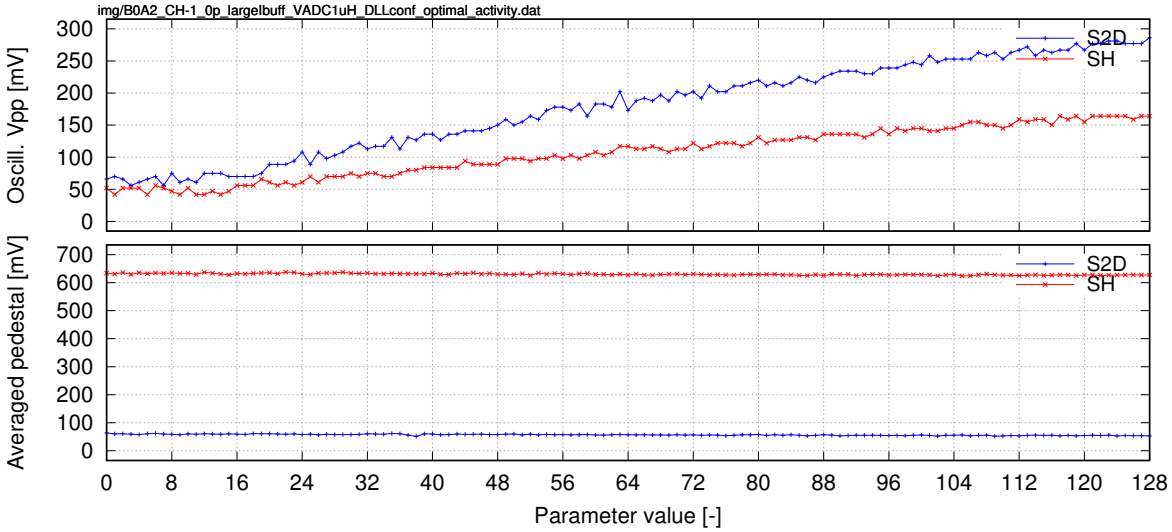

Figure 54: B0A2, channel -1, cap-PCB bonded, no capacitors assembled; Ibuf current maximized; ADC power supply with 1 μH series inductor. Parameter=no. of active ADCs

4.6.2 Optimized test pulse and ADC delay

ASIC configuration: JC configuration (tables 1 & 2) + test pulse and ADC delay optimizations (table 3).

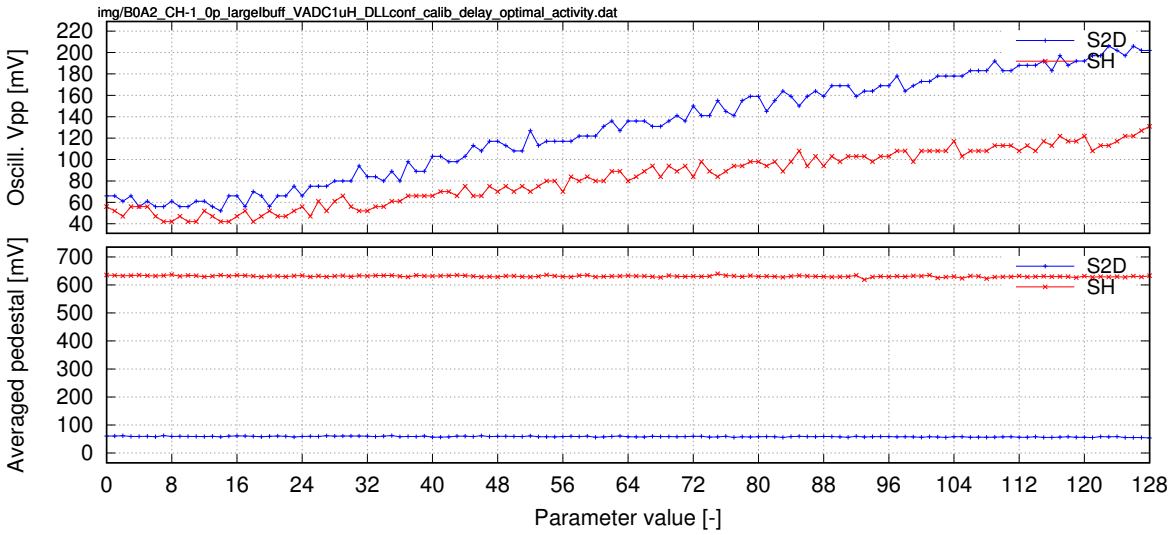

Figure 55: B0A2, channel -1, cap-PCB bonded, no capacitors assembled; Ibuf current maximized; ADC power supply with 1 μH series inductor. Optimized test pulse and ADC delay. Parameter=no. of active ADCs

4.7 Cap-PCB bonded, no capacitors assembled; Ibuf current maximized; ADC power supply with 1 μH series inductor; floating copper foil on ASIC

Cap-PCB assembled, bonded to SALT input pads 0 and 127, no capacitors assembled to the cap-PCB.
Ibuf current maximized – 1 kΩ resistor between VDDA and Ibuf pad.
1 μH inductor assembled in series between onboard decoupling power supply capacitors and VDDADC + VREFD bonds.
Floating copper foil glued directly on passivation on top of the ASIC (see figure 149).
Channel 128 have damaged input.

4.7.1 Default ASIC configuration

ASIC configuration: JC configuration (tables 1 & 2).

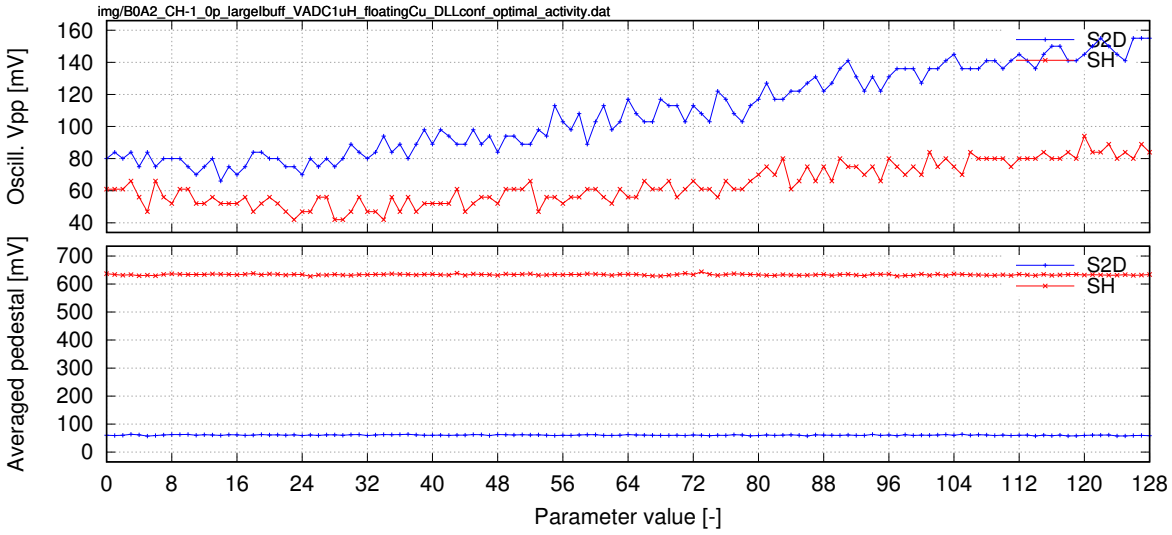

Figure 56: B0A2, channel -1, cap-PCB bonded, no capacitors assembled; Ibuf current maximized; ADC power supply with 1 μH series inductor; floating copper foil on ASIC. Parameter=no. of active ADCs

4.7.2 Optimized test pulse and ADC delay

ASIC configuration: JC configuration (tables 1 & 2) + test pulse and ADC delay optimizations (table 3).

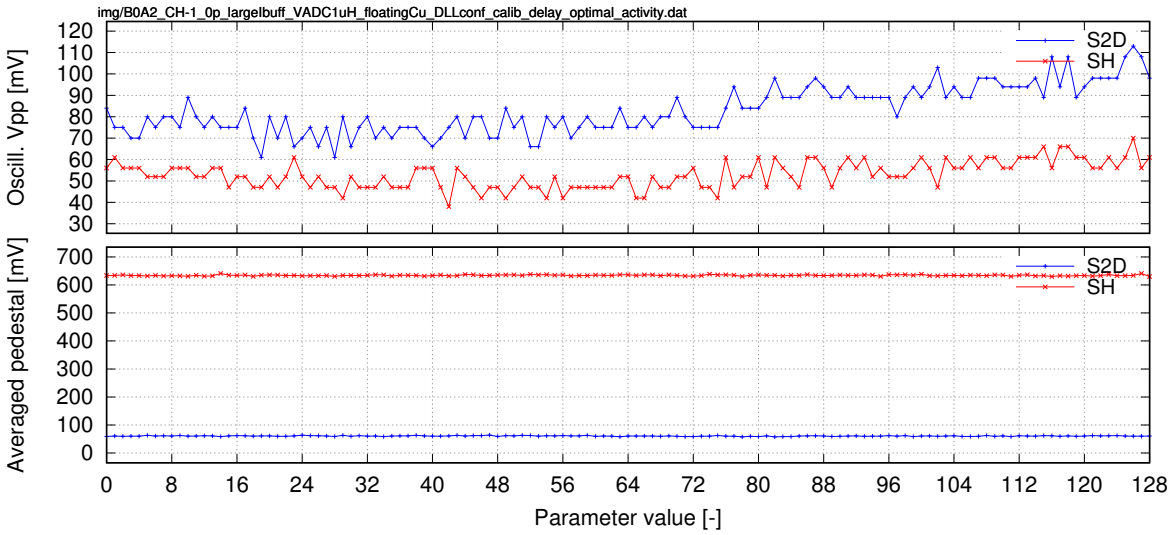

Figure 57: B0A2, channel -1, cap-PCB bonded, no capacitors assembled; Ibuf current maximized; ADC power supply with 1 μH series inductor; floating copper foil on ASIC. Optimized test pulse and ADC delay. Parameter=no. of active ADCs

4.8 Cap-PCB bonded, 12 pF capacitors assembled; Ibuf current maximized; ADC power supply with 1 μH series inductor; floating copper foil on ASIC

Cap-PCB assembled, bonded to SALT input pads 0 and 127, no capacitors assembled to the cap-PCB.
Ibuf current maximized – 1 kΩ resistor between VDDA and Ibuf pad.
1 μH inductor assembled in series between onboard decoupling power supply capacitors and VDDADC + VREFD bonds.
Floating copper foil glued directly on passivation on top of the ASIC (see figure 149).
Channel 128 have damaged input.

4.8.1 Default ASIC configuration

ASIC configuration: JC configuration (tables 1 & 2).

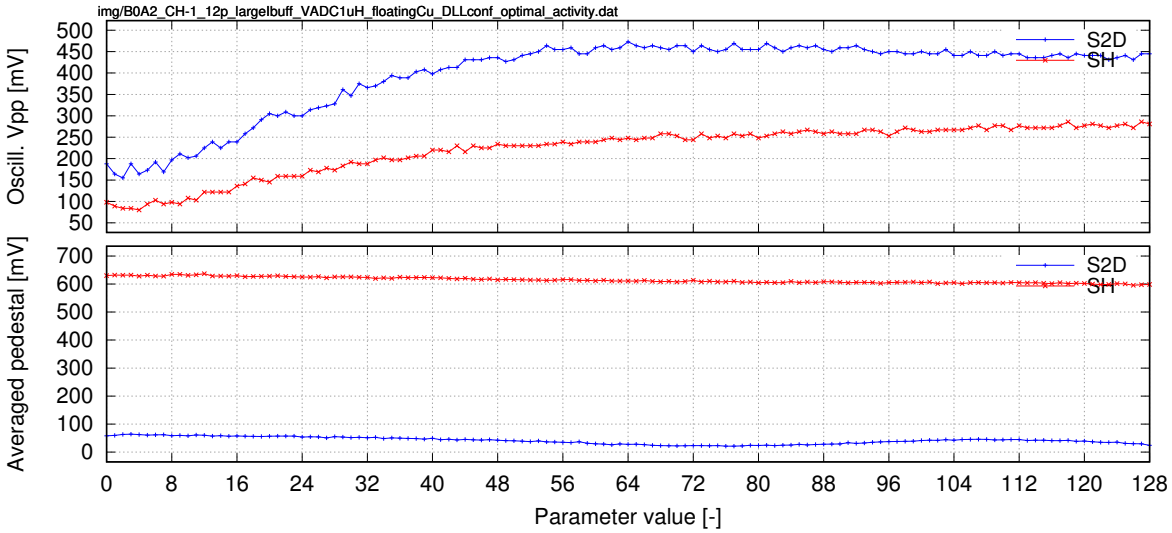

Figure 58: B0A2, channel -1, cap-PCB bonded, 12 pF capacitors assembled; Ibuf current maximized; ADC power supply with 1 μH series inductor; floating copper foil on ASIC. Parameter=no. of active ADCs

4.8.2 Optimized test pulse and ADC delay

ASIC configuration: JC configuration (tables 1 & 2) + test pulse and ADC delay optimizations (table 3).

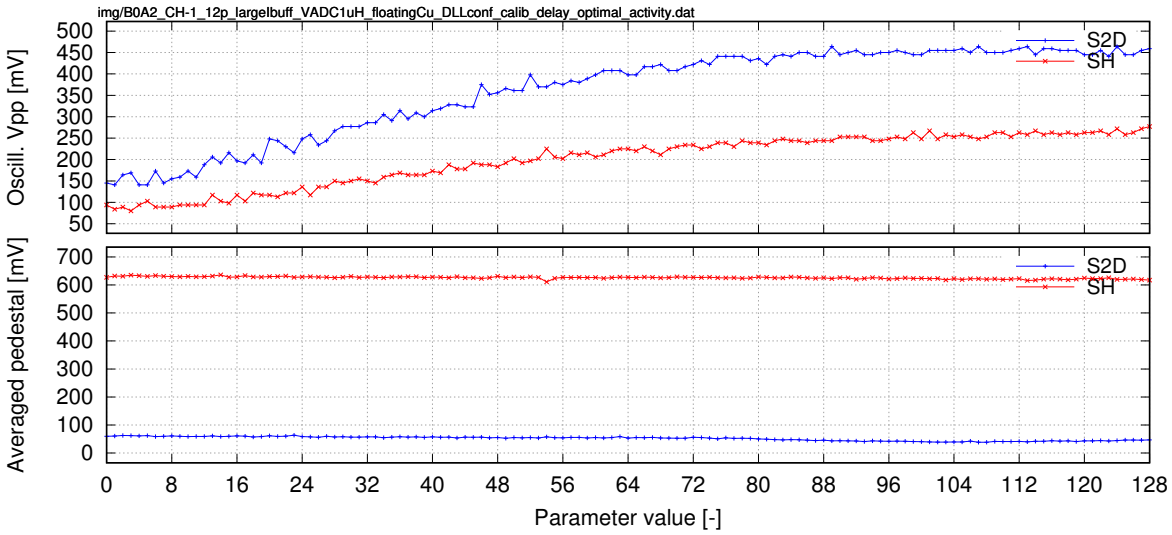

Figure 59: B0A2, channel -1, cap-PCB bonded, 12 pF capacitors assembled; Ibuf current maximized; ADC power supply with 1 μH series inductor; floating copper foil on ASIC. Optimized test pulse and ADC delay. Parameter=no. of active ADCs

4.9 Cap-PCB bonded, 12 pF capacitors assembled; Ibuf current maximized; ADC power supply with 1 μH series inductor; floating copper foil on ASIC; Preamp GND configuration – input + backside

Cap-PCB assembled, bonded to SALT input pads 0 and 127, 12 pF capacitors assembled to the cap-PCB.
Ibuf current maximized – 1 kΩ resistor between VDDA and Ibuf pad.
1 μH inductor assembled in series between onboard decoupling power supply capacitors and VDDADC + VREFD bonds.
Floating copper foil glued directly on passivation on top of the ASIC (see figure 149).
Preamp GND bonded from both sides - input pads + backside (default) pads.
Channel 128 have damaged input.

4.9.1 Default ASIC configuration

ASIC configuration: JC configuration (tables 1 & 2).

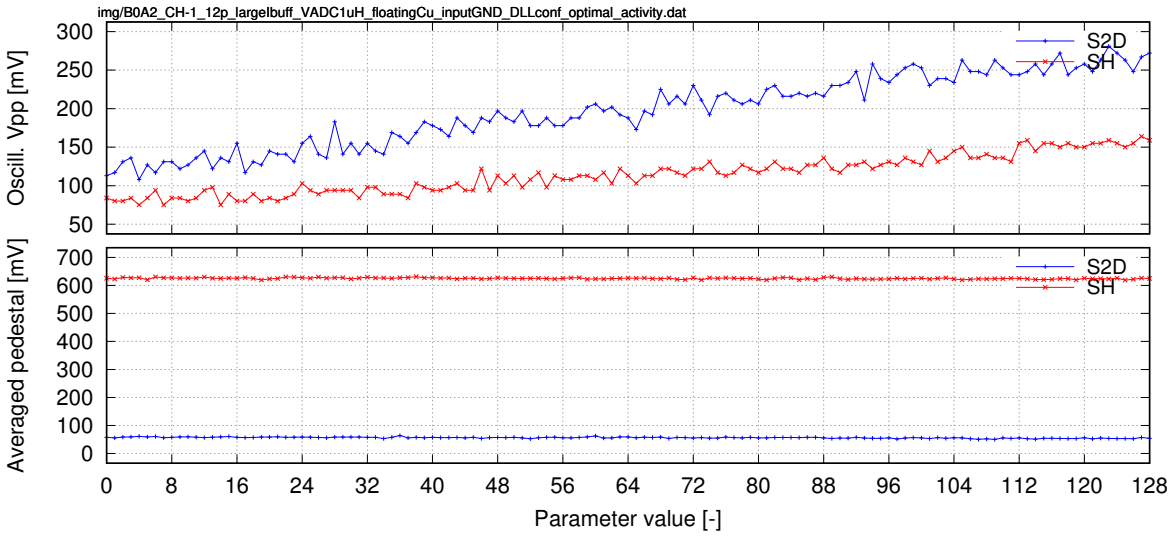

Figure 60: B0A2, channel -1, cap-PCB bonded, 12 pF capacitors assembled; Ibuf current maximized; ADC power supply with 1 μH series inductor; floating copper foil on ASIC; Preamp GND configuration – input + backside. Parameter=no. of active ADCs

4.9.2 Optimized test pulse and ADC delay

ASIC configuration: JC configuration (tables 1 & 2) + test pulse and ADC delay optimizations (table 3).

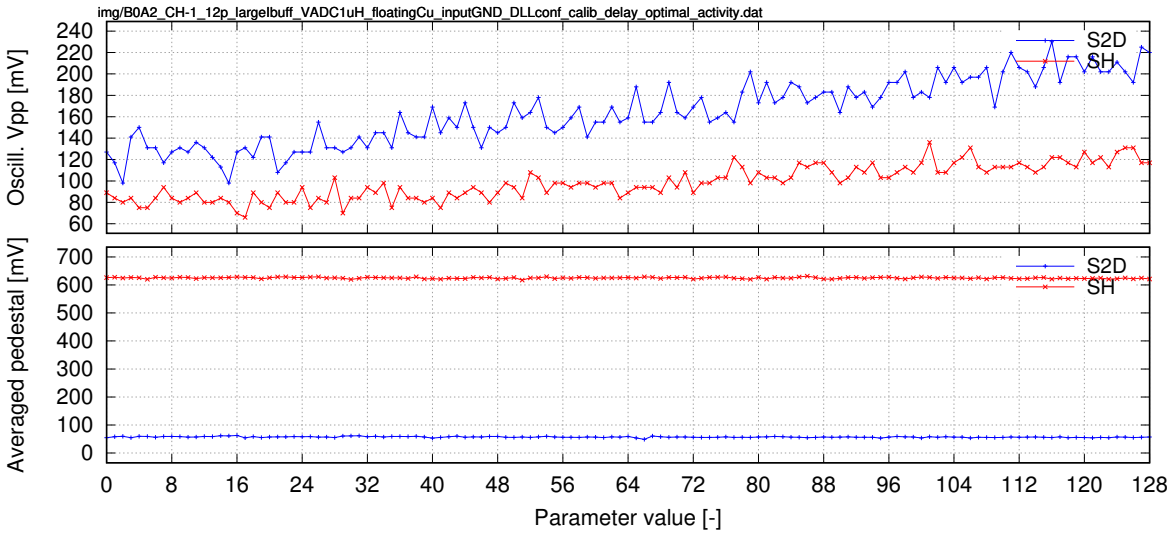

Figure 61: B0A2, channel -1, cap-PCB bonded, 12 pF capacitors assembled; Ibuf current maximized; ADC power supply with 1 μH series inductor; floating copper foil on ASIC; Preamp GND configuration – input + backside. Optimized test pulse and ADC delay. Parameter=no. of active ADCs

4.10 Cap-PCB bonded, 12 pF capacitors assembled; Ibuf current maximized; ADC power supply with 1 μH series inductor; grounded copper foil on ASIC; Preamp GND configuration – input + backside

Cap-PCB assembled, bonded to SALT input pads 0 and 127, no capacitors assembled to the cap-PCB.
Ibuf current maximized – 1 kΩ resistor between VDDA and Ibuf pad.
1 μH inductor assembled in series between onboard decoupling power supply capacitors and VDDADC + VREFD bonds.
Grounded copper foil glued directly on passivation on top of the ASIC.
Preamp GND bonded from both sides - input pads + backside (default) pads.
Channel 128 have damaged input.

4.10.1 Default ASIC configuration

ASIC configuration: JC configuration (tables 1 & 2).

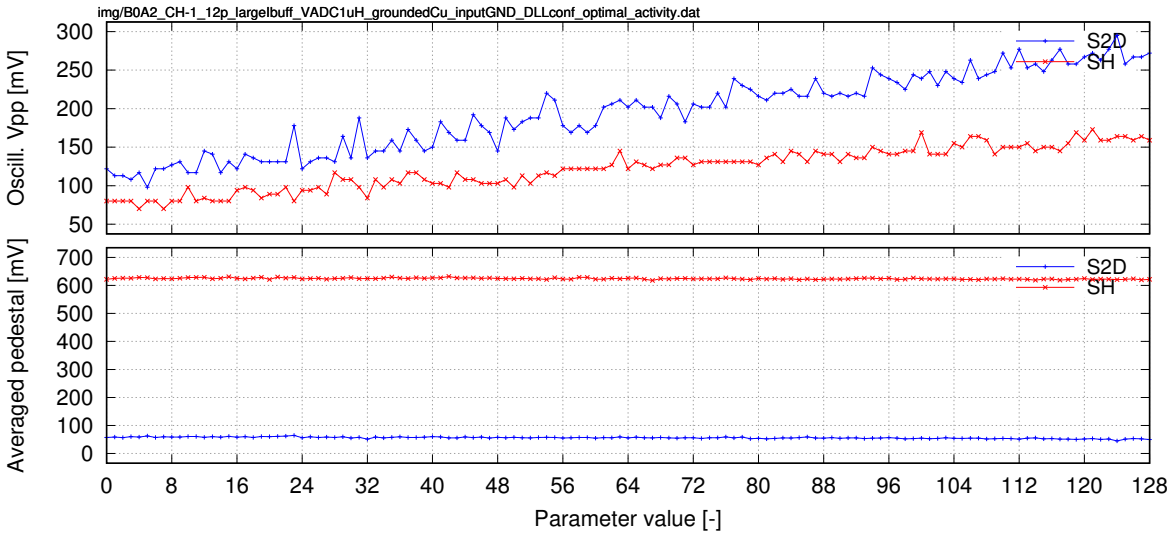

Figure 62: B0A2, channel -1, cap-PCB bonded, 12 pF capacitors assembled; Ibuf current maximized; ADC power supply with 1 μH series inductor; grounded copper foil on ASIC; Preamp GND configuration – input + backside. Parameter=no. of active ADCs

4.10.2 Optimized test pulse and ADC delay

ASIC configuration: JC configuration (tables 1 & 2) + test pulse and ADC delay optimizations (table 3).

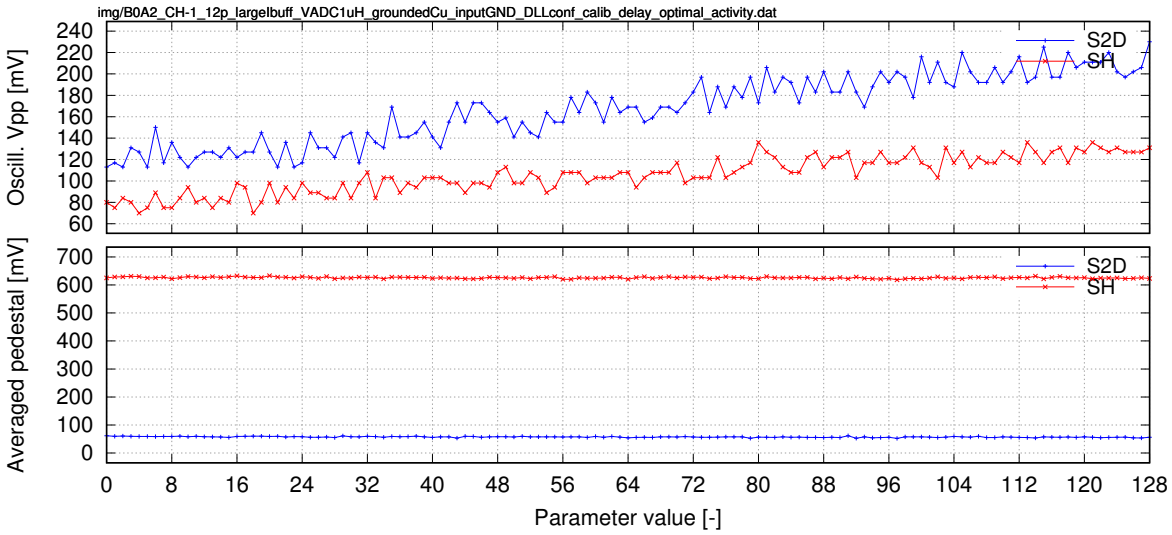

Figure 63: B0A2, channel -1, cap-PCB bonded, 12 pF capacitors assembled; Ibuf current maximized; ADC power supply with 1 μH series inductor; grounded copper foil on ASIC; Preamp GND configuration – input + backside. Optimized test pulse and ADC delay. Parameter=no. of active ADCs

4.11 Cap-PCB bonded, 12 pF capacitors assembled; Ibuf current maximized; ALL power supply with 1 μH series inductor; grounded copper foil on ASIC; Preamp GND configuration – input + backside

Cap-PCB assembled, bonded to SALT input pads 0 and 127, no capacitors assembled to the cap-PCB.
Ibuf current maximized – 1 kΩ resistor between VDDA and Ibuf pad.
1 μH inductor assembled in series between onboard decoupling power supply capacitors and all VDD bonds.
Grounded copper foil glued directly on passivation on top of the ASIC.
Preamp GND bonded from both sides - input pads + backside (default) pads.
Channel 128 have damaged input.

4.11.1 Default ASIC configuration

ASIC configuration: JC configuration (tables 1 & 2).

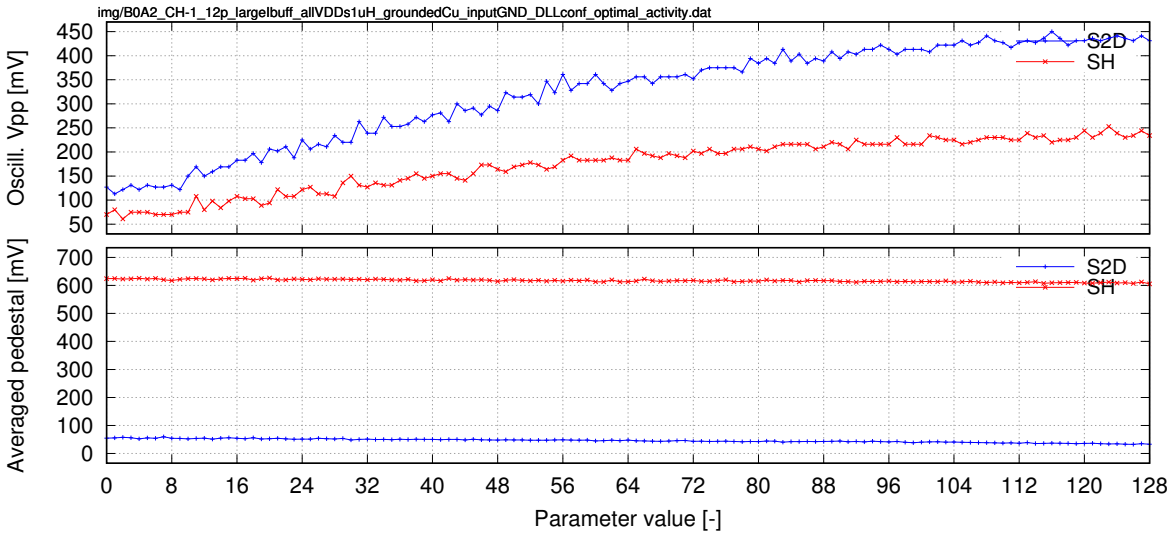

Figure 64: B0A2, channel -1, cap-PCB bonded, 12 pF capacitors assembled; Ibuf current maximized; ALL power supply with 1 μH series inductor; grounded copper foil on ASIC; Preamp GND configuration – input + backside. Parameter=no. of active ADCs

4.11.2 Optimized test pulse and ADC delay

ASIC configuration: JC configuration (tables 1 & 2) + test pulse and ADC delay optimizations (table 3).

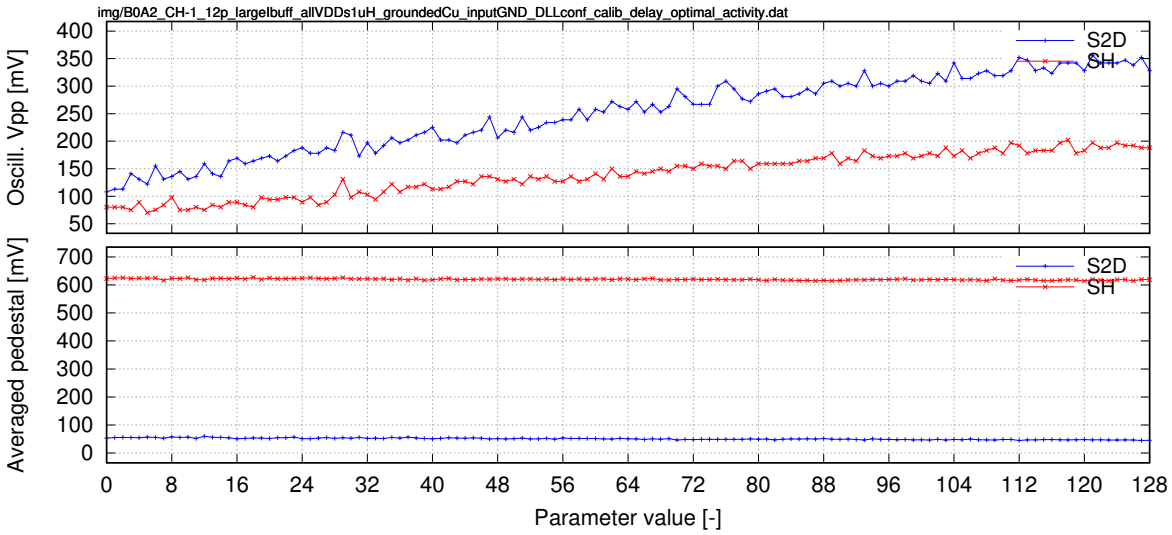

Figure 65: B0A2, channel -1, cap-PCB bonded, 12 pF capacitors assembled; Ibuf current maximized; ALL power supply with 1 μH series inductor; grounded copper foil on ASIC; Preamp GND configuration – input + backside. Optimized test pulse and ADC delay. Parameter=no. of active ADCs

4.11.3 ASIC response for EMI source

ASIC configuration: default (chip after reset), EMI source 152 1cm over the ASIC.

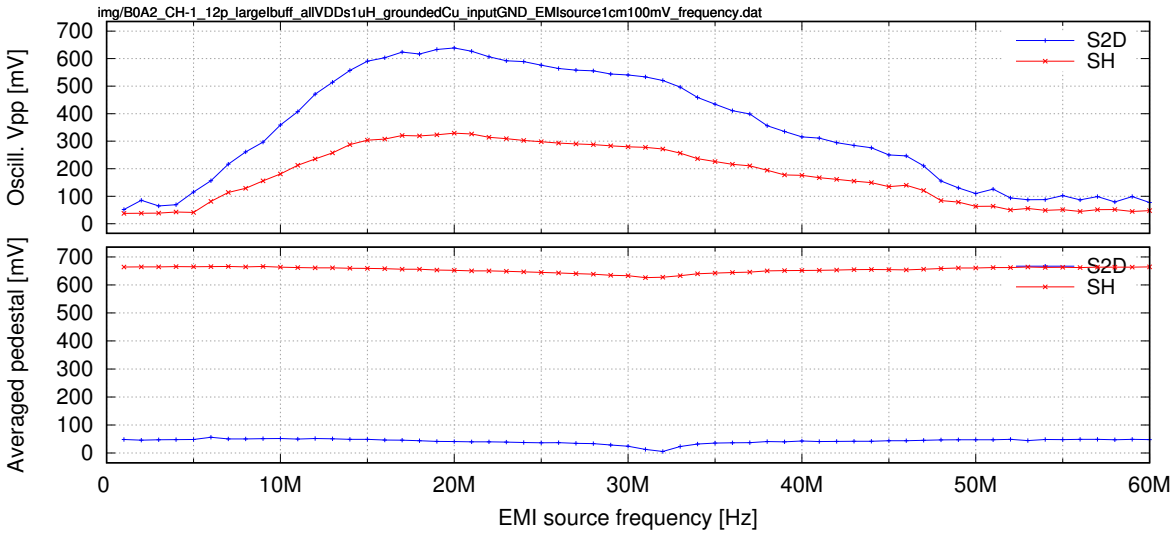

Figure 66: B0A2, channel -1, cap-PCB bonded, 12 pF capacitors assembled; Ibuf current maximized; ALL power supply with 1 μH series inductor; grounded copper foil on ASIC; Preamp GND configuration – input + backside. EMI source amplitude 100mV. Parameter=frequency of EMI source

4.12 Cap-PCB bonded, 12 pF capacitors assembled; Ibuf current maximized; ALL power supply with 1 μH series inductor; grounded copper foil on ASIC; Preamp GND configuration – only backside

Cap-PCB assembled, bonded to SALT input pads 0 and 127, no capacitors assembled to the cap-PCB.
Ibuf current maximized – 1 kΩ resistor between VDDA and Ibuf pad.
1 μH inductor assembled in series between onboard decoupling power supply capacitors and all VDD bonds.
Grounded copper foil glued directly on passivation on top of the ASIC.
Preamp GND bonded only from backside (default) pads.
Channel 128 have damaged input.

4.12.1 ASIC response for EMI source

ASIC configuration: default (chip after reset), EMI source 152 1cm over the ASIC.

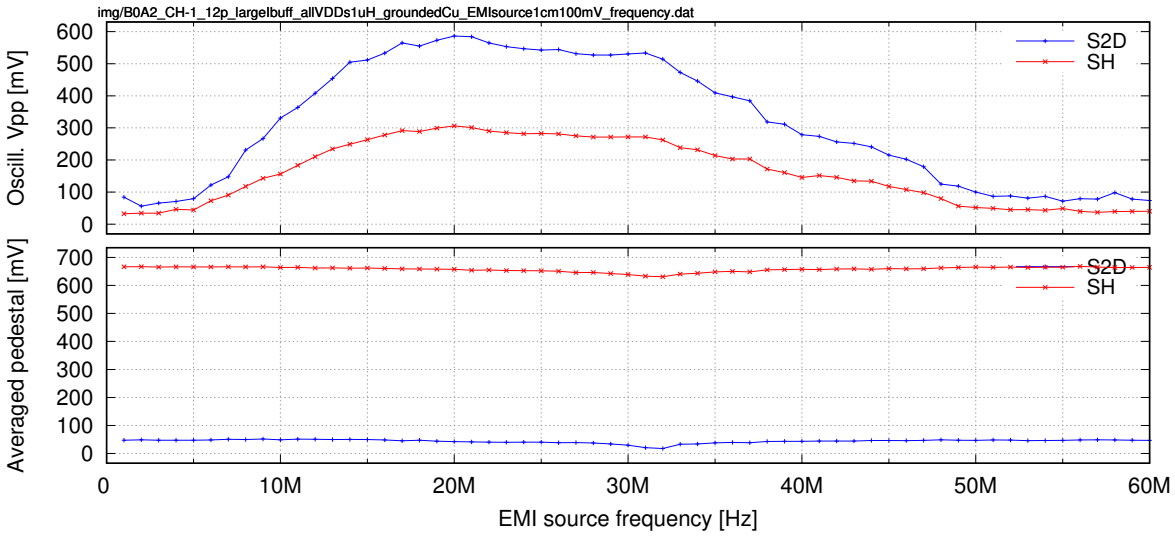

Figure 67: B0A2, channel -1, cap-PCB bonded, 12 pF capacitors assembled; Ibuf current maximized; ALL power supply with 1 μH series inductor; grounded copper foil on ASIC; Preamp GND configuration – only backside. EMI source amplitude 100mV. Parameter=frequency of EMI source

4.13 S2D response for different sampling frequencies

1 μH inductor assembled in series between onboard decoupling power supply capacitors and VDDADC + VREFD bonds.
Channel 128 S2D output shown (yellow trace) with sampling clock (purple trace). Scope triggered on sampling clock; averaging active.
ASIC configuration - default after reset.

4.13.1 Response at 1 MHz at full activity with 12 pF + 820 kΩ at input

Cap-PCB assembled, bonded to SALT input pads 0 and 127, two 12 pF capacitors assembled to the cap-PCB, 820 kΩ resistors soldered in parallel to the capacitors.

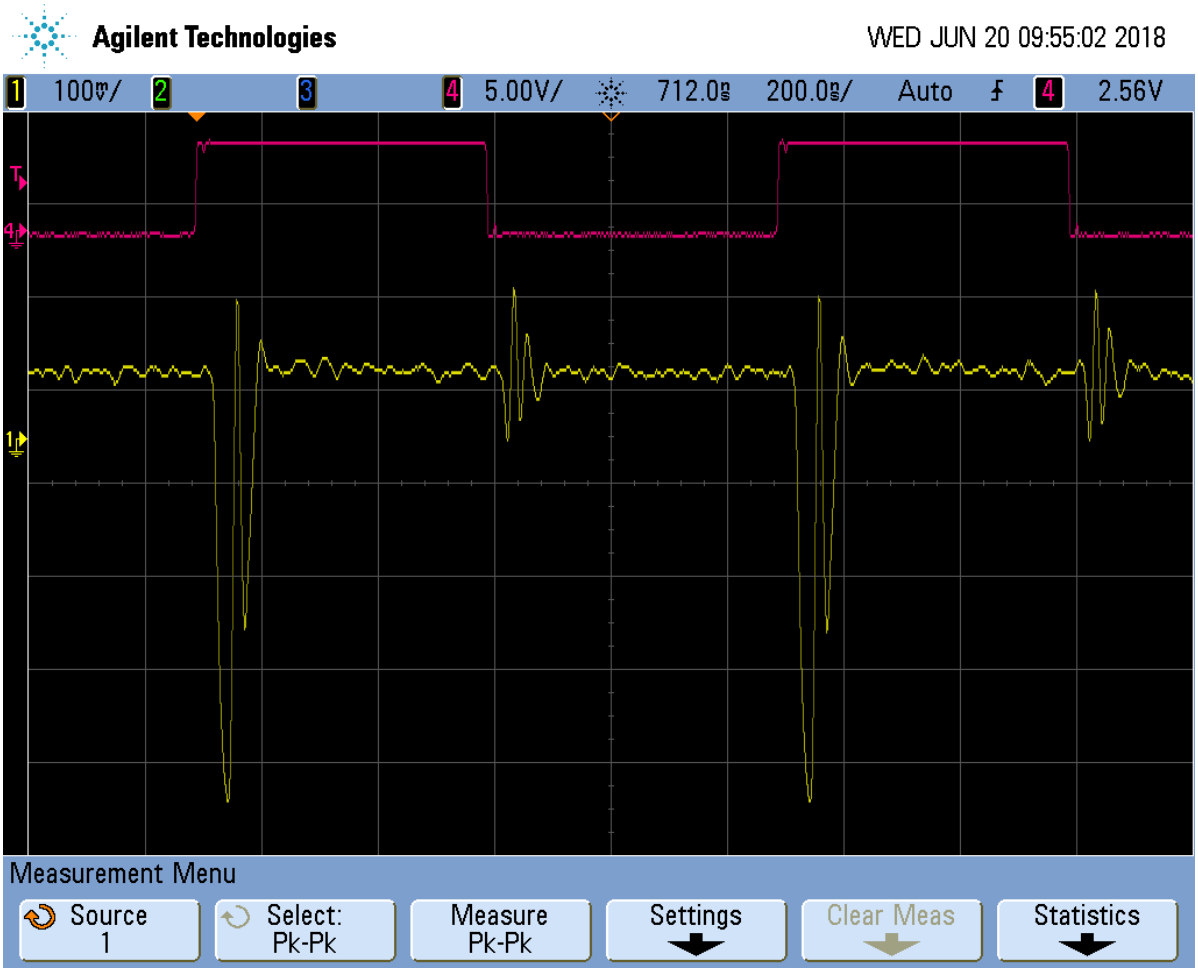

Figure 68: B0A2, S2D response at 1 MHz of main clock. Rising edge corresponds to the ADC conversion. 12 pF + 820 kΩ at input.

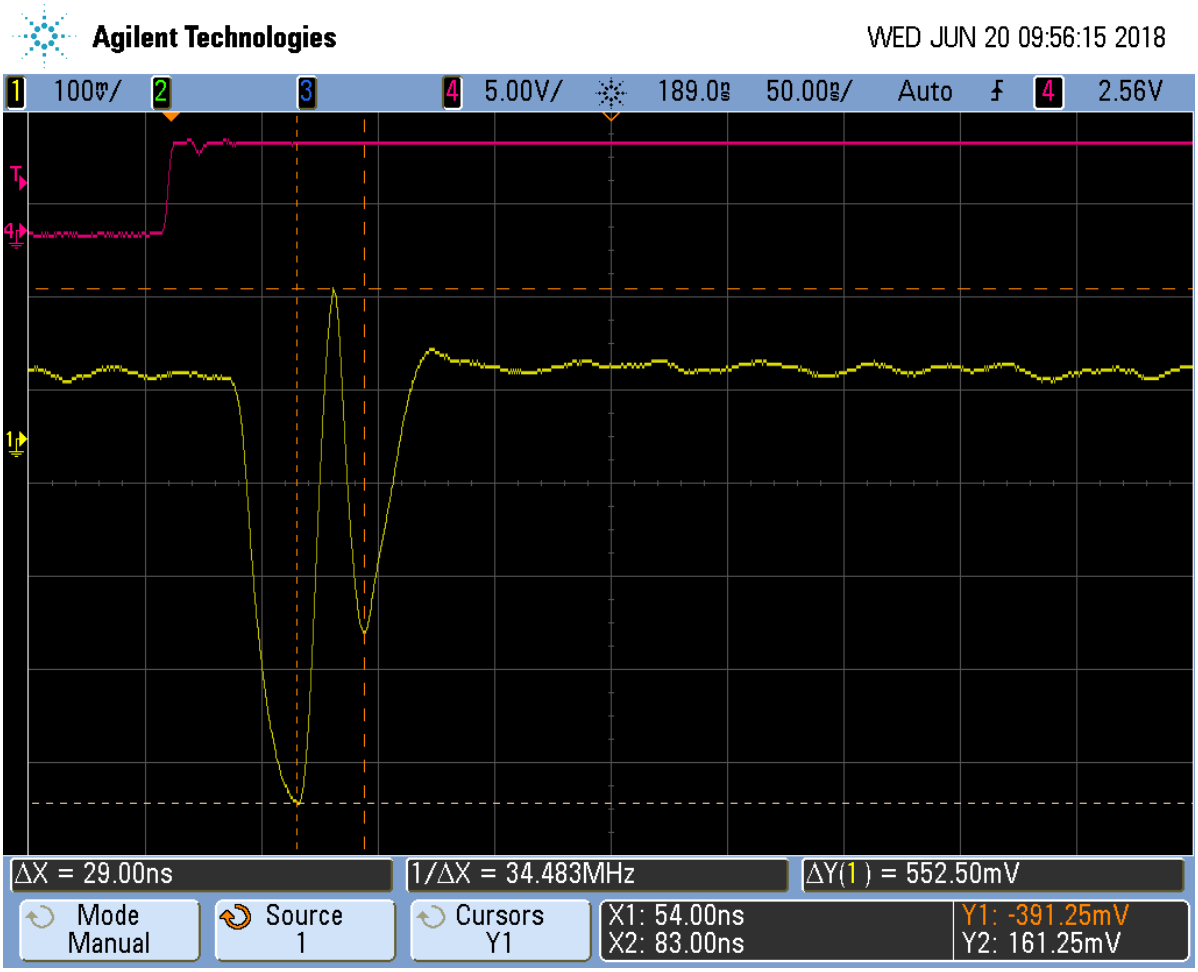

Figure 69: B0A2, Amplitude of S2D response at 1 MHz. 12 pF + 820 kΩ at input.

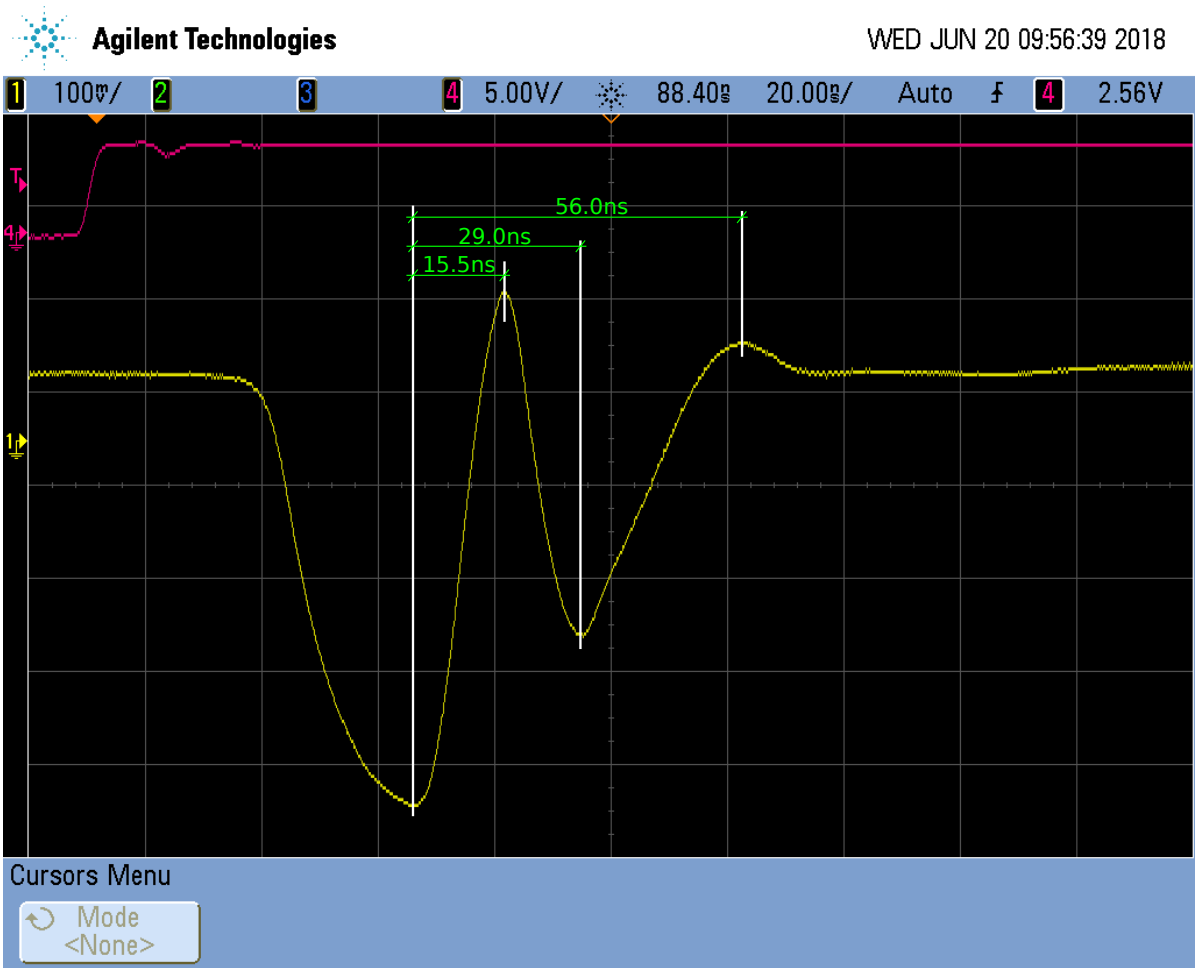

Figure 70: B0A2, Time structure of S2D response at 1 MHz. 12 pF + 820 kΩ at input.

4.13.2 Response at 1 MHz at full activity with 0 pF; floating copper foil on ASIC

Cap-PCB assembled, bonded to SALT input pads 0 and 127, no capacitors assembled to the cap-PCB.
Floating copper foil glued directly on passivation on top of the ASIC (see figure 149).

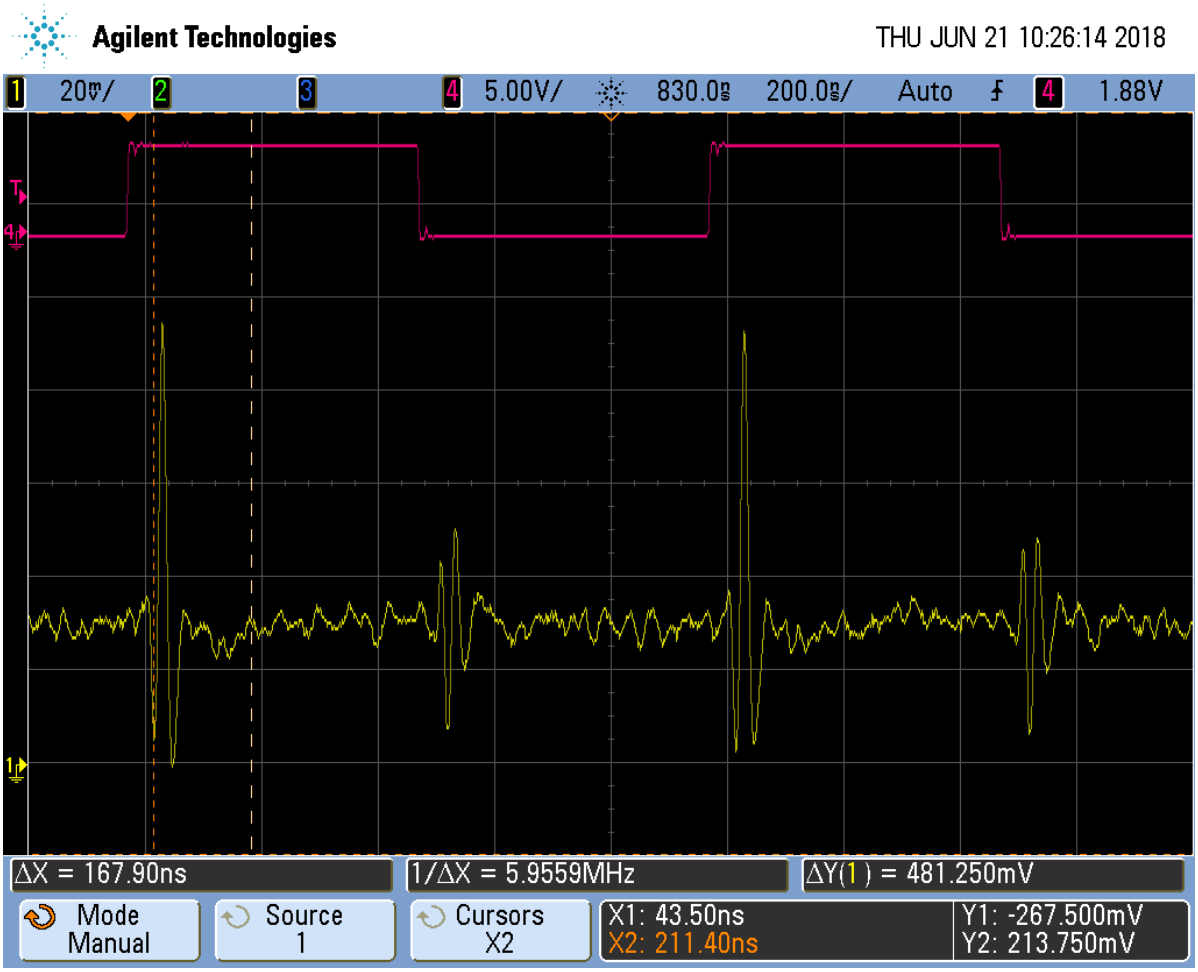

Figure 71: B0A2, S2D response at 1 MHz of main clock. Rising edge corresponds to the ADC conversion. 0 pF; floating plane on passivation.

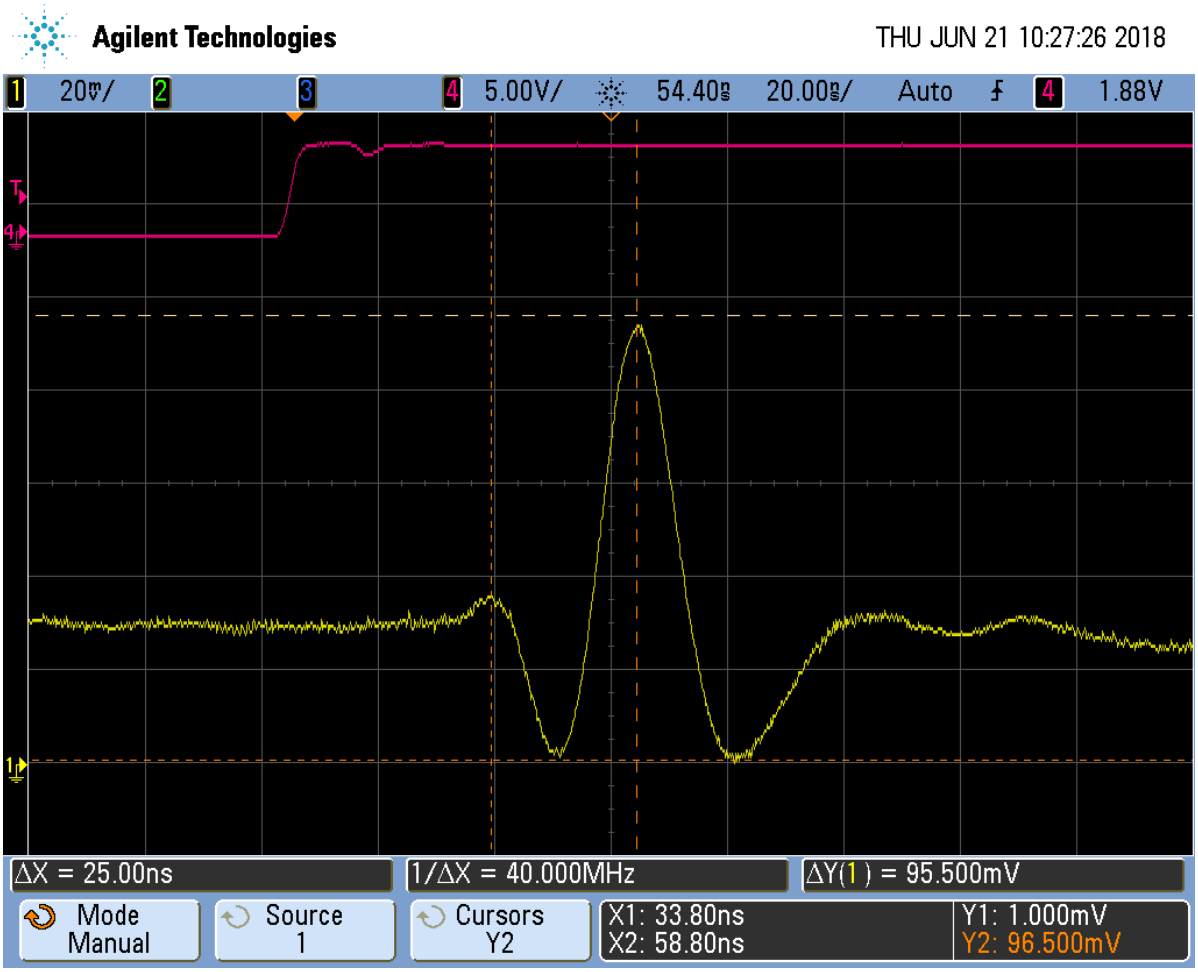

Figure 72: B0A2, Amplitude of S2D response at 1 MHz. 0 pF; floating plane on passivation.

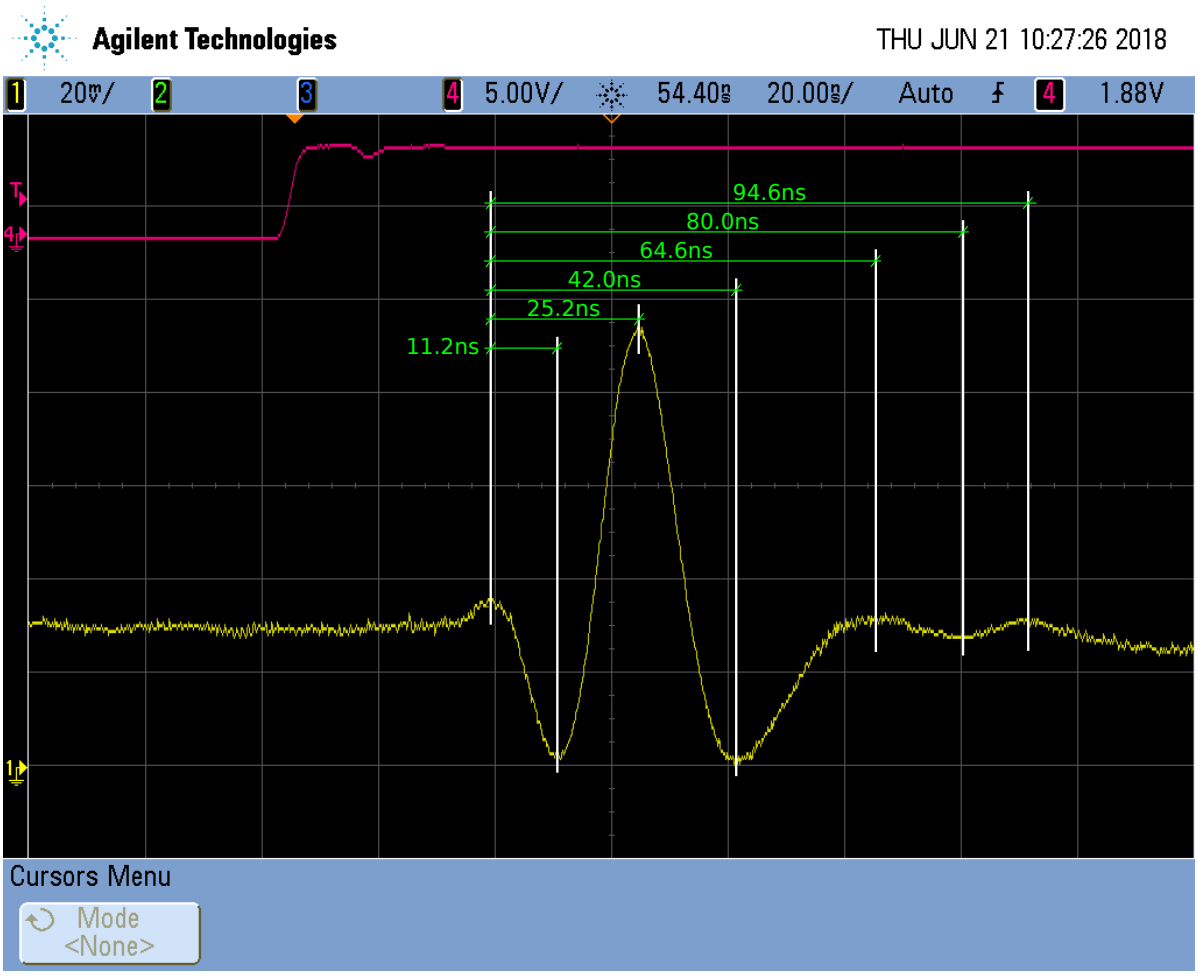

Figure 73: B0A2, Time structure of S2D response at 1 MHz. 0 pF; floating plane on passivation.

4.13.3 Response at 1 MHz at full activity with 12 pF; grounded copper foil on ASIC; Preamp GND configuration – input + backside.

Cap-PCB assembled, bonded to SALT input pads 0 and 127, two 12 pF capacitors assembled to the cap-PCB.
Grounded copper foil glued directly on passivation on top of the ASIC (see figure 149).
Preamp GND bonded from both sides - input pads + backside (default) pads.

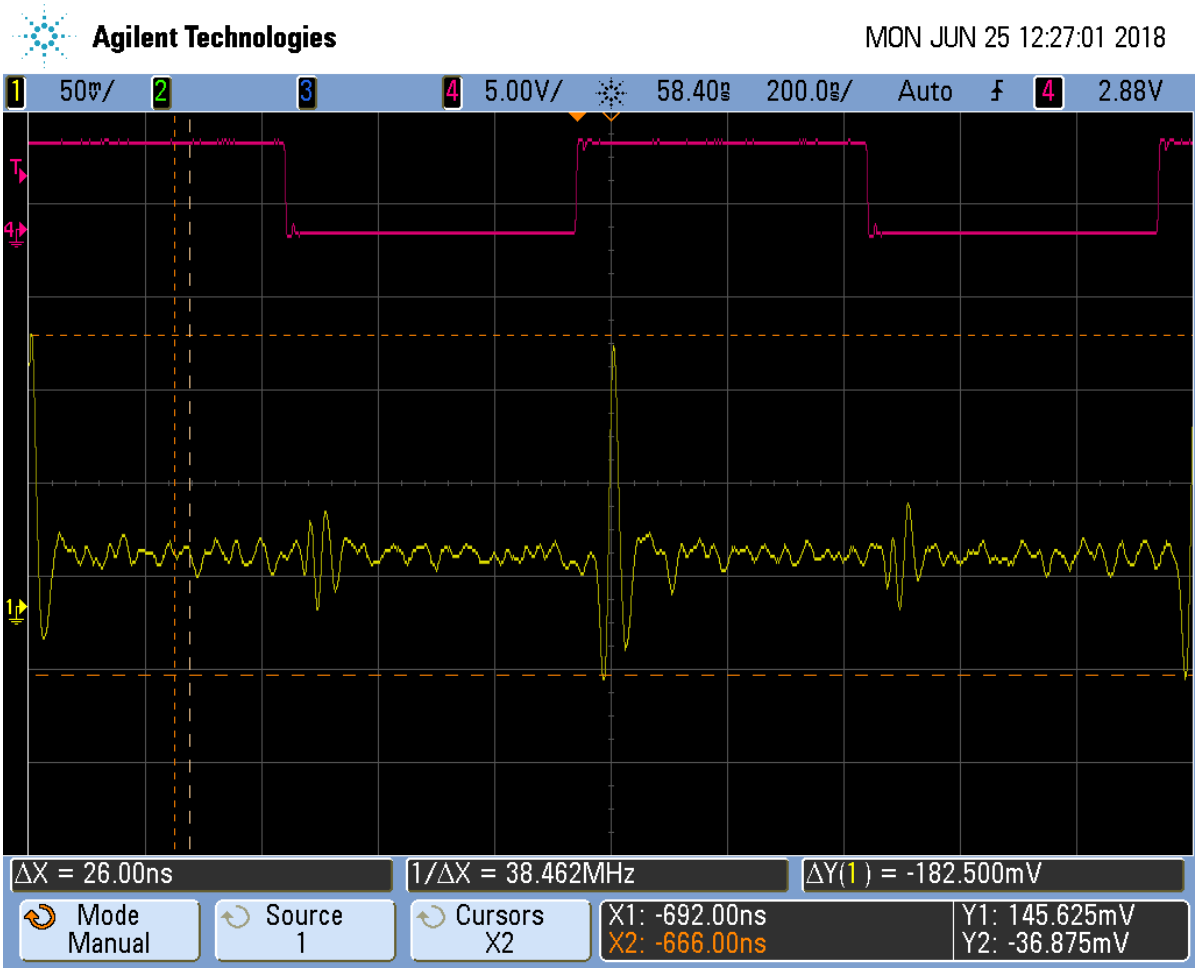

Figure 74: B0A2, S2D response at 1 MHz of main clock. Rising edge corresponds to the ADC conversion. 12 pF; grounded plane on passivation; Preamp GND configuration – input + backside.

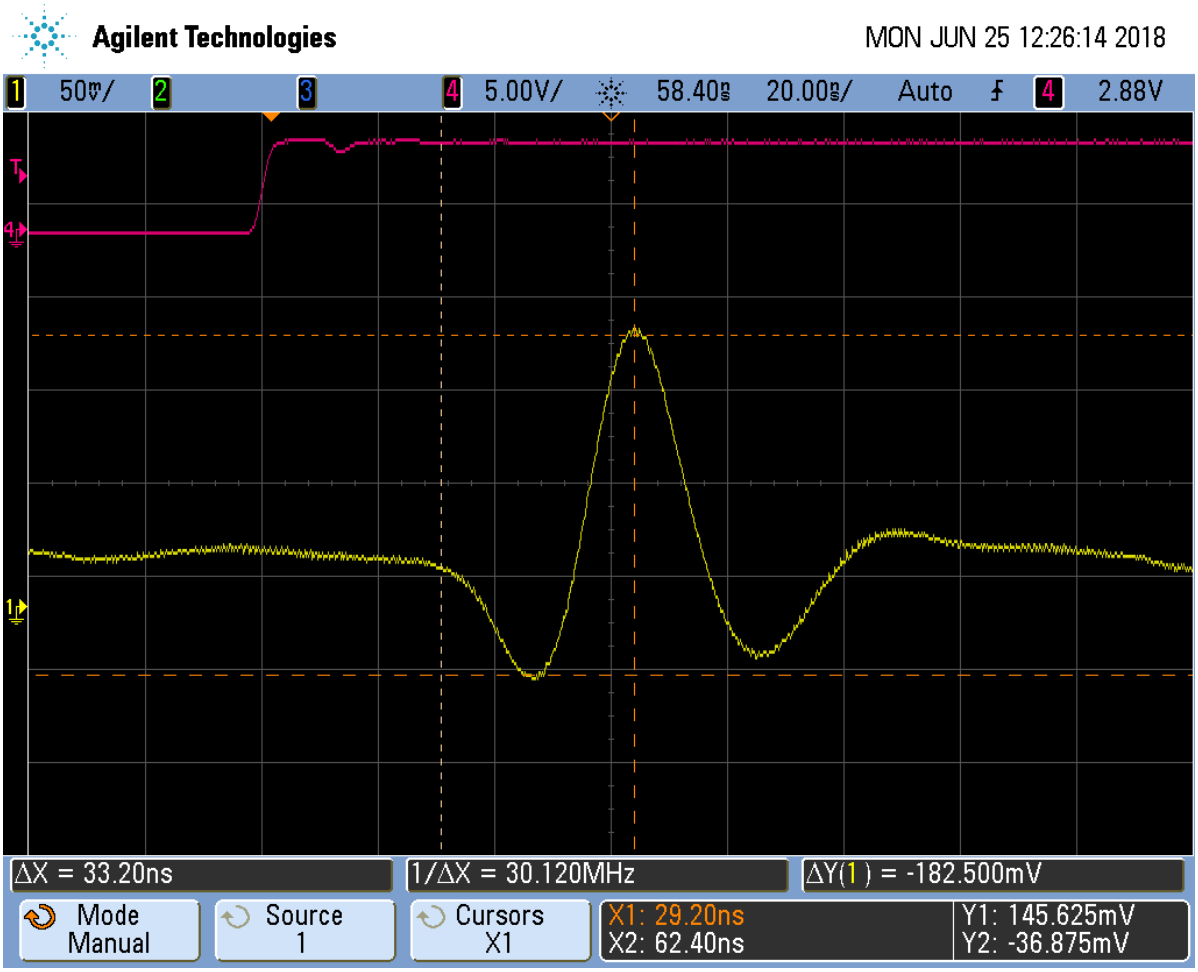

Figure 75: B0A2, Amplitude of S2D response at 1 MHz. 12 pF; grounded plane on passivation; Preamp GND configuration – input + backside.

5 Board 1 with ASIC 4

5.1 S2D response for different sampling frequencies

Channel 128 S2D output shown (yellow trace) with sampling clock (purple trace). Scope triggered on sampling clock; averaging active.
ASIC configuration - default after reset.

5.1.1 Response at 1 MHz at full activity without input pads bonded

Input pads not bonded.

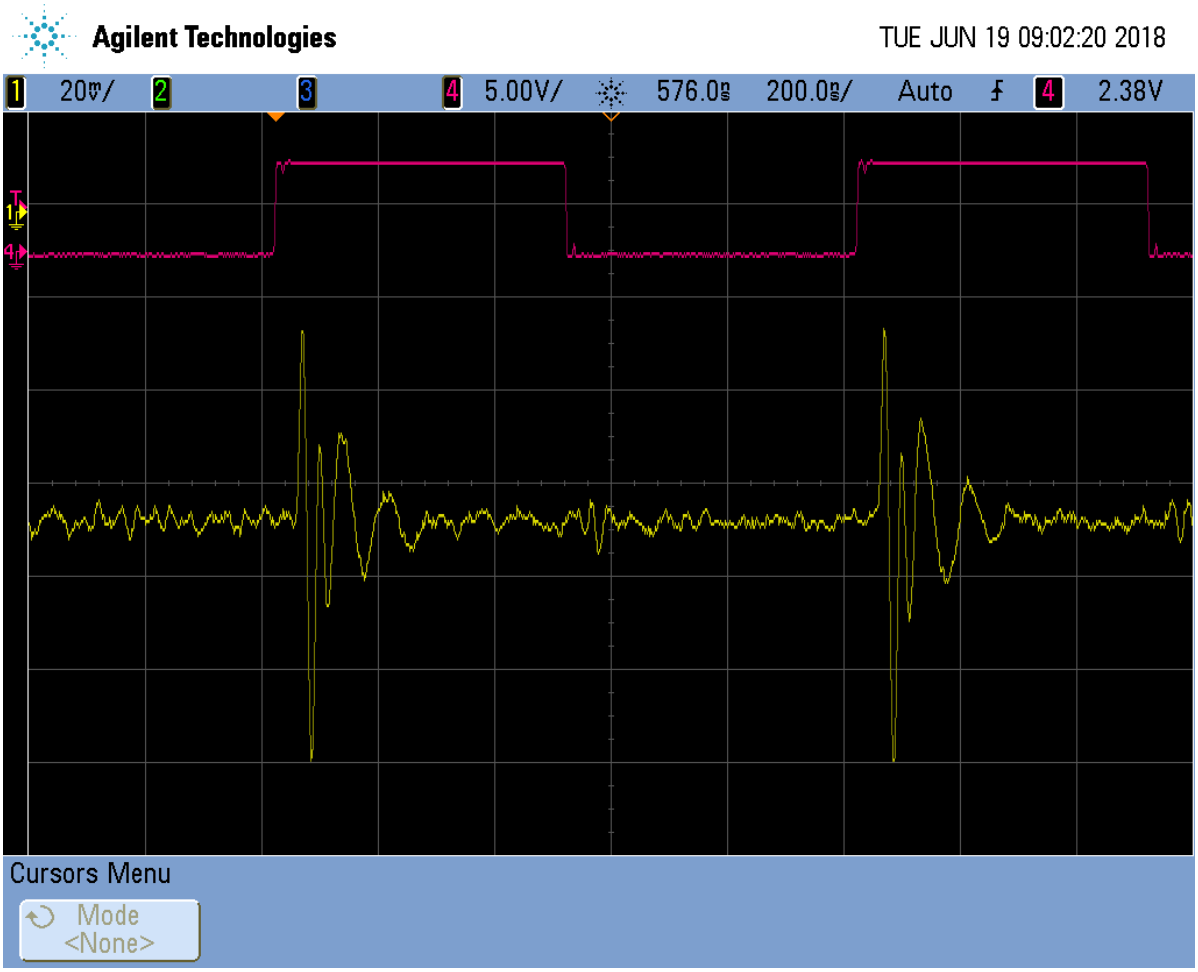

Figure 76: B1A4, S2D response at 1 MHz of main clock. Rising edge corresponds to the ADC conversion. Input pads not bonded.

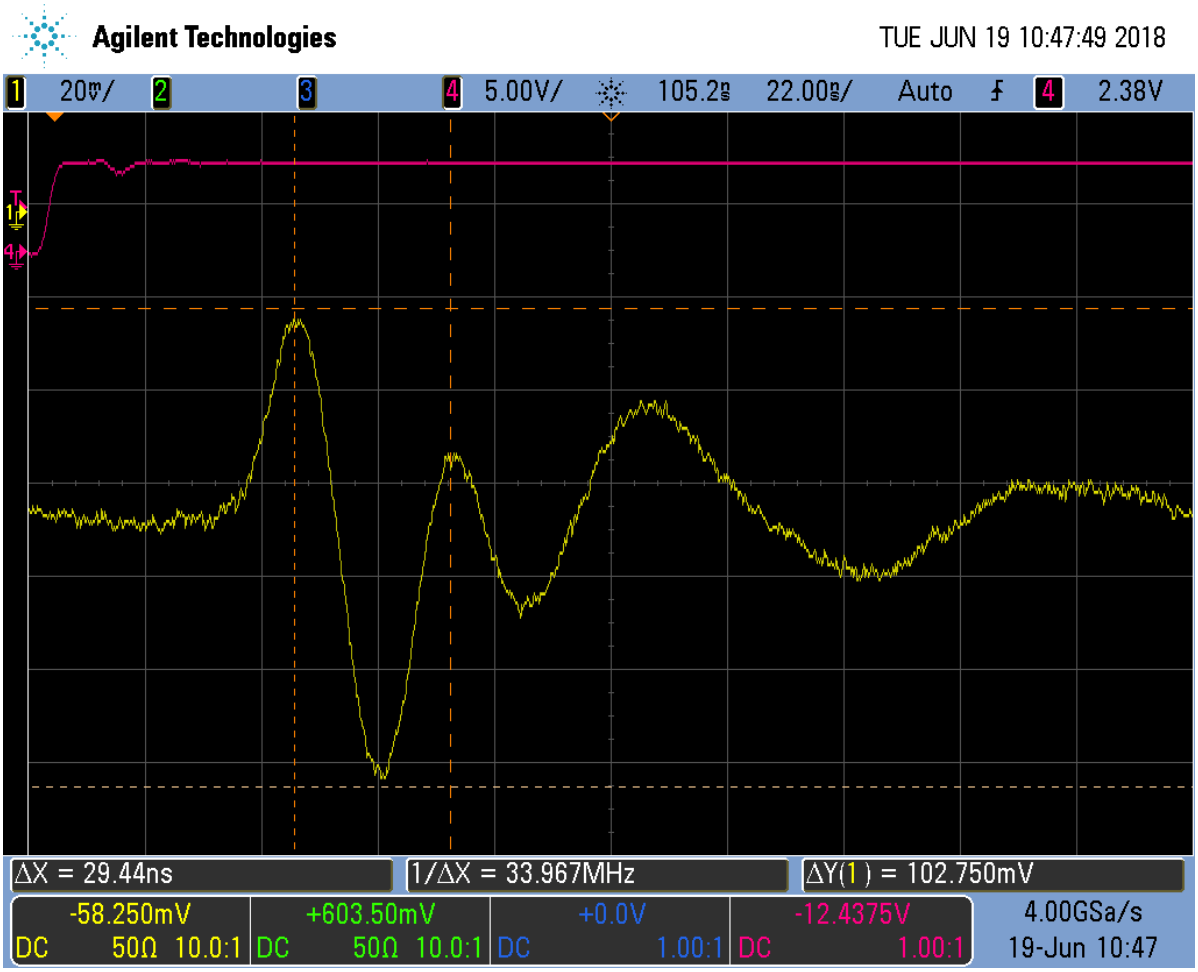

Figure 77: B1A4, Amplitude of S2D response at 1 MHz. Input pads not bonded.

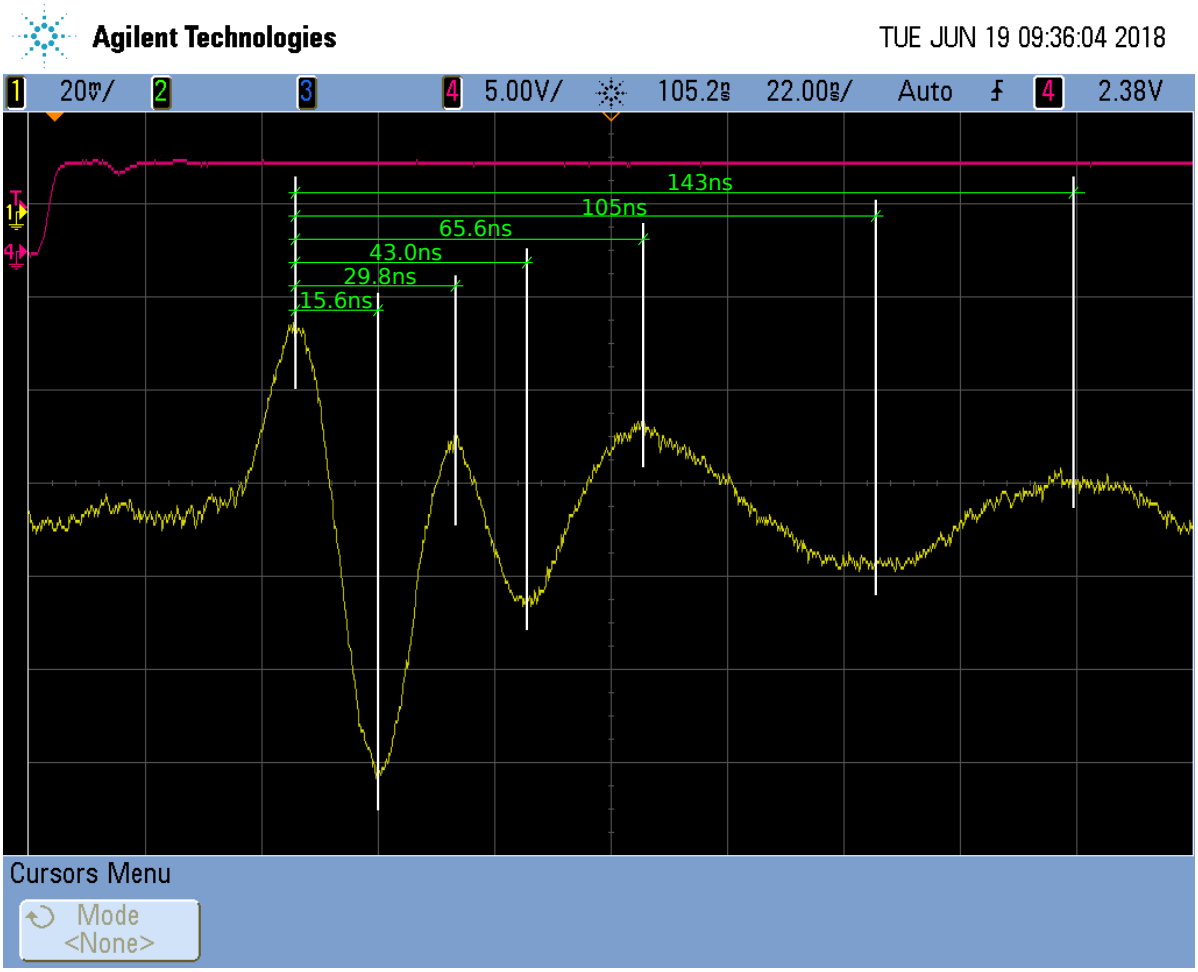

Figure 78: B1A4, Time structure of S2D response at 1 MHz. Input pads not bonded.

5.1.2 Response at 1 MHz at full activity with 12 pF at input

Cap-PCB assembled, bonded to SALT input pads 0 and 127, two 12 pF capacitors assembled to the cap-PCB.

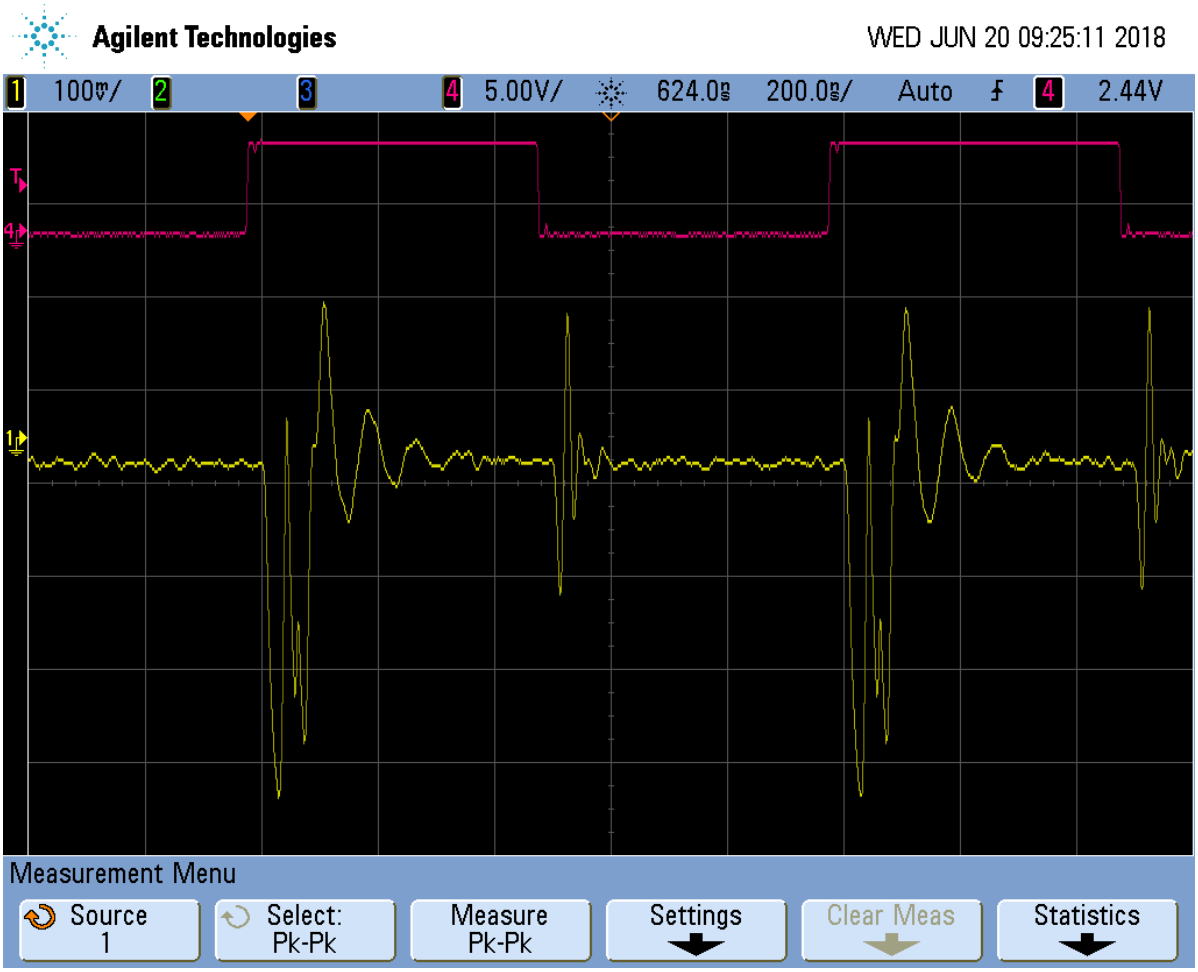

Figure 79: B1A4, S2D response at 1 MHz of main clock. Rising edge corresponds to the ADC conversion. 12 pF at inputs.

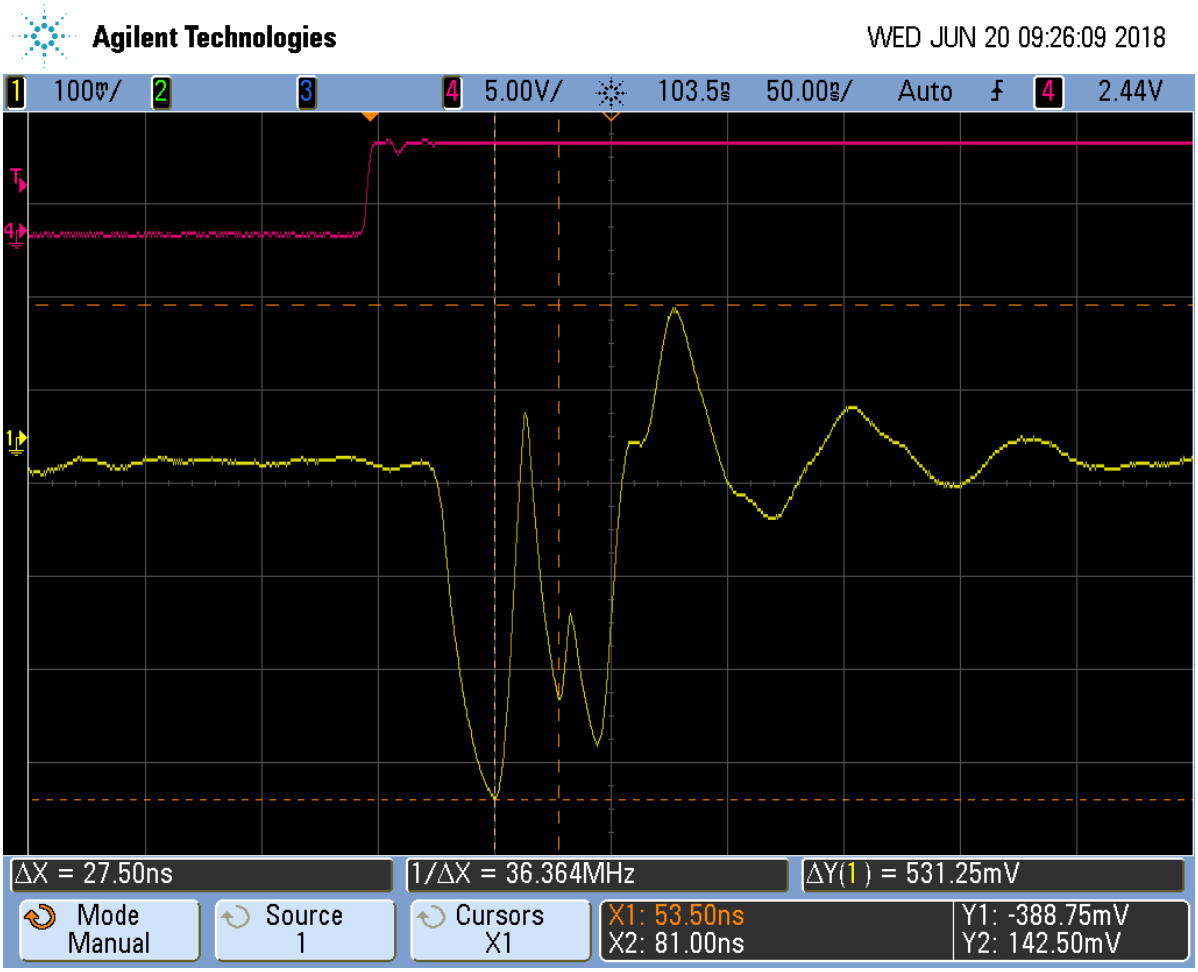

Figure 80: B1A4, Amplitude of S2D response at 1 MHz. 12 pF at inputs.

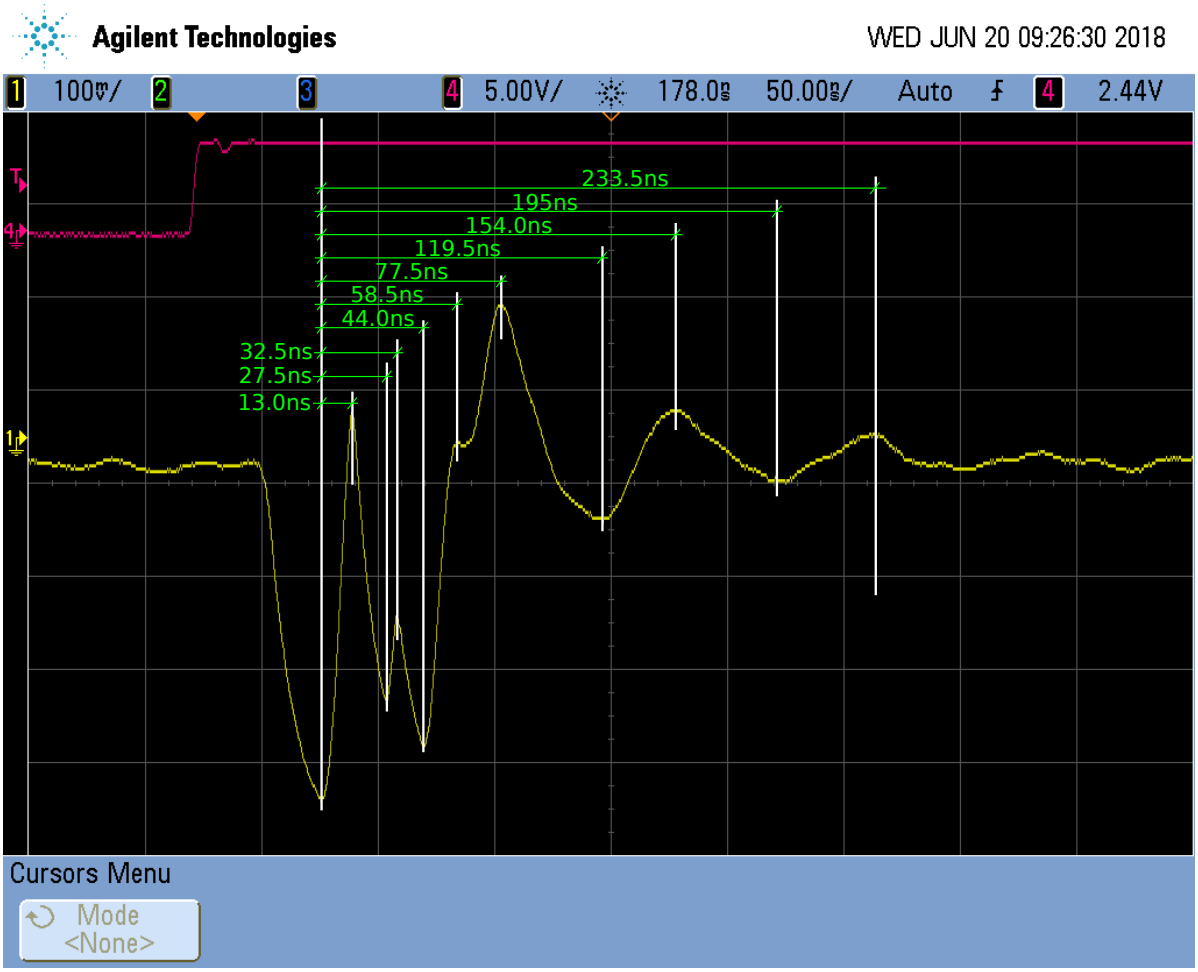

Figure 81: B1A4, Time structure of S2D response at 1 MHz. 12 pF at inputs.

5.1.3 Response at 1 MHz at full activity with 12 pF at input; preamp GND configuration – input + backside

Cap-PCB assembled, bonded to SALT input pads 0 and 127, two 12 pF capacitors assembled to the cap-PCB.
Preamp GND configuration – input + backside

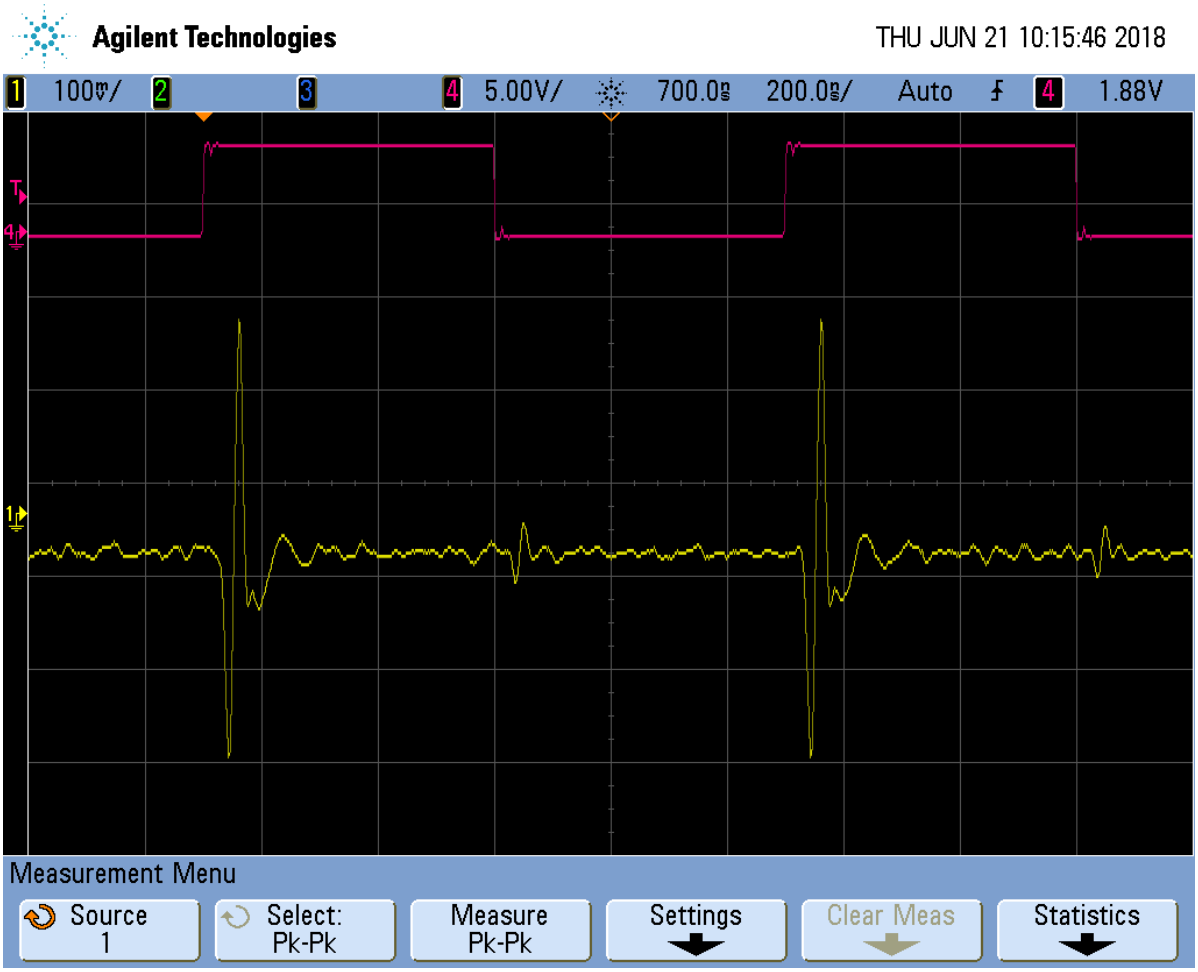

Figure 82: B1A4, S2D response at 1 MHz of main clock. Rising edge corresponds to the ADC conversion. 12 pF at inputs. Preamp GND – input + backside

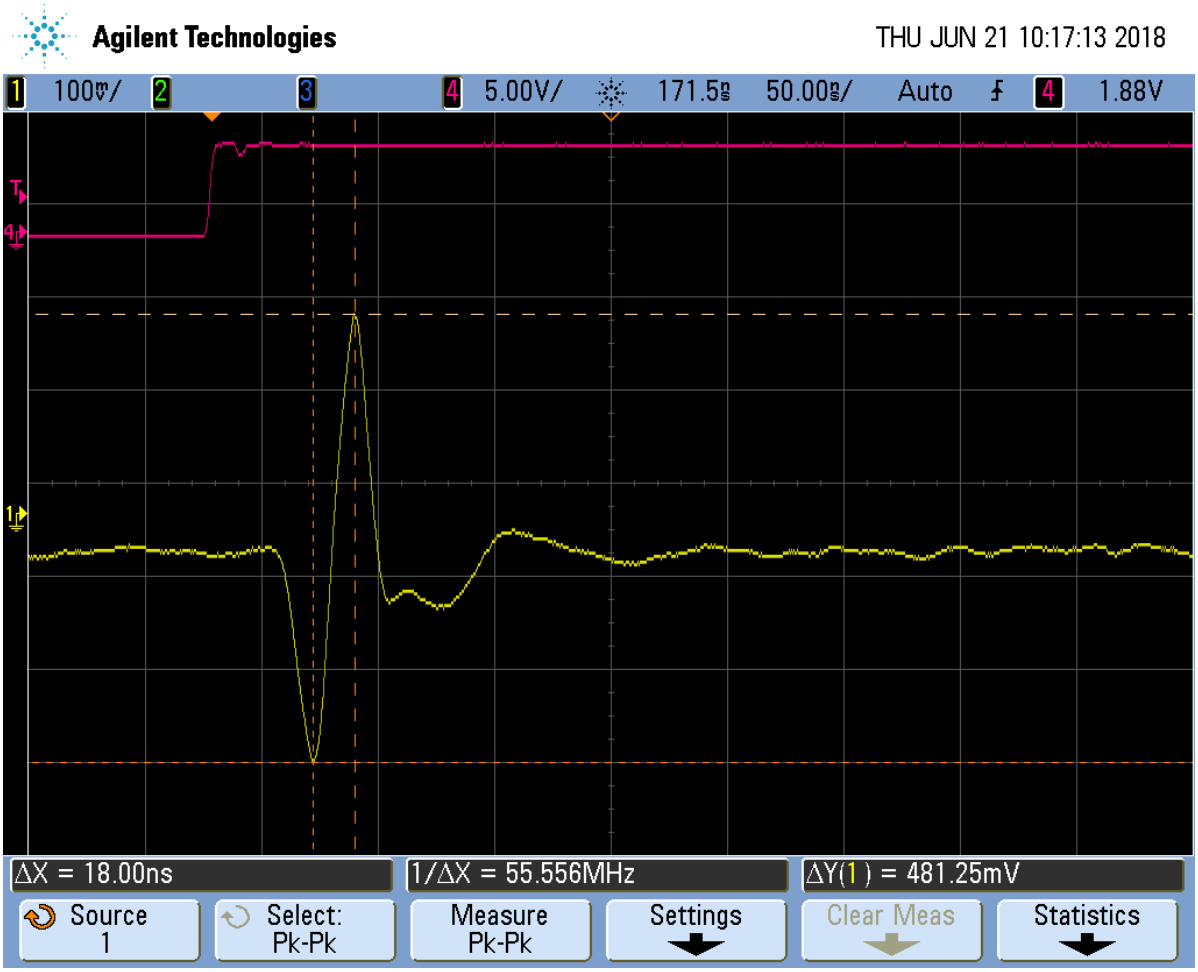

Figure 83: B1A4, Amplitude of S2D response at 1 MHz. 12 pF at inputs. Preamp GND – input + backside

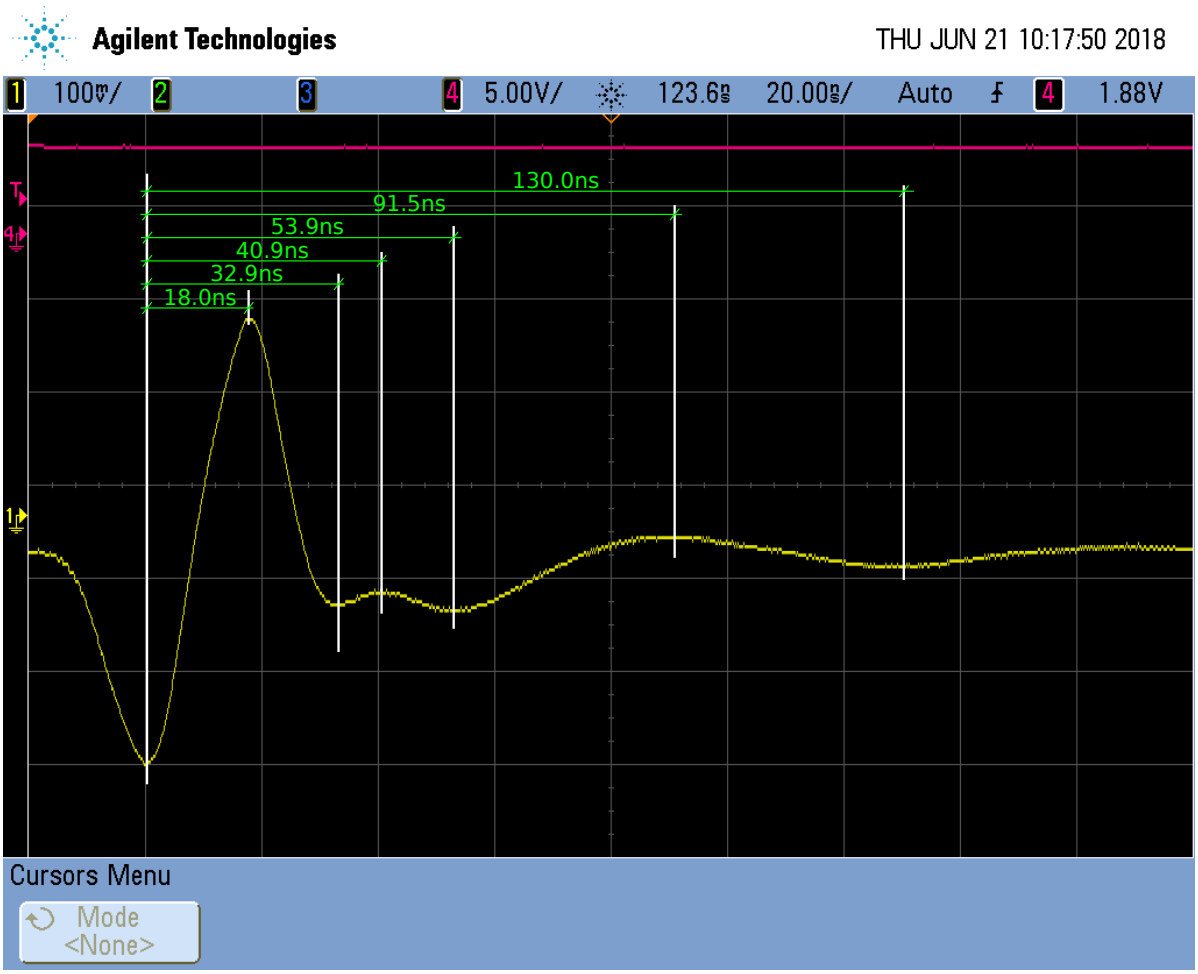

Figure 84: B1A4, Time structure of S2D response at 1 MHz. 12 pF at inputs. Preamp GND – input + backside

5.1.4 Response vs main clock frequency without input pads bonded

5.1.5 Response at 1 MHz vs activity without input pads bonded

5.2 Before input pads bonded

5.2.1 Default ASIC configuration

ASIC configuration: JC configuration (tables 1 & 2).

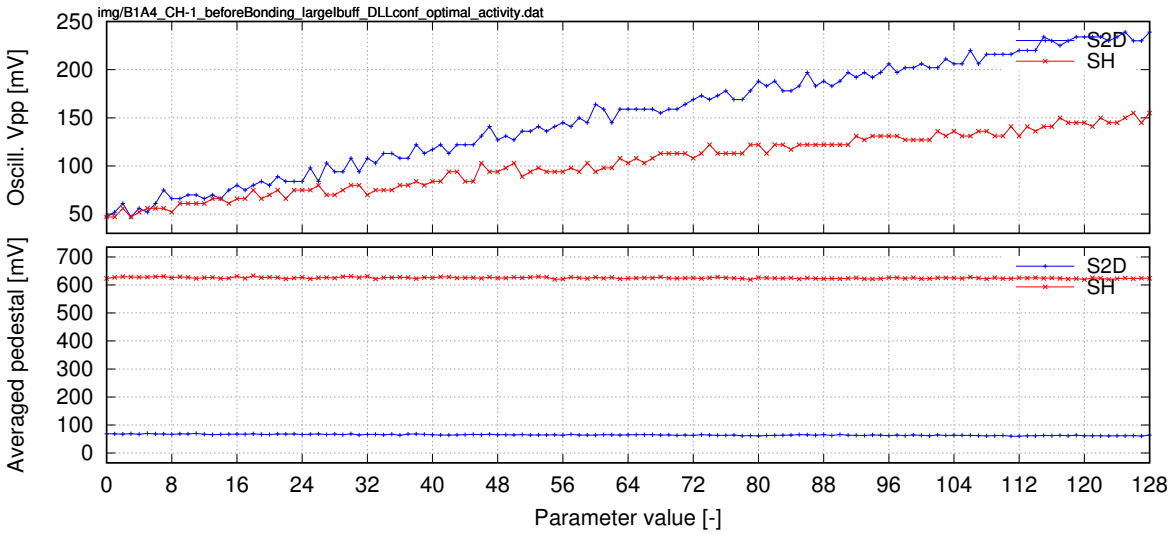

Figure 85: B1A4, channel -1, Before input pads bonded. Parameter=no. of active ADCs

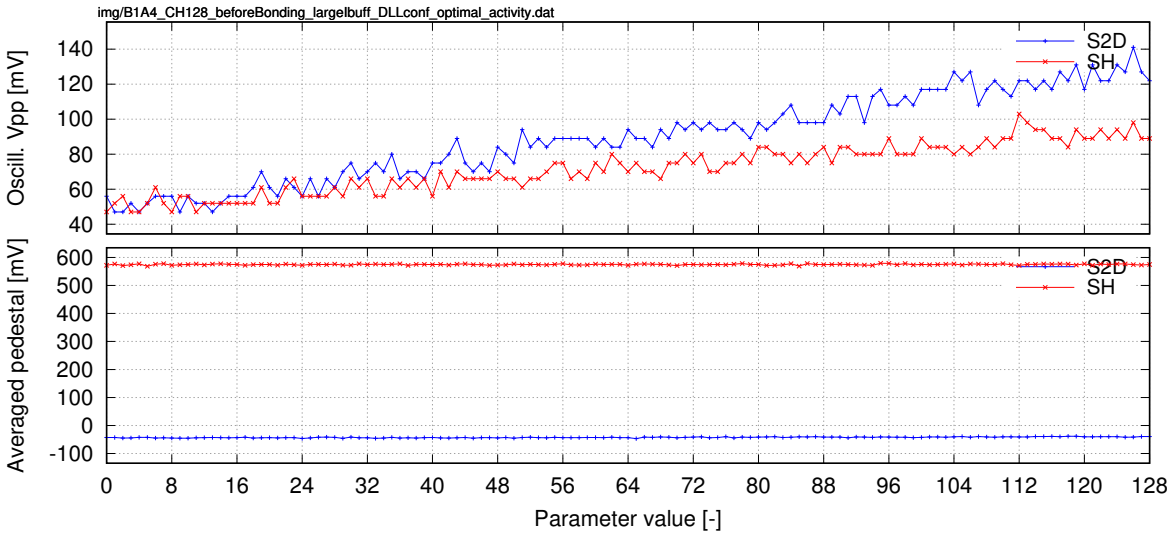

Figure 86: B1A4, channel 128, Before input pads bonded. Parameter=no. of active ADCs

5.2.2 Optimized test pulse and ADC delay

ASIC configuration: JC configuration (tables 1 & 2) + test pulse and ADC delay optimizations (table 3).

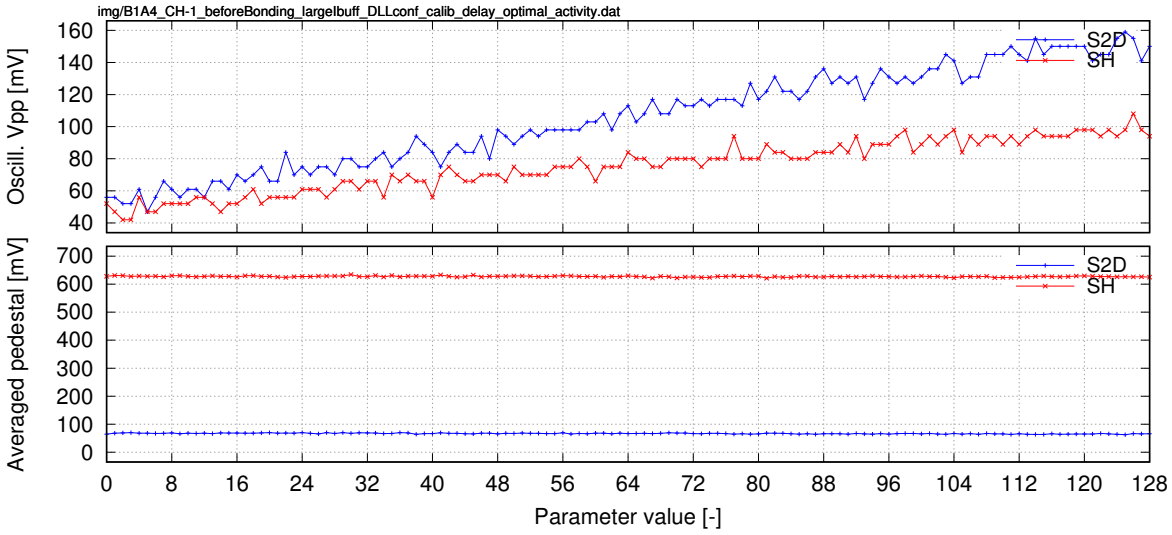

Figure 87: B1A4, channel -1, Before input pads bonded. Optimized test pulse and ADC delay. Parameter=no. of active ADCs

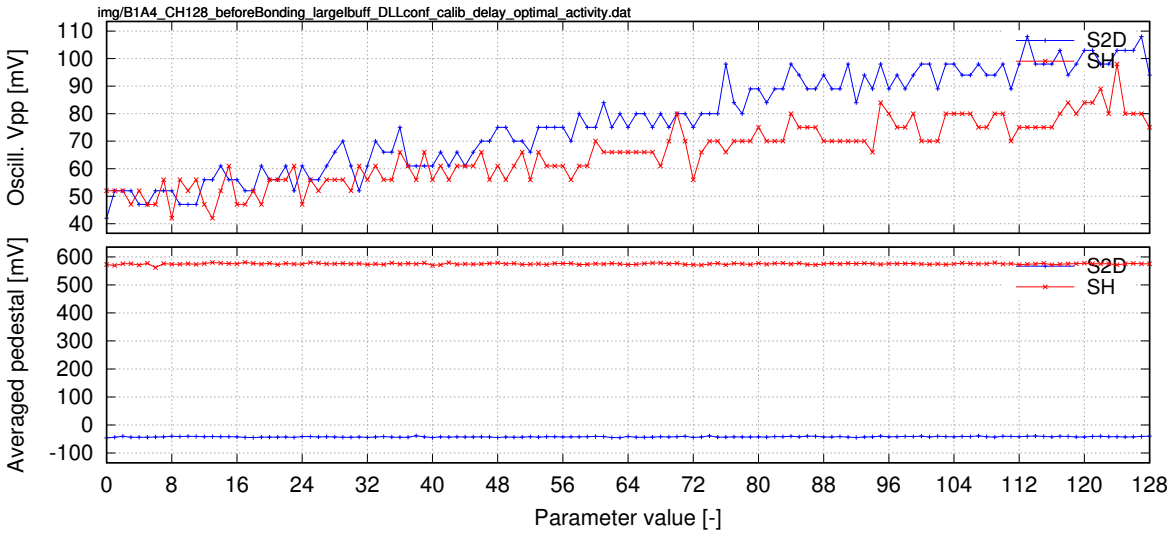

Figure 88: B1A4, channel 128, Before input pads bonded. Optimized test pulse and ADC delay. Parameter=no. of active ADCs

5.3 Cap-PCB bonded, 12 pF capacitors assembled; Ibuf current maximized

Cap-PCB assembled, bonded to SALT input pads 0 and 127, two 12 pF capacitors assembled to the cap-PCB.
Ibuf current maximized – 1 kΩ resistor between VDDA and Ibuf pad.

5.3.1 Default ASIC configuration

ASIC configuration: JC configuration (tables 1 & 2).

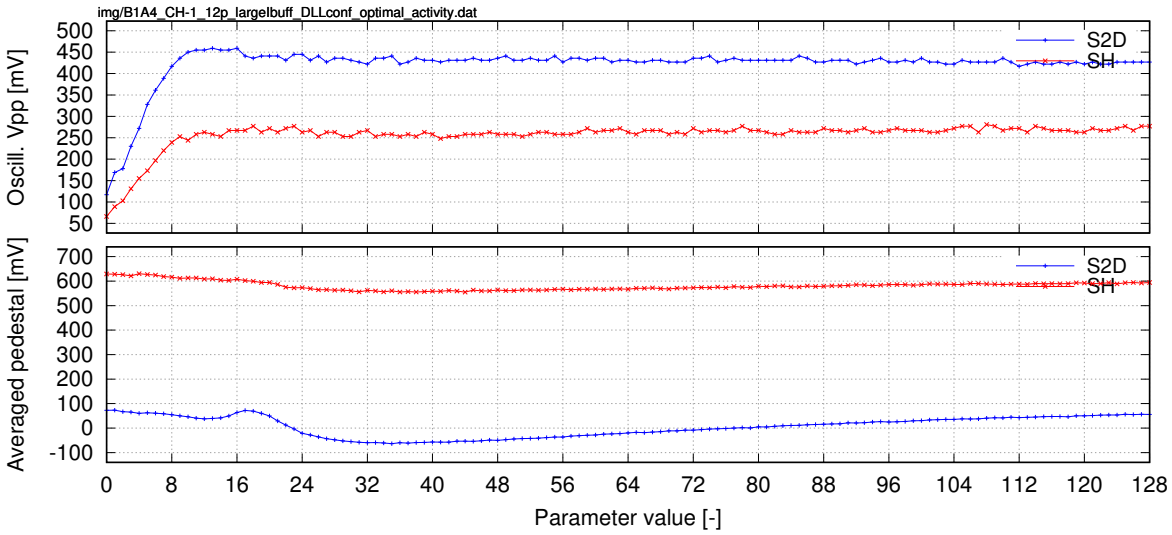

Figure 89: B1A4, channel -1, cap-PCB bonded, 12 pF capacitors; Ibuf current maximized. Parameter=no. of active ADCs

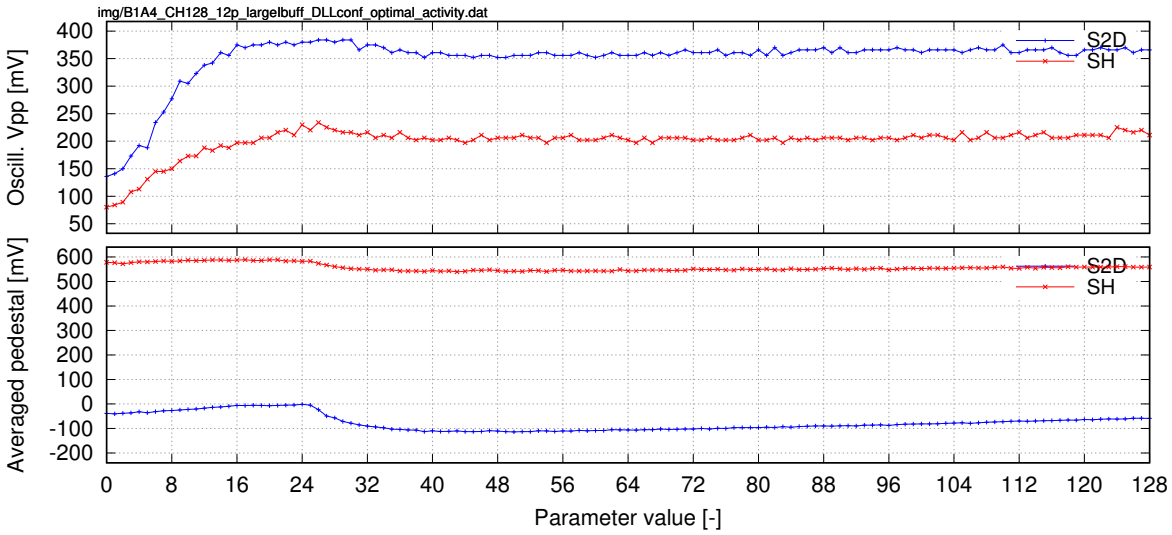

Figure 90: B1A4, channel 128, cap-PCB bonded, 12 pF capacitors; Ibuf current maximized. Parameter=no. of active ADCs

5.3.2 Optimized test pulse and ADC delay

ASIC configuration: JC configuration (tables 1 & 2) + test pulse and ADC delay optimizations (table 3).

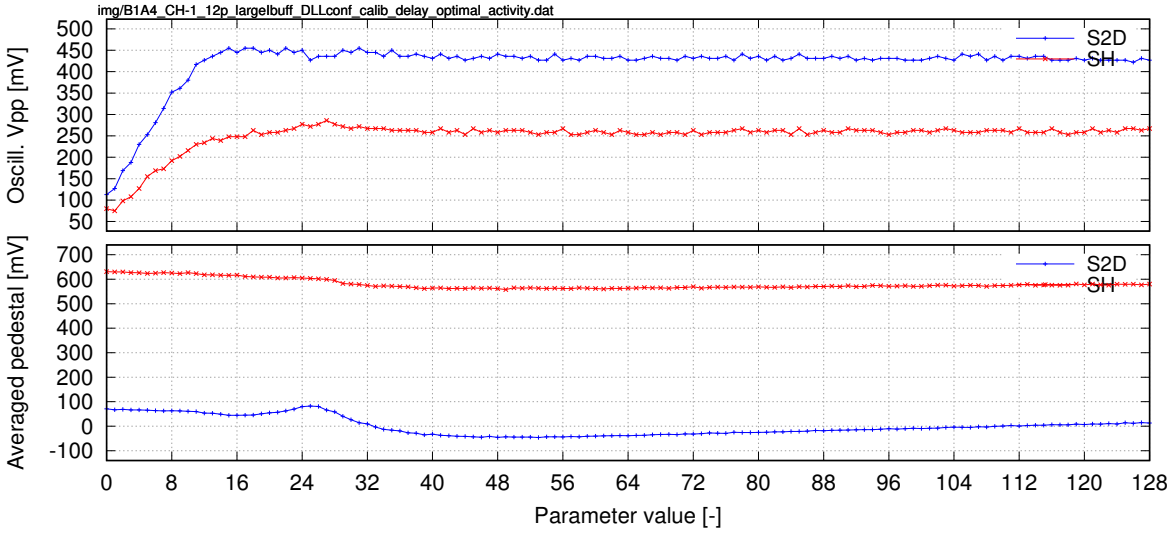

Figure 91: B1A4, channel -1, cap-PCB bonded, 12 pF capacitors; Ibuf current maximized. Optimized test pulse and ADC delay. Parameter=no. of active ADCs

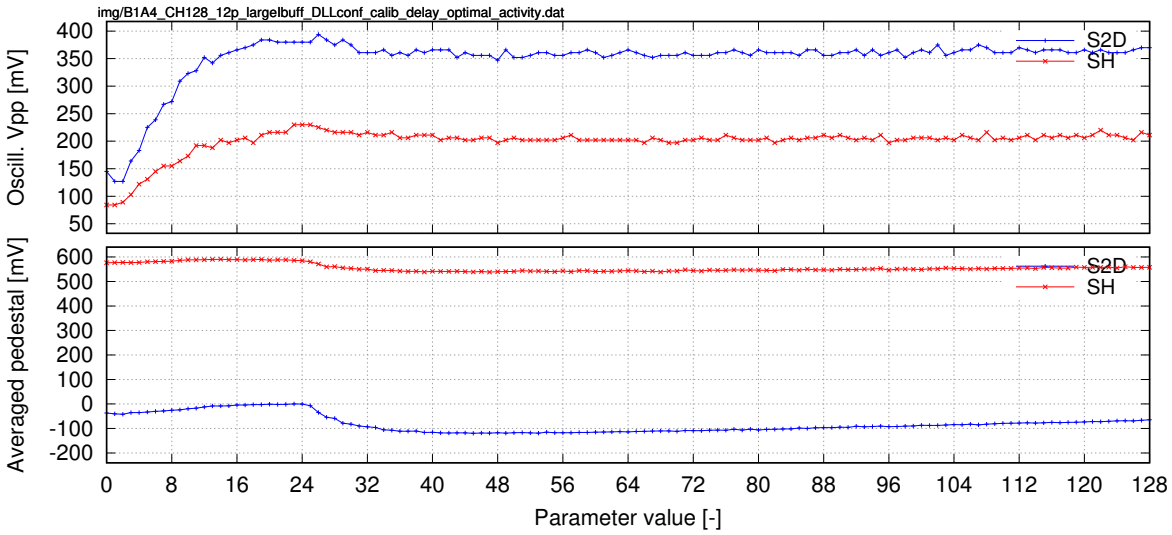

Figure 92: B1A4, channel 128, cap-PCB bonded, 12 pF capacitors; Ibuf current maximized. Optimized test pulse and ADC delay. Parameter=no. of active ADCs

5.4 Cap-PCB bonded, 12 pF capacitors assembled; Ibuf current maximized; Fsmp=33 MHz

Cap-PCB assembled, bonded to SALT input pads 0 and 127, two 12 pF capacitors assembled to the cap-PCB.
Ibuf current maximized – 1 kΩ resistor between VDDA and Ibuf pad.
Main clock (ADC sampling) frequency = 33 MHz.
Only channel 128 measured.

5.4.1 Default ASIC configuration

ASIC configuration: JC configuration (tables 1 & 2).

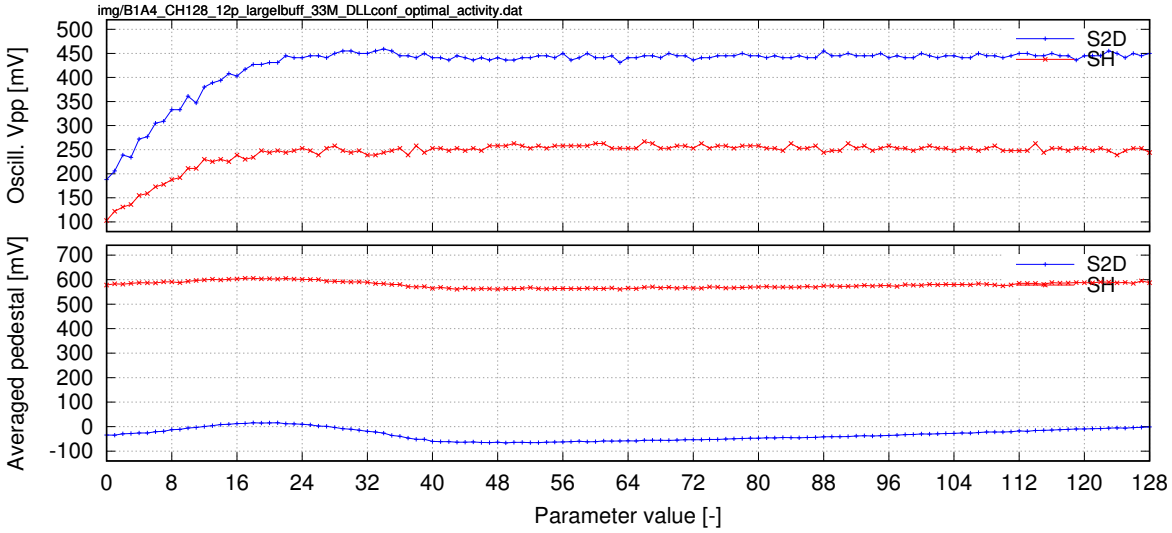

Figure 93: B1A4, channel 128, cap-PCB bonded, 12 pF capacitors; Ibuf current maximized; Fsmp=33 MHz. Parameter=no. of active ADCs

5.4.2 Optimized test pulse and ADC delay

ASIC configuration: JC configuration (tables 1 & 2) + test pulse and ADC delay optimizations (table 3).

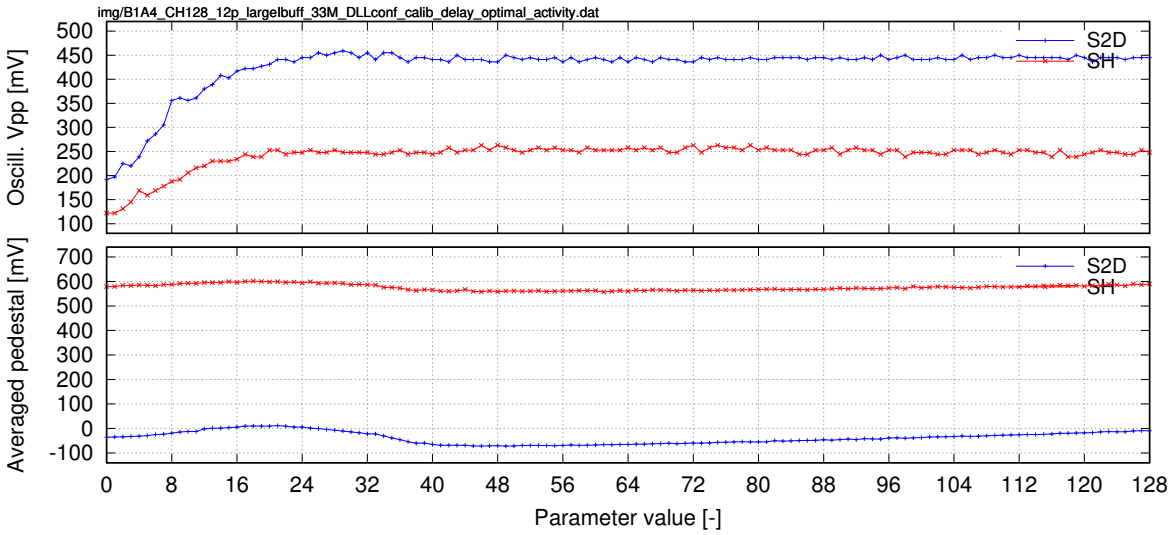

Figure 94: B1A4, channel 128, cap-PCB bonded, 12 pF capacitors; Ibuf current maximized; Fsmp=33 MHz. Optimized test pulse and ADC delay. Parameter=no. of active ADCs

5.5 Cap-PCB bonded, 12 pF capacitors assembled; Ibuf current maximized; Preamp GND configuration – input + backside

Cap-PCB assembled, bonded to SALT input pads 0 and 127, two 12 pF capacitors assembled to the cap-PCB.
Ibuf current maximized – 1 kΩ resistor between VDDA and Ibuf pad.
Preamp GND bonded from both sides - input pads + backside (default) pads.

5.5.1 Default ASIC configuration

ASIC configuration: JC configuration (tables 1 & 2).

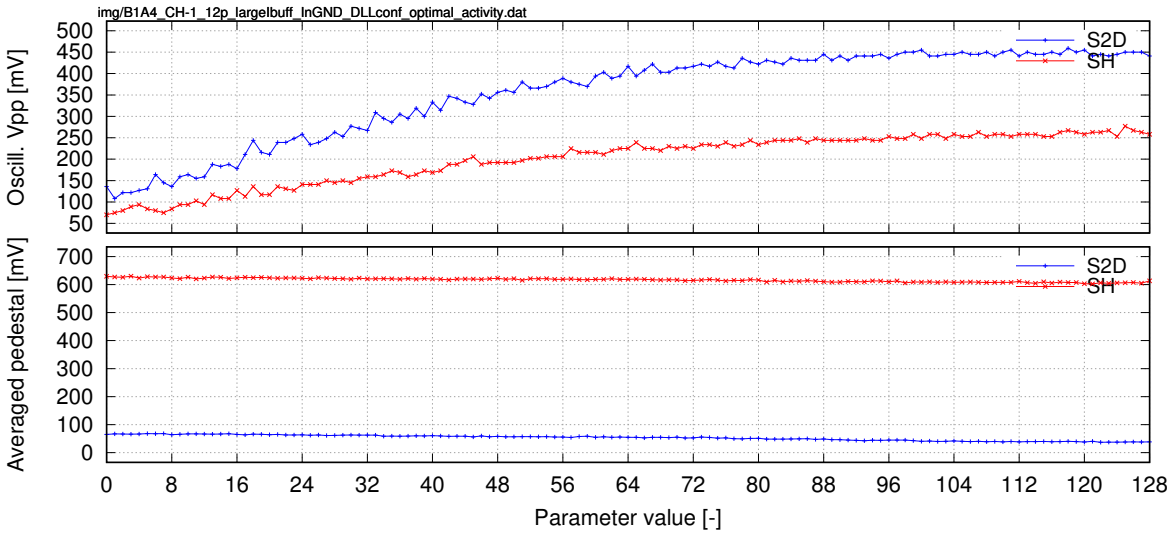

Figure 95: B1A4, channel -1, cap-PCB bonded, 12 pF capacitors; Ibuf current maximized; Preamp GND configuration – input + backside. Parameter=no. of active ADCs

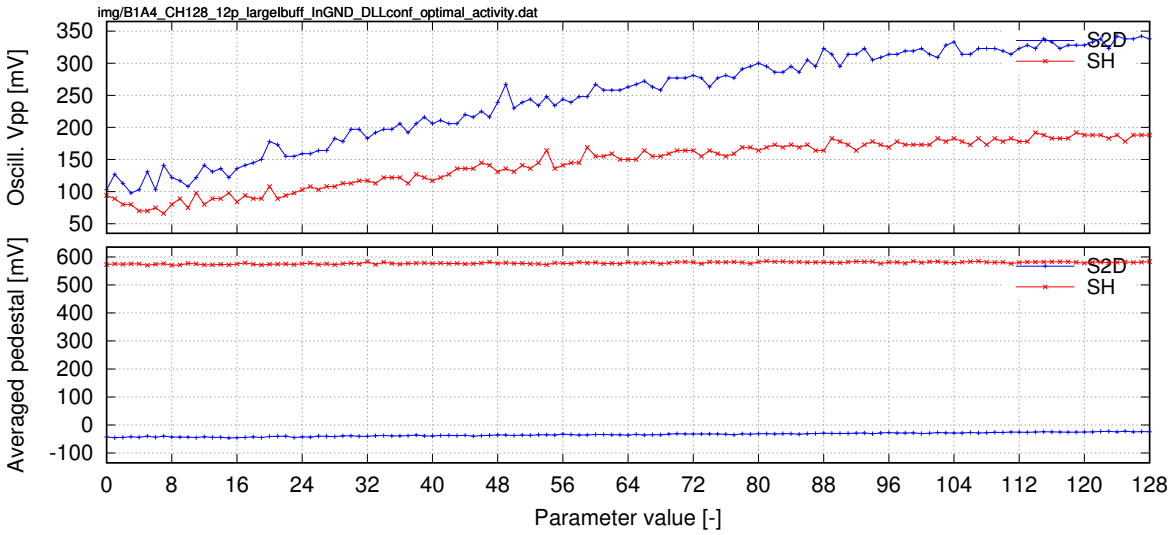

Figure 96: B1A4, channel 128, cap-PCB bonded, 12 pF capacitors; Ibuf current maximized; Preamp GND configuration – input + backside. Parameter=no. of active ADCs

5.5.2 Optimized test pulse and ADC delay

ASIC configuration: JC configuration (tables 1 & 2) + test pulse and ADC delay optimizations (table 3).

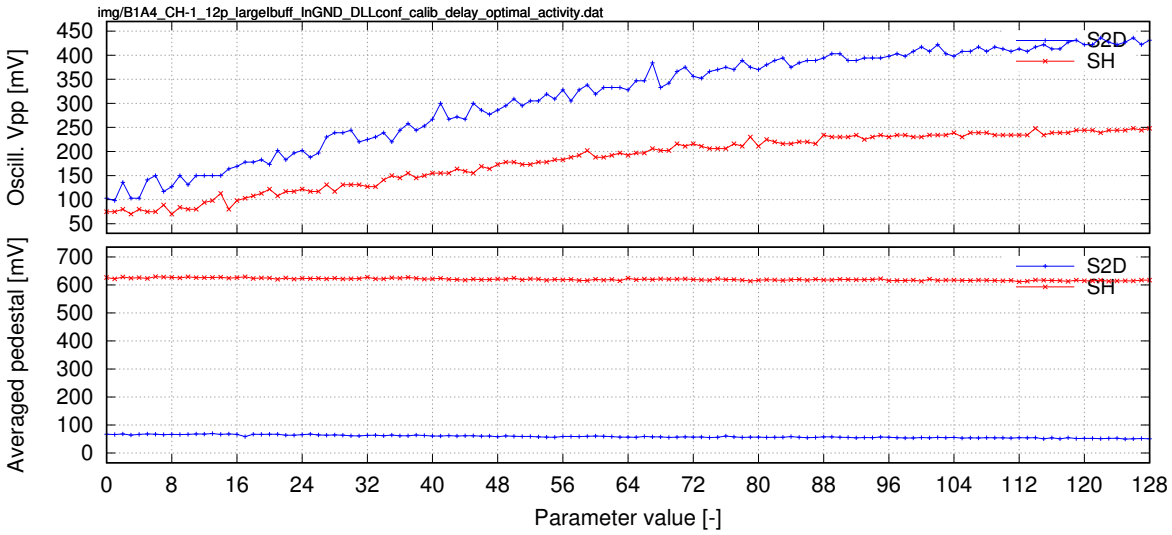

Figure 97: B1A4, channel -1, cap-PCB bonded, 12 pF capacitors; Ibuf current maximized; Preamp GND configuration – input + backside. Optimized test pulse and ADC delay. Parameter=no. of active ADCs

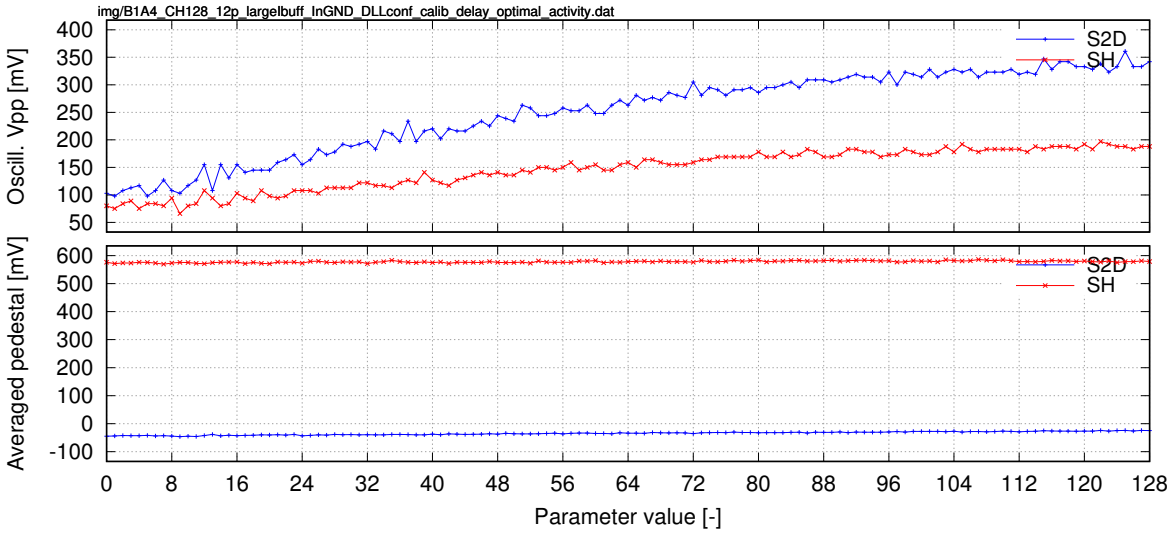

Figure 98: B1A4, channel 128, cap-PCB bonded, 12 pF capacitors; Ibuf current maximized; Preamp GND configuration – input + backside. Optimized test pulse and ADC delay. Parameter=no. of active ADCs

5.6 Cap-PCB bonded, 12 pF capacitors assembled; Ibuf current maximized; Preamp GND configuration – only input

Cap-PCB assembled, bonded to SALT input pads 0 and 127, two 12 pF capacitors assembled to the cap-PCB.
Ibuf current maximized – 1 kΩ resistor between VDDA and Ibuf pad.
Preamp GND bonded only using input pads.

5.6.1 Default ASIC configuration

ASIC configuration: JC configuration (tables 1 & 2).

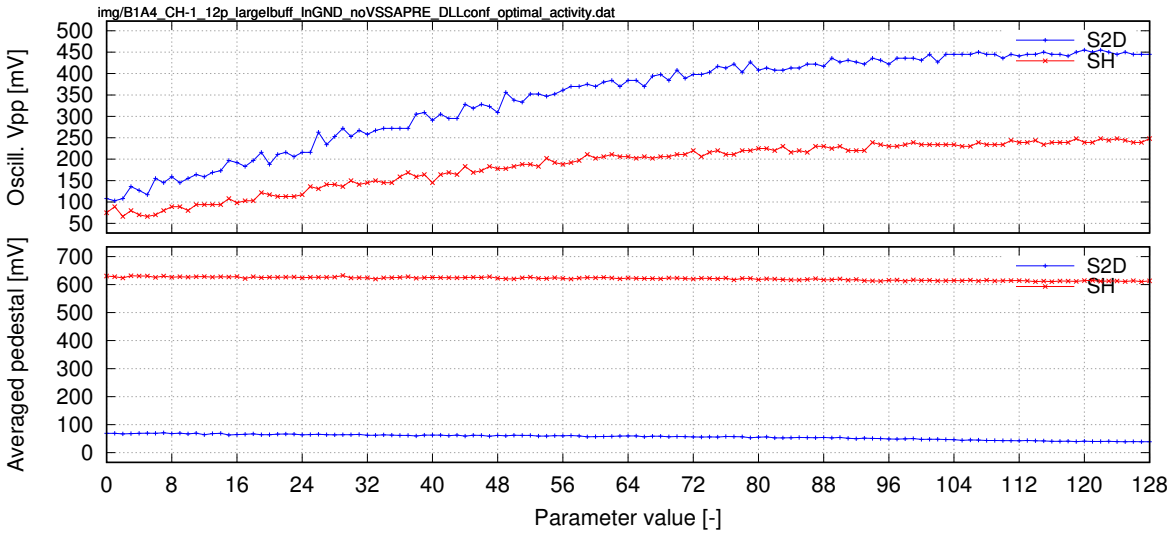

Figure 99: B1A4, channel -1, cap-PCB bonded, 12 pF capacitors; Ibuf current maximized; Preamp GND configuration – only input. Parameter=no. of active ADCs

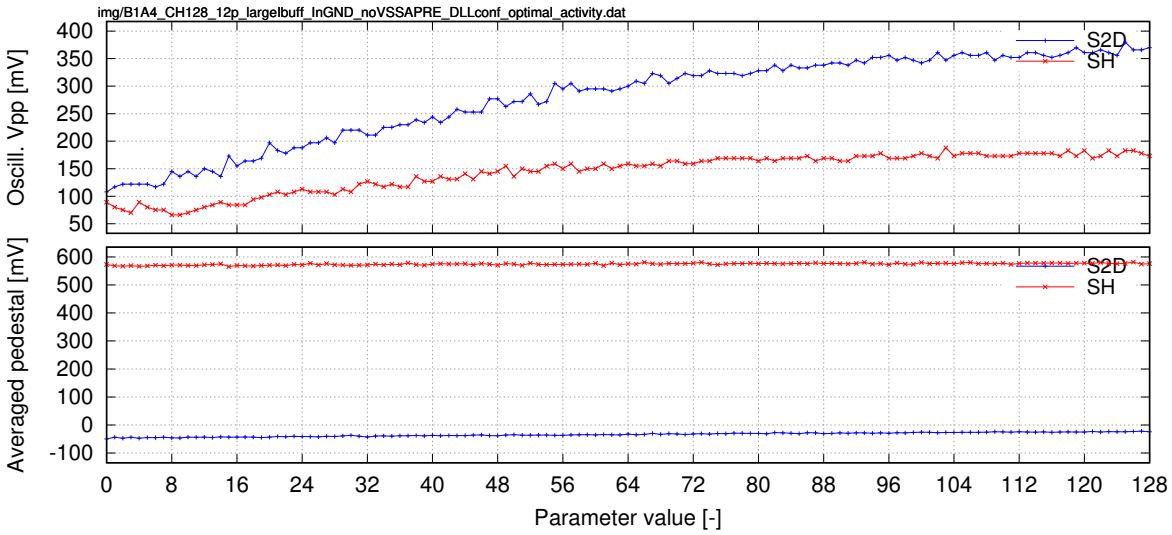

Figure 100: B1A4, channel 128, cap-PCB bonded, 12 pF capacitors; Ibuf current maximized; Preamp GND configuration – only input. Parameter=no. of active ADCs

5.6.2 Optimized test pulse and ADC delay

ASIC configuration: JC configuration (tables 1 & 2) + test pulse and ADC delay optimizations (table 3).

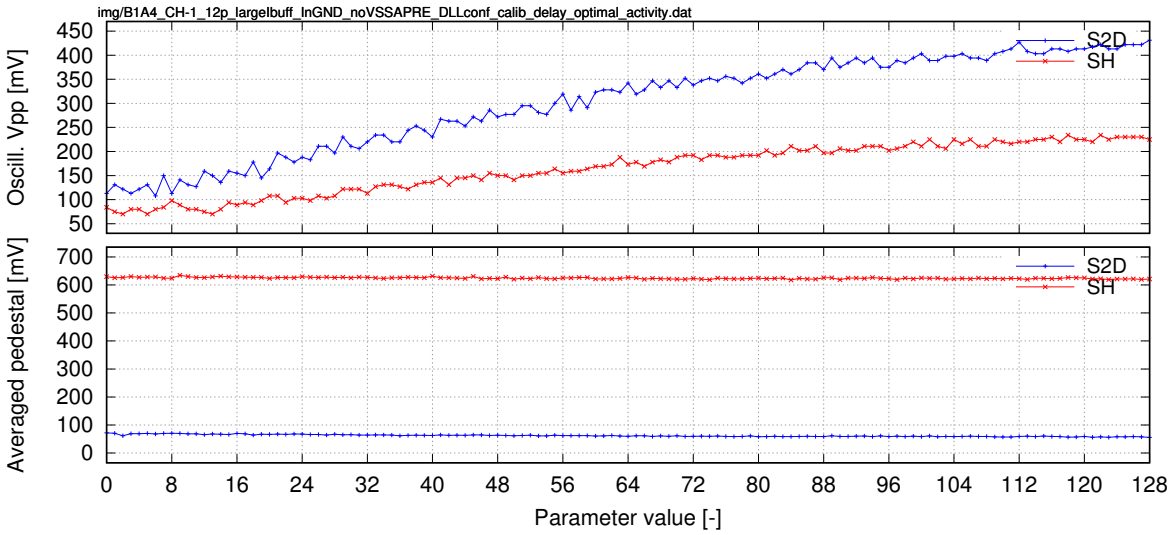

Figure 101: B1A4, channel -1, cap-PCB bonded, 12 pF capacitors; Ibuf current maximized; Preamp GND configuration – only input. Optimized test pulse and ADC delay. Parameter=no. of active ADCs

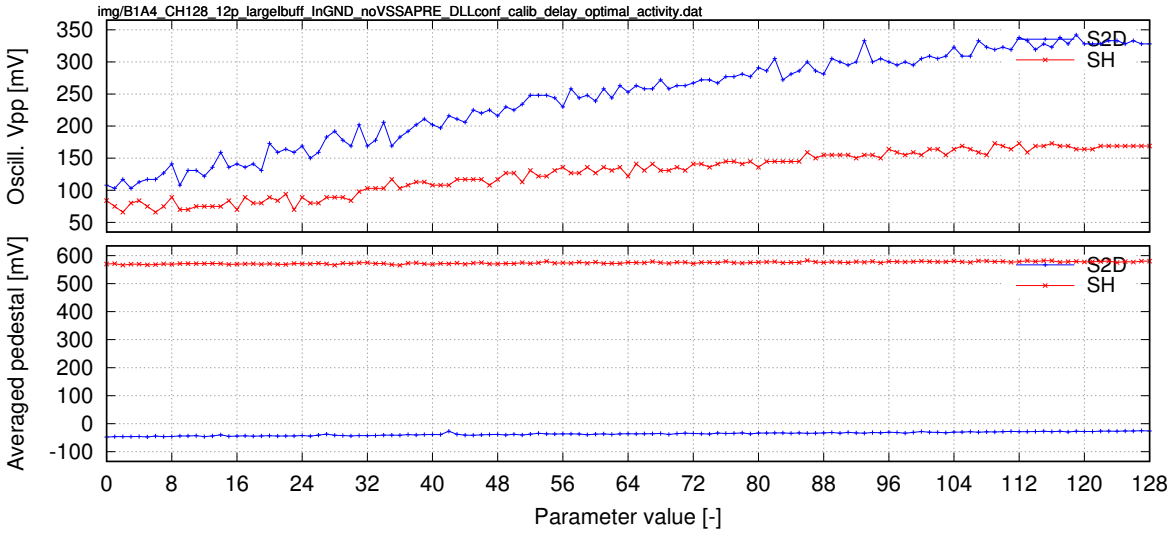

Figure 102: B1A4, channel 128, cap-PCB bonded, 12 pF capacitors; Ibuf current maximized; Preamp GND configuration – only input. Optimized test pulse and ADC delay. Parameter=no. of active ADCs

5.7 Cap-PCB bonded, 12 pF capacitors assembled; Ibuf current maximized; floating copper foil on ASIC; Preamp GND configuration – only input

Cap-PCB assembled, bonded to SALT input pads 0 and 127, two 12 pF capacitors assembled to the cap-PCB.
Ibuf current maximized – 1 kΩ resistor between VDDA and Ibuf pad.
Floating copper foil glued directly on passivation on top of the ASIC (see figure 149).
Preamp GND bonded only using input pads.

5.7.1 Default ASIC configuration

ASIC configuration: JC configuration (tables 1 & 2).

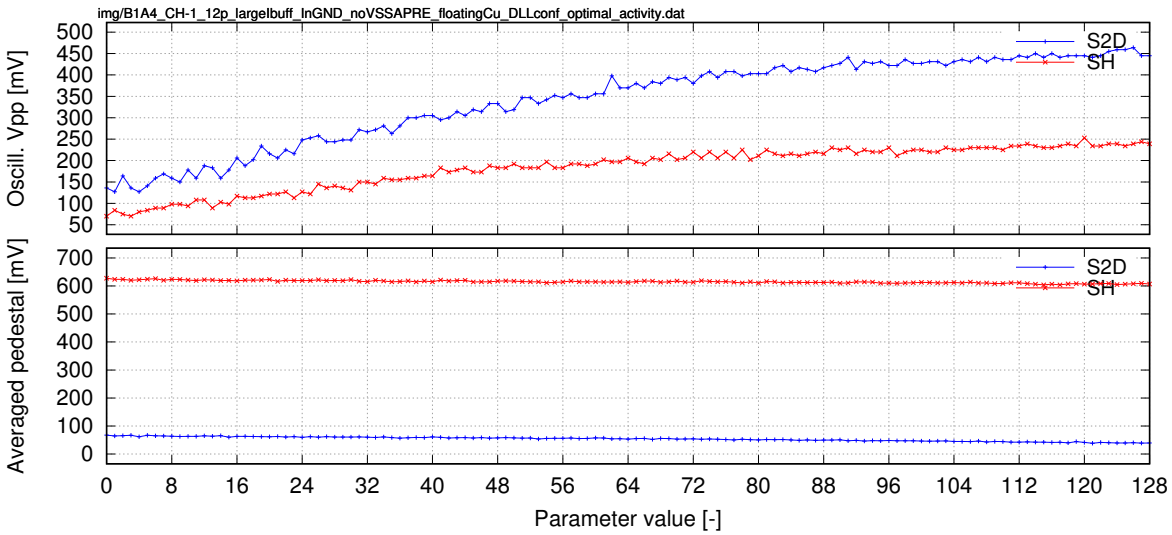

Figure 103: B1A4, channel -1, cap-PCB bonded, 12 pF capacitors; Ibuf current maximized; floating copper foil on ASIC; Preamp GND configuration – only input. Parameter=no. of active ADCs

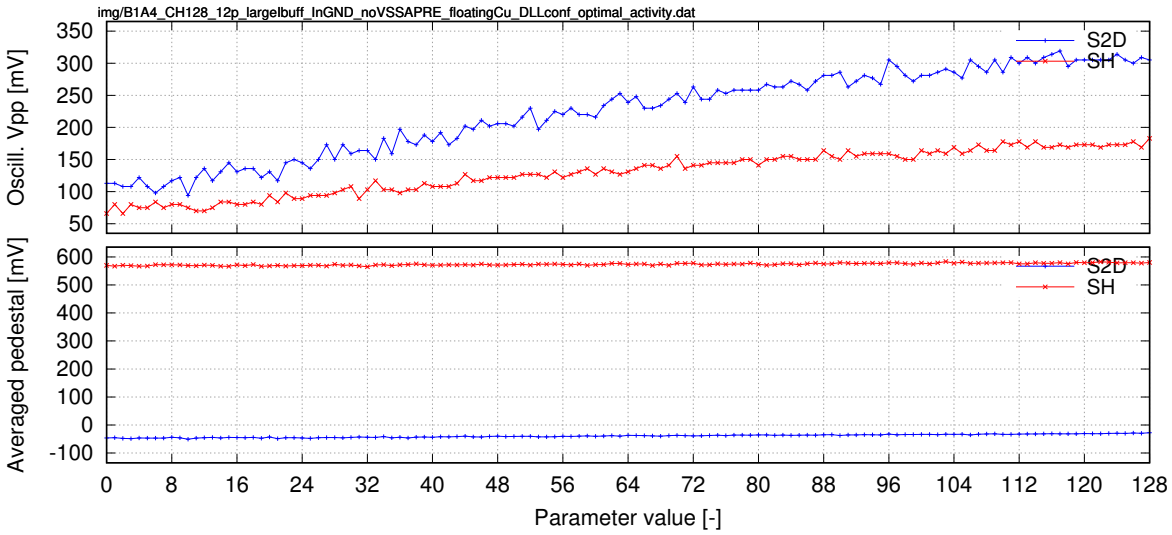

Figure 104: B1A4, channel 128, cap-PCB bonded, 12 pF capacitors; Ibuf current maximized; floating copper foil on ASIC; Preamp GND configuration – only input. Parameter=no. of active ADCs

5.7.2 Optimized test pulse and ADC delay

ASIC configuration: JC configuration (tables 1 & 2) + test pulse and ADC delay optimizations (table 3).

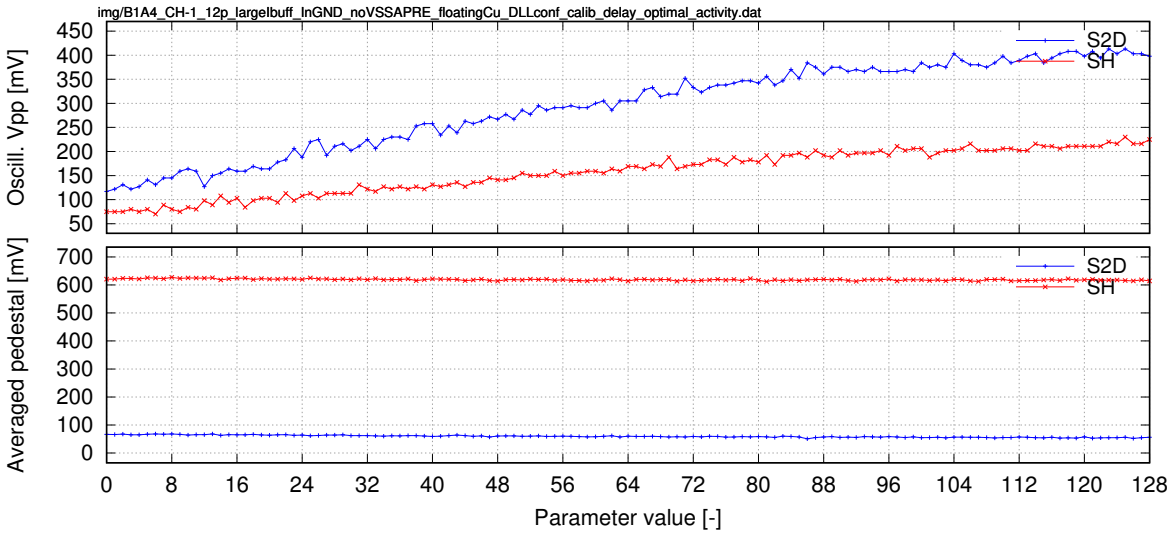

Figure 105: B1A4, channel -1, cap-PCB bonded, 12 pF capacitors; Ibuf current maximized; floating copper foil on ASIC; Preamp GND configuration – only input. Optimized test pulse and ADC delay. Parameter=no. of active ADCs

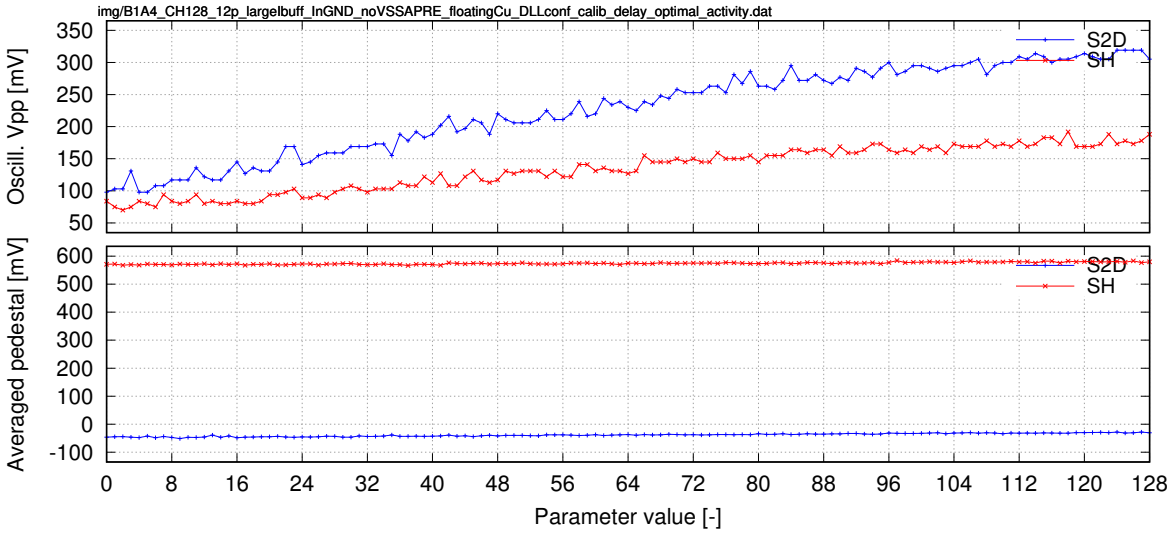

Figure 106: B1A4, channel 128, cap-PCB bonded, 12 pF capacitors; Ibuf current maximized; floating copper foil on ASIC; Preamp GND configuration – only input. Optimized test pulse and ADC delay. Parameter=no. of active ADCs

5.8 Cap-PCB bonded, 12 pF capacitors assembled; Ibuf current maximized; floating copper foil on ASIC; Preamp GND configuration – input + backside

Cap-PCB assembled, bonded to SALT input pads 0 and 127, two 12 pF capacitors assembled to the cap-PCB.
Ibuf current maximized – 1 kΩ resistor between VDDA and Ibuf pad.
Floating copper foil glued directly on passivation on top of the ASIC (see figure 149).
Preamp GND bonded from both sides - input pads + backside (default) pads.

5.8.1 Default ASIC configuration

ASIC configuration: JC configuration (tables 1 & 2).

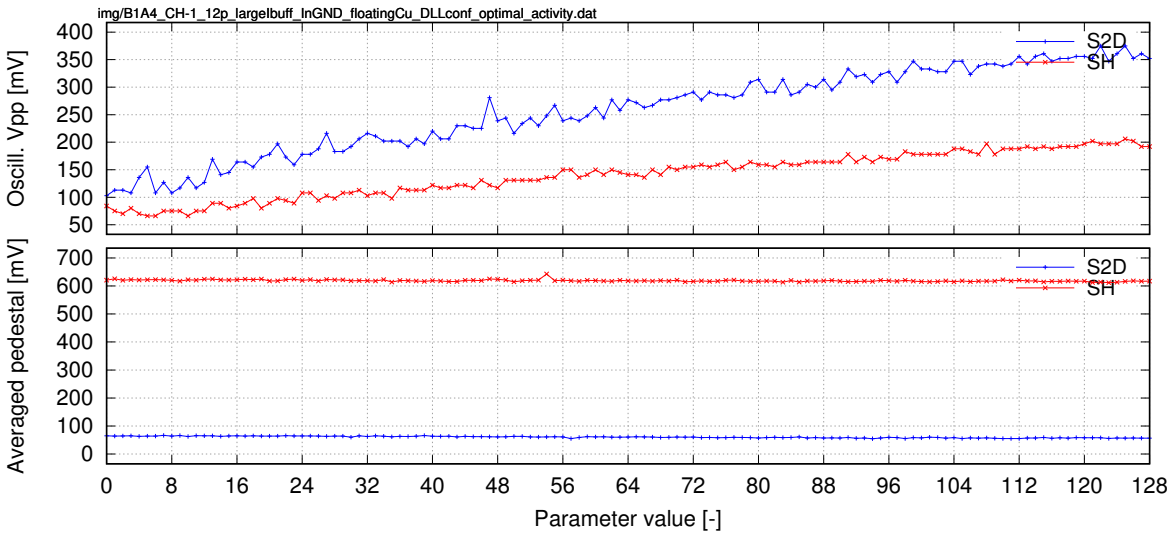

Figure 107: B1A4, channel -1, cap-PCB bonded, 12 pF capacitors; Ibuf current maximized; floating copper foil on ASIC; Preamp GND configuration – input + backside. Parameter=no. of active ADCs

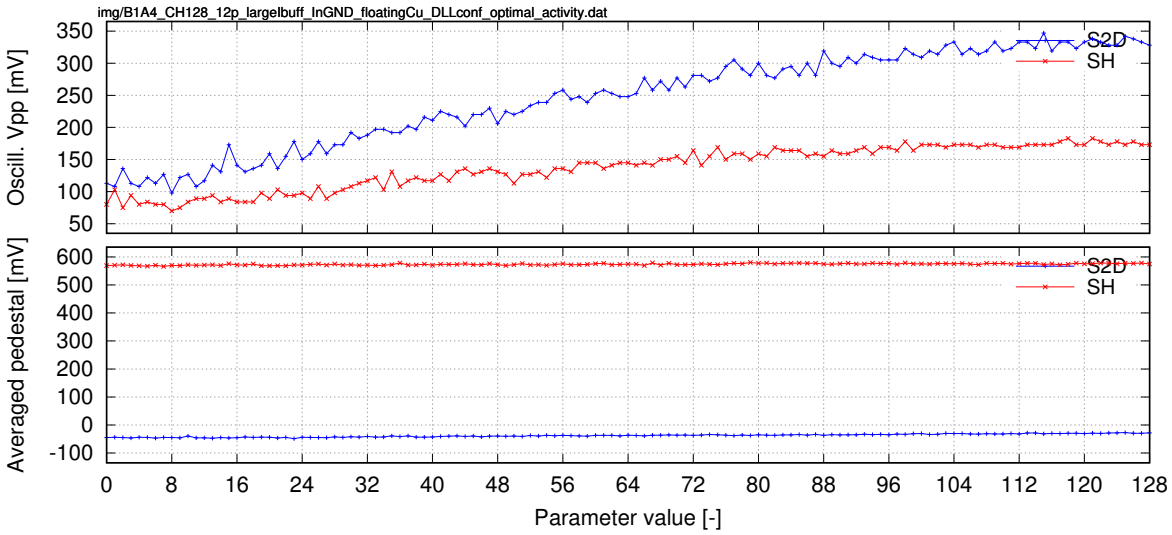

Figure 108: B1A4, channel 128, cap-PCB bonded, 12 pF capacitors; Ibuf current maximized; floating copper foil on ASIC; Preamp GND configuration – input + backside. Parameter=no. of active ADCs

5.8.2 Optimized test pulse and ADC delay

ASIC configuration: JC configuration (tables 1 & 2) + test pulse and ADC delay optimizations (table 3).

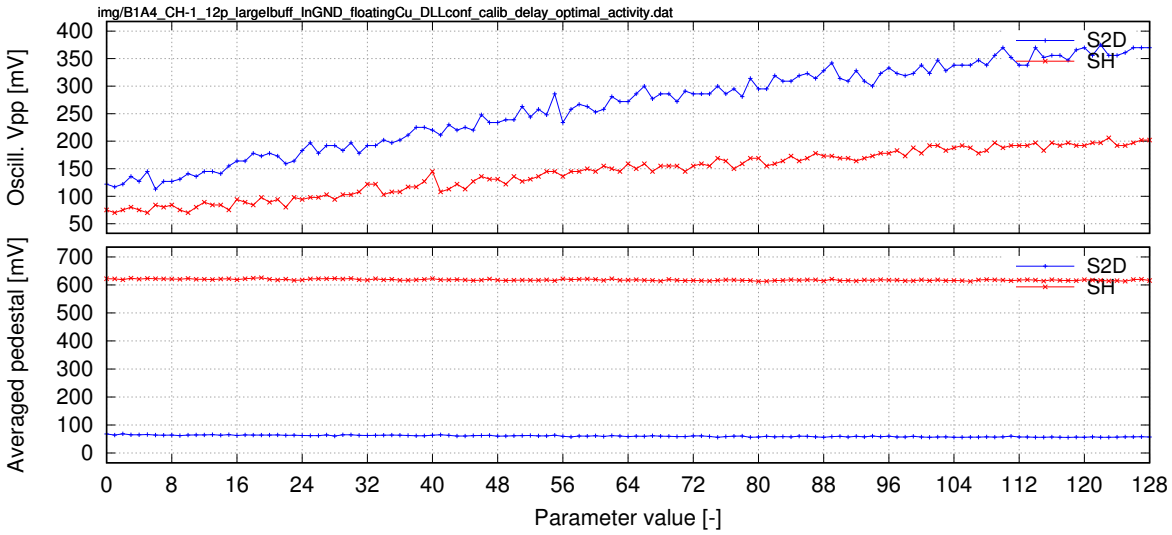

Figure 109: B1A4, channel -1, cap-PCB bonded, 12 pF capacitors; Ibuf current maximized; floating copper foil on ASIC; Preamp GND configuration – input + backside. Optimized test pulse and ADC delay. Parameter=no. of active ADCs

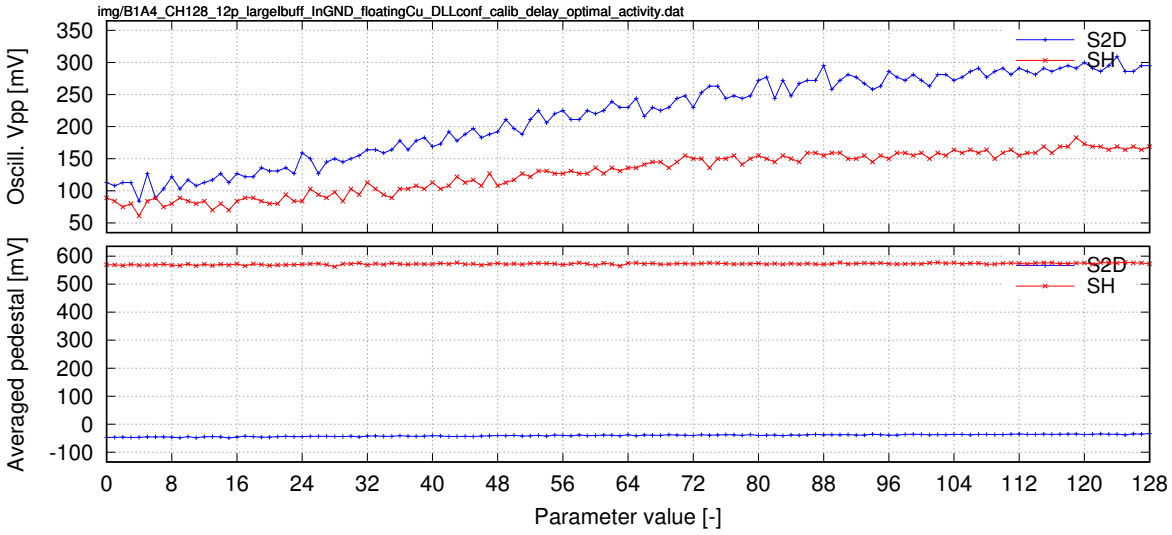

Figure 110: B1A4, channel 128, cap-PCB bonded, 12 pF capacitors; Ibuf current maximized; floating copper foil on ASIC; Preamp GND configuration – input + backside. Optimized test pulse and ADC delay. Parameter=no. of active ADCs

5.9 Cap-PCB bonded, 12 pF capacitors assembled; Ibuf current maximized; floating copper foil on ASIC; Preamp GND configuration – only backside

Cap-PCB assembled, bonded to SALT input pads 0 and 127, two 12 pF capacitors assembled to the cap-PCB.
Ibuf current maximized – 1 kΩ resistor between VDDA and Ibuf pad.
Floating copper foil glued directly on passivation on top of the ASIC (see figure 149).
Preamp GND bonded only from backside (default pads).

5.9.1 Default ASIC configuration

ASIC configuration: JC configuration (tables 1 & 2).

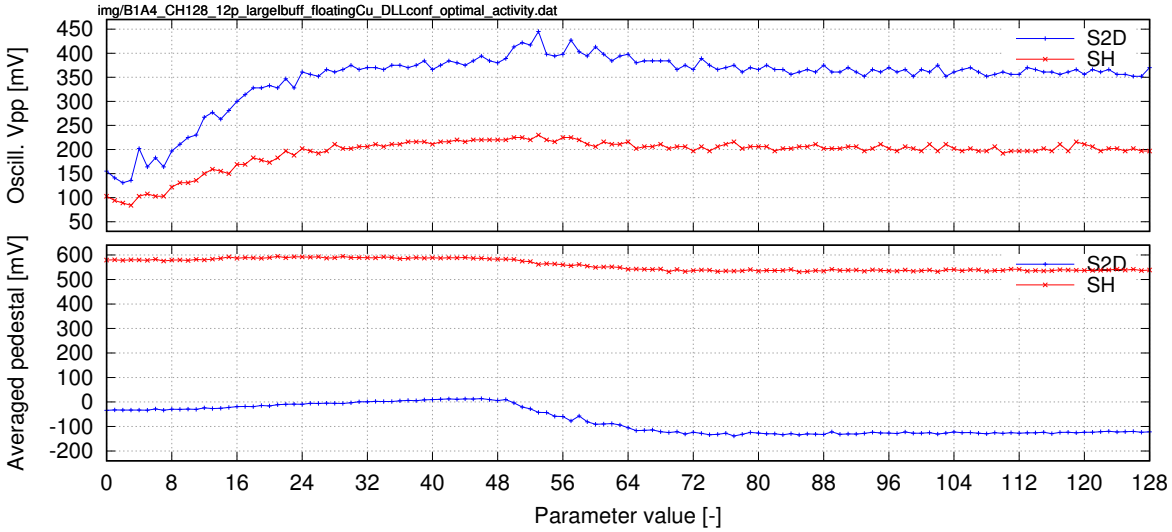

Figure 111: B1A4, channel 128, cap-PCB bonded, 12 pF capacitors; Ibuf current maximized; floating copper foil on ASIC; Preamp GND configuration – only backside. Parameter=no. of active ADCs

5.9.2 Optimized test pulse and ADC delay

ASIC configuration: JC configuration (tables 1 & 2) + test pulse and ADC delay optimizations (table 3).

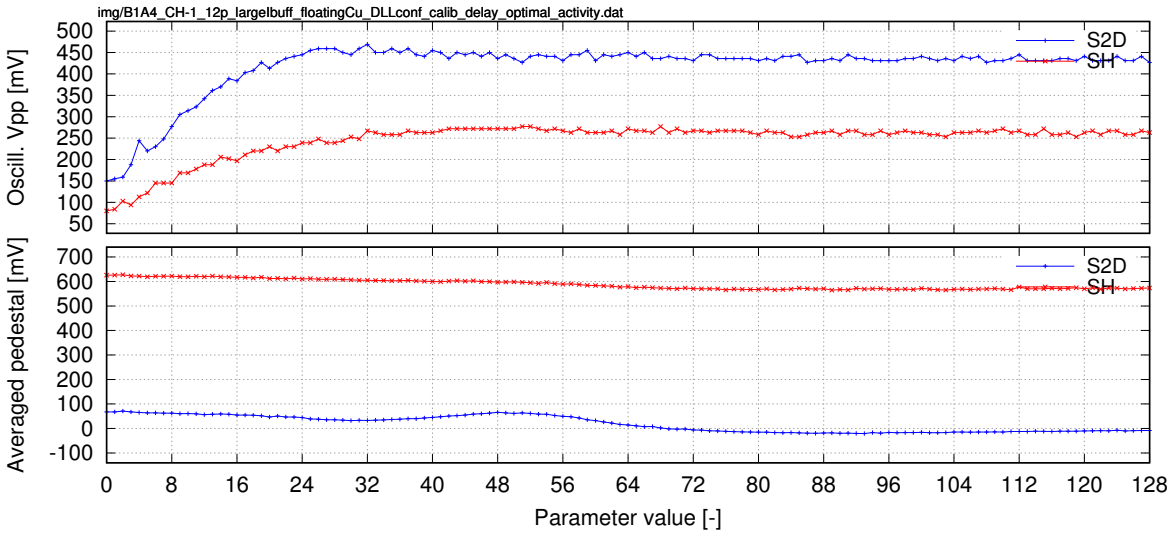

Figure 112: B1A4, channel -1, cap-PCB bonded, 12 pF capacitors; Ibuf current maximized; floating copper foil on ASIC; Preamp GND configuration – only backside. Optimized test pulse and ADC delay. Parameter=no. of active ADCs

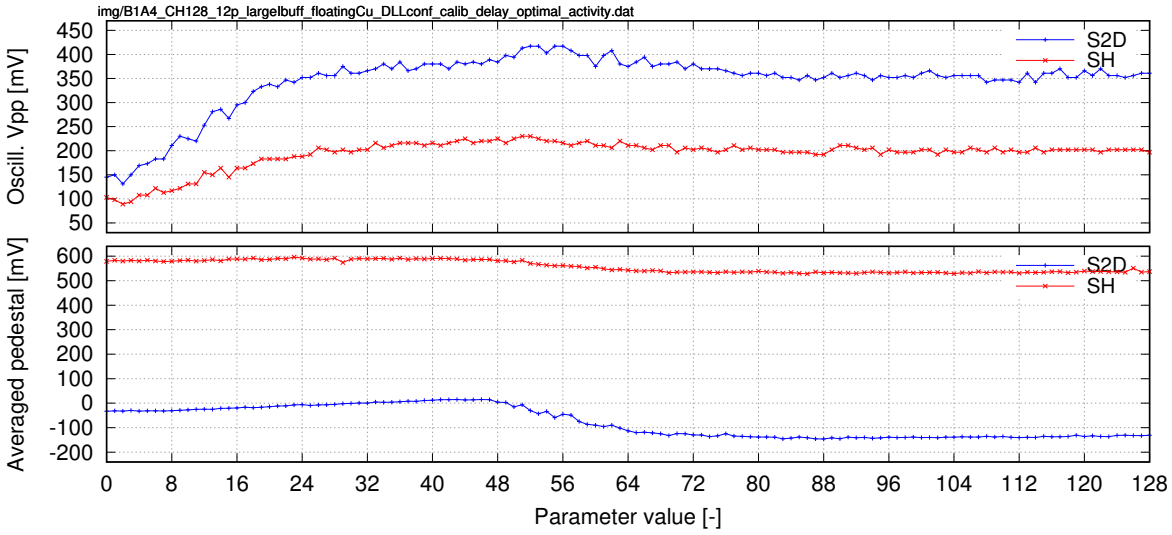

Figure 113: B1A4, channel 128, cap-PCB bonded, 12 pF capacitors; Ibuf current maximized; floating copper foil on ASIC; Preamp GND configuration – only backside. Optimized test pulse and ADC delay. Parameter=no. of active ADCs

5.10 Cap-PCB bonded, 12 pF capacitors assembled; Ibuf current maximized; floating copper foil on ASIC; All inputs grounded; Preamp GND configuration – only backside

Cap-PCB assembled, bonded to SALT input pads 0 and 127, two 12 pF capacitors assembled to the cap-PCB.
Ibuf current maximized – 1 kΩ resistor between VDDA and Ibuf pad.
Floating copper foil glued directly on passivation on top of the ASIC (see figure 149).
All inputs was bonded to ground (except test channels -1 and 128) Preamp GND bonded only from backside (default pads).

5.10.1 Default ASIC configuration

ASIC configuration: JC configuration (tables 1 & 2).

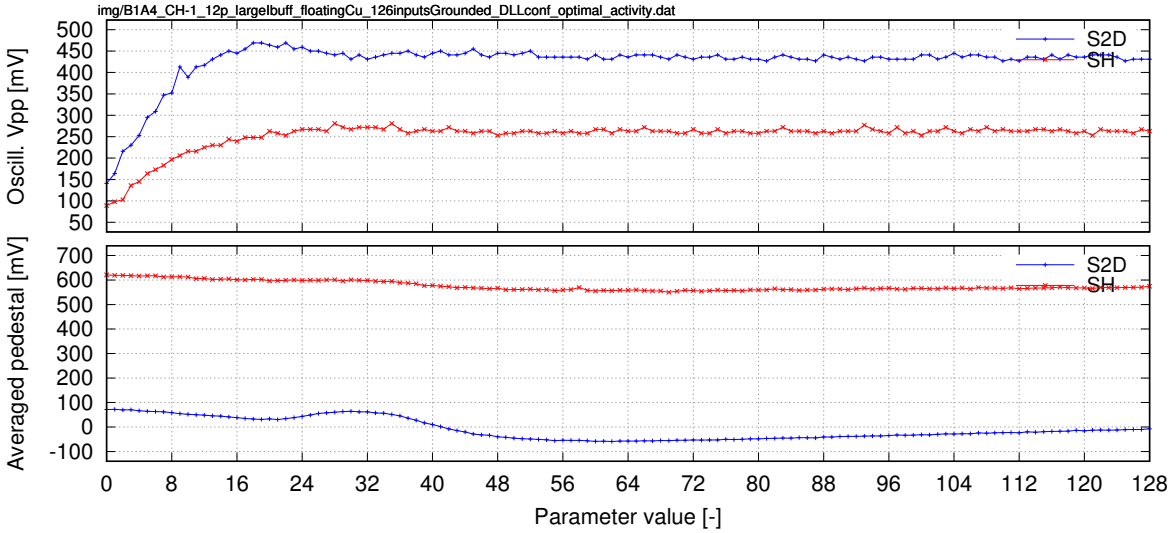

Figure 114: B1A4, channel -1, cap-PCB bonded, 12 pF capacitors; Ibuf current maximized; floating copper foil on ASIC; All inputs grounded; Preamp GND configuration – only backside. Parameter=no. of active ADCs

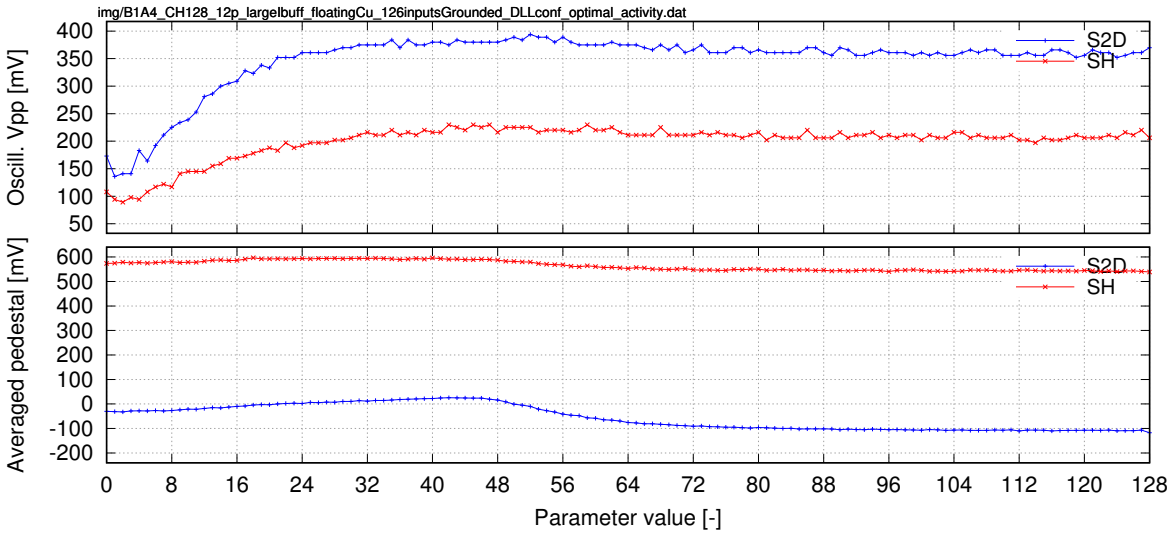

Figure 115: B1A4, channel 128, cap-PCB bonded, 12 pF capacitors; Ibuf current maximized; floating copper foil on ASIC; All inputs grounded; Preamp GND configuration – only backside. Parameter=no. of active ADCs

5.10.2 Optimized test pulse and ADC delay

ASIC configuration: JC configuration (tables 1 & 2) + test pulse and ADC delay optimizations (table 3).

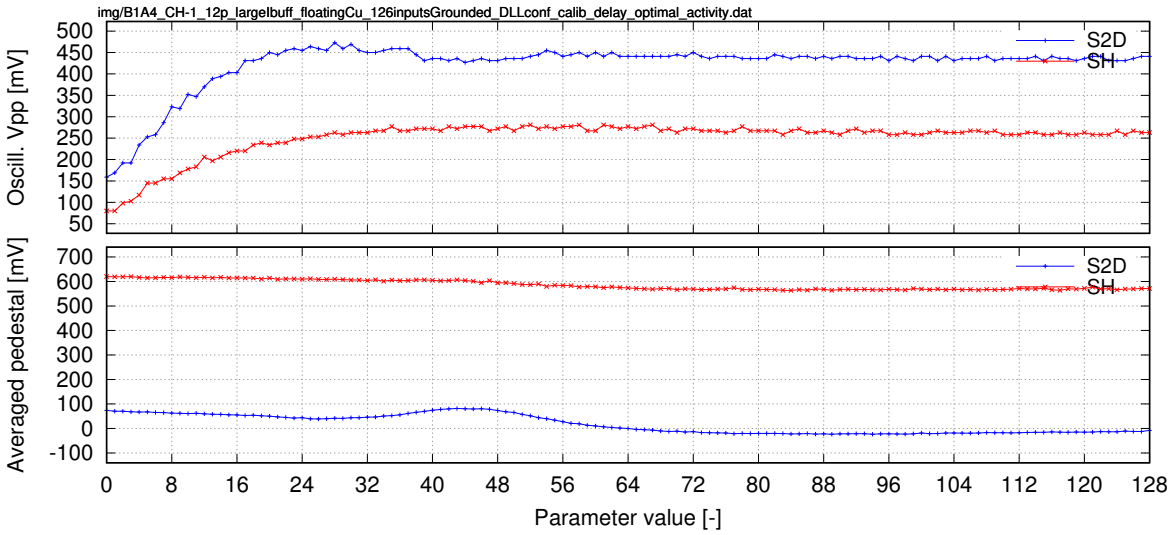

Figure 116: B1A4, channel -1, cap-PCB bonded, 12 pF capacitors; Ibuf current maximized; floating copper foil on ASIC; All inputs grounded; Preamp GND configuration – only backside. Optimized test pulse and ADC delay. Parameter=no. of active ADCs

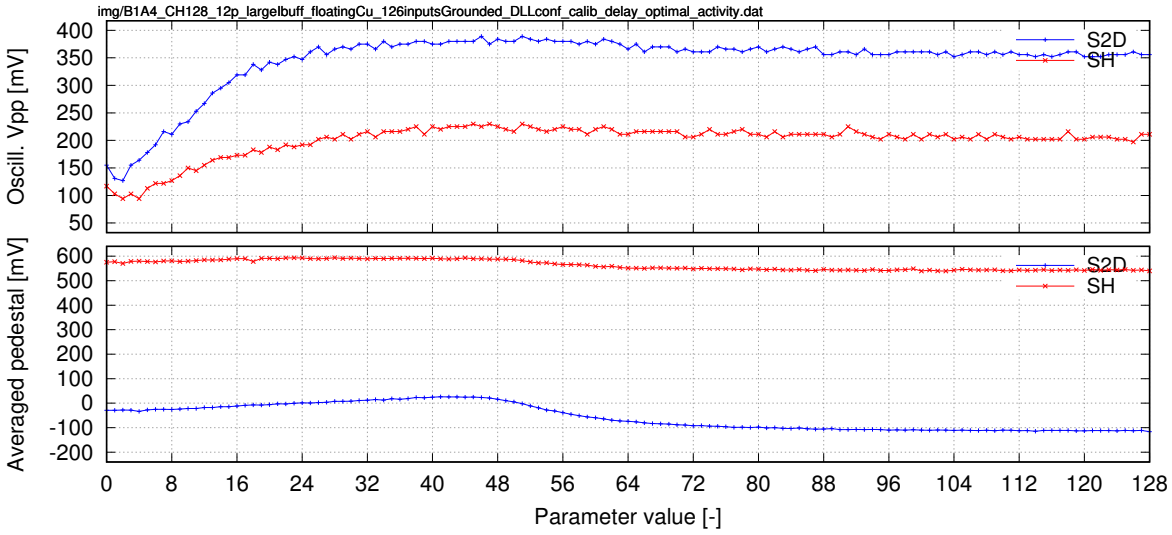

Figure 117: B1A4, channel 128, cap-PCB bonded, 12 pF capacitors; Ibuf current maximized; floating copper foil on ASIC; All inputs grounded; Preamp GND configuration – only backside. Optimized test pulse and ADC delay. Parameter=no. of active ADCs

5.11 Cap-PCB bonded, 12 pF capacitors assembled; Ibuf current maximized; floating small horizontal copper foil on ASIC; All inputs grounded; Preamp GND configuration – only backside

Cap-PCB assembled, bonded to SALT input pads 0 and 127, two 12 pF capacitors assembled to the cap-PCB.
Ibuf current maximized – 1 kΩ resistor between VDDA and Ibuf pad.
Floating small horizontal copper foil glued directly on passivation on top of the ASIC (see figure 151).
All inputs was bonded to ground (except test channels -1 and 128) Preamp GND bonded only from backside (default pads).

5.11.1 Default ASIC configuration

ASIC configuration: JC configuration (tables 1 & 2).

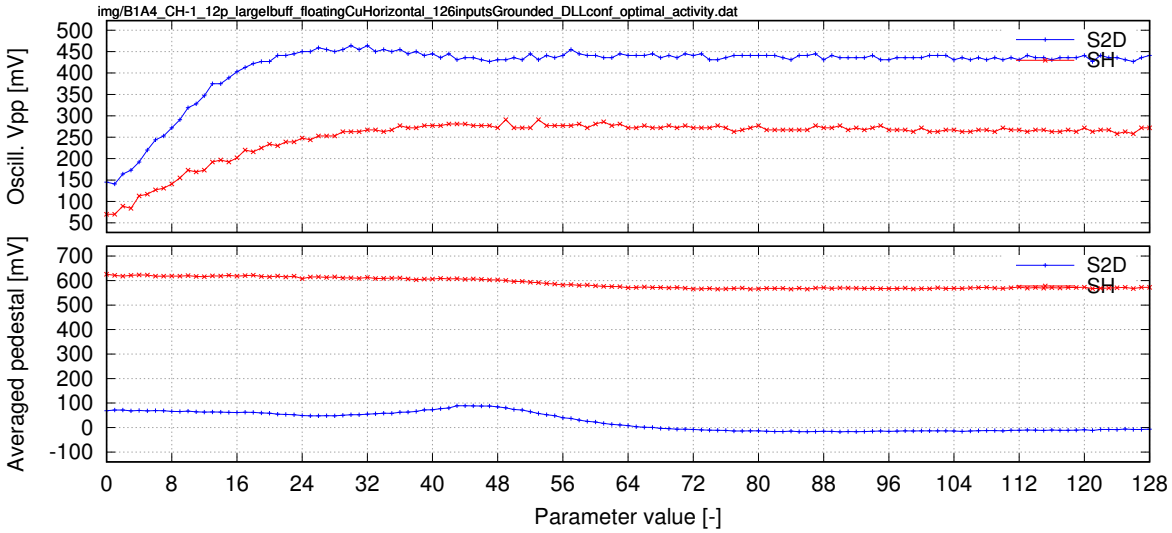

Figure 118: B1A4, channel -1, cap-PCB bonded, 12 pF capacitors; Ibuf current maximized; floating small horizontal copper foil on ASIC; All inputs grounded; Preamp GND configuration – only backside. Parameter=no. of active ADCs

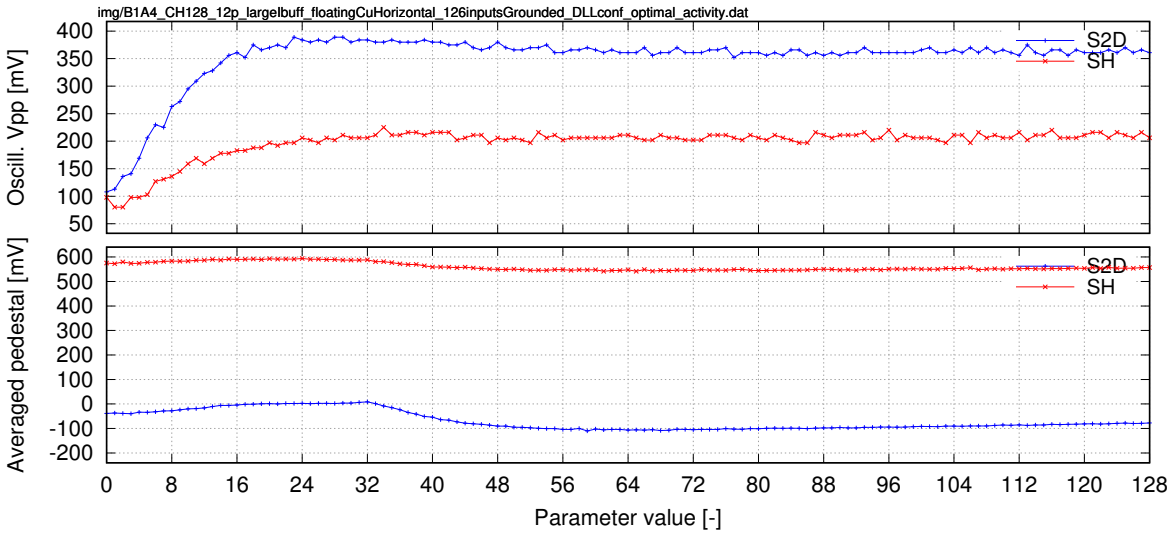

Figure 119: B1A4, channel 128, cap-PCB bonded, 12 pF capacitors; Ibuf current maximized; floating small horizontal copper foil on ASIC; All inputs grounded; Preamp GND configuration – only backside. Parameter=no. of active ADCs

5.11.2 Optimized test pulse and ADC delay

ASIC configuration: JC configuration (tables 1 & 2) + test pulse and ADC delay optimizations (table 3).

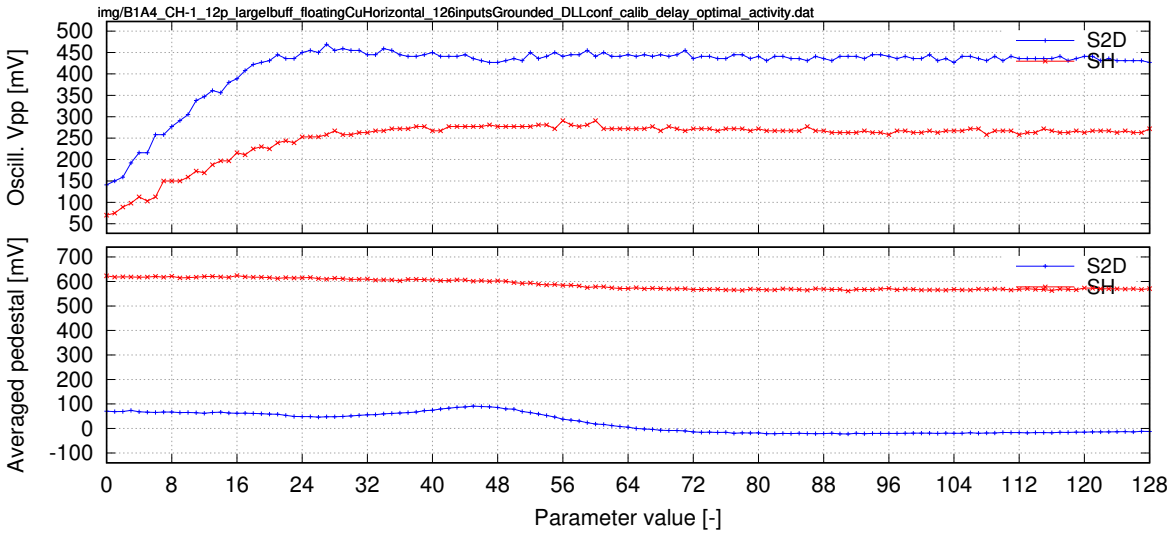

Figure 120: B1A4, channel -1, cap-PCB bonded, 12 pF capacitors; Ibuf current maximized; floating small horizontal copper foil on ASIC; All inputs grounded; Preamp GND configuration – only backside. Optimized test pulse and ADC delay. Parameter=no. of active ADCs

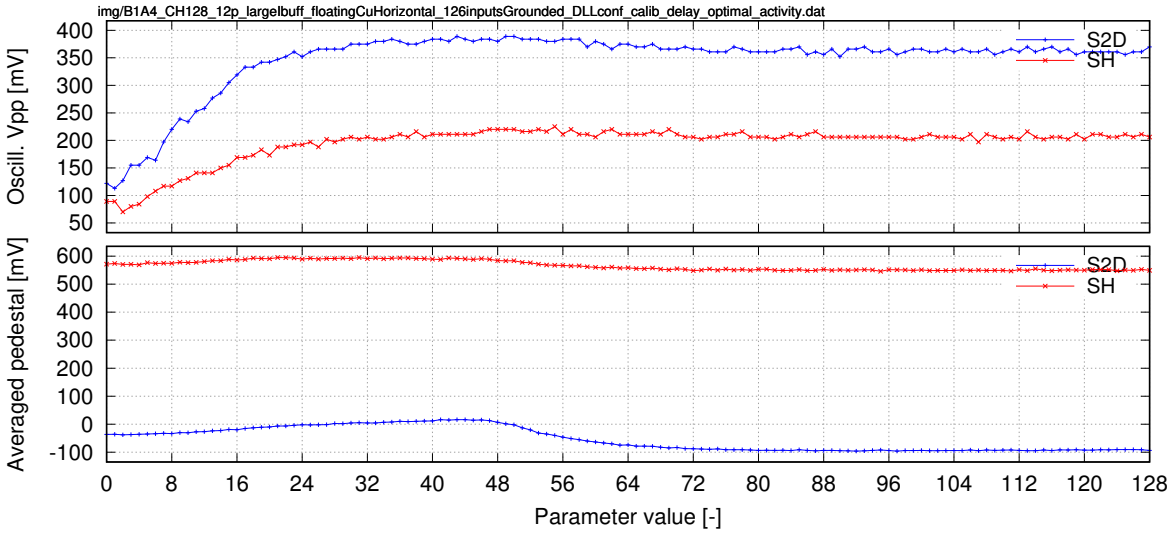

Figure 121: B1A4, channel 128, cap-PCB bonded, 12 pF capacitors; Ibuf current maximized; floating small horizontal copper foil on ASIC; All inputs grounded; Preamp GND configuration – only backside. Optimized test pulse and ADC delay. Parameter=no. of active ADCs

5.12 Cap-PCB bonded, 12 pF capacitors assembled; Ibuf current maximized; floating small horizontal copper foil on ASIC; Preamp GND configuration – only backside

Cap-PCB assembled, bonded to SALT input pads 0 and 127, two 12 pF capacitors assembled to the cap-PCB.
Ibuf current maximized – 1 kΩ resistor between VDDA and Ibuf pad.
Floating small horizontal copper foil glued directly on passivation on top of the ASIC (see figure 151).
Preamp GND bonded only from backside (default pads).

5.12.1 Default ASIC configuration

ASIC configuration: JC configuration (tables 1 & 2).

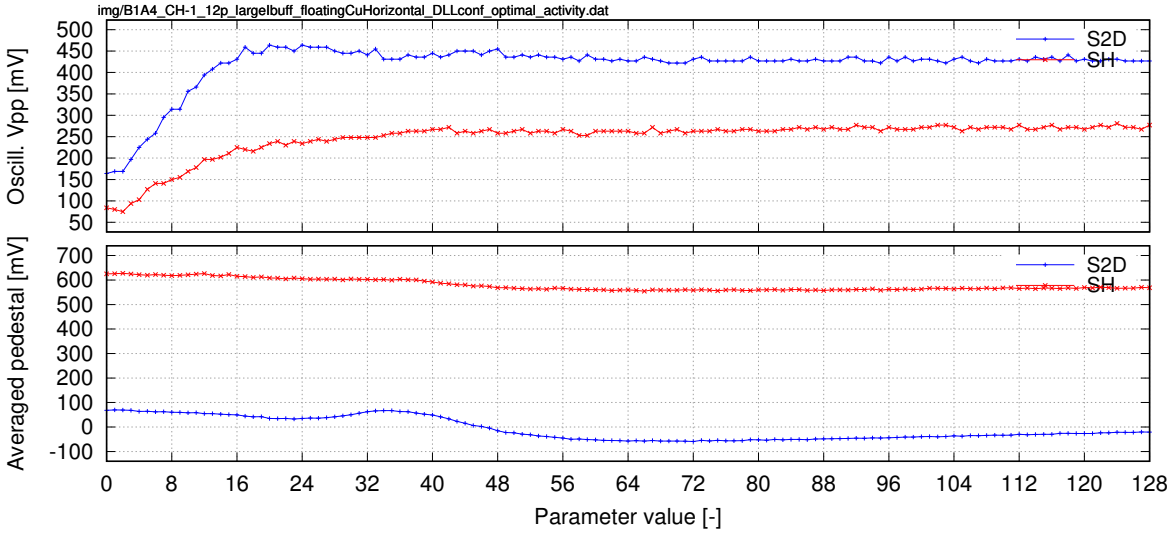

Figure 122: B1A4, channel -1, cap-PCB bonded, 12 pF capacitors; Ibuf current maximized; floating small horizontal copper foil on ASIC; Preamp GND configuration – only backside. Parameter=no. of active ADCs

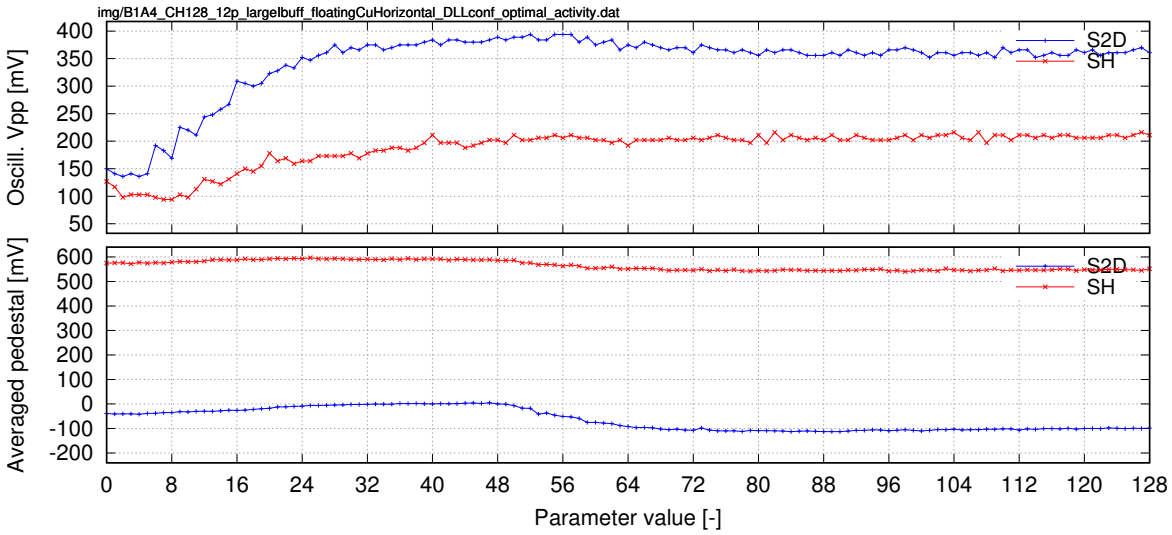

Figure 123: B1A4, channel 128, cap-PCB bonded, 12 pF capacitors; Ibuf current maximized; floating small horizontal copper foil on ASIC; Preamp GND configuration – only backside. Parameter=no. of active ADCs

5.12.2 Optimized test pulse and ADC delay

ASIC configuration: JC configuration (tables 1 & 2) + test pulse and ADC delay optimizations (table 3).

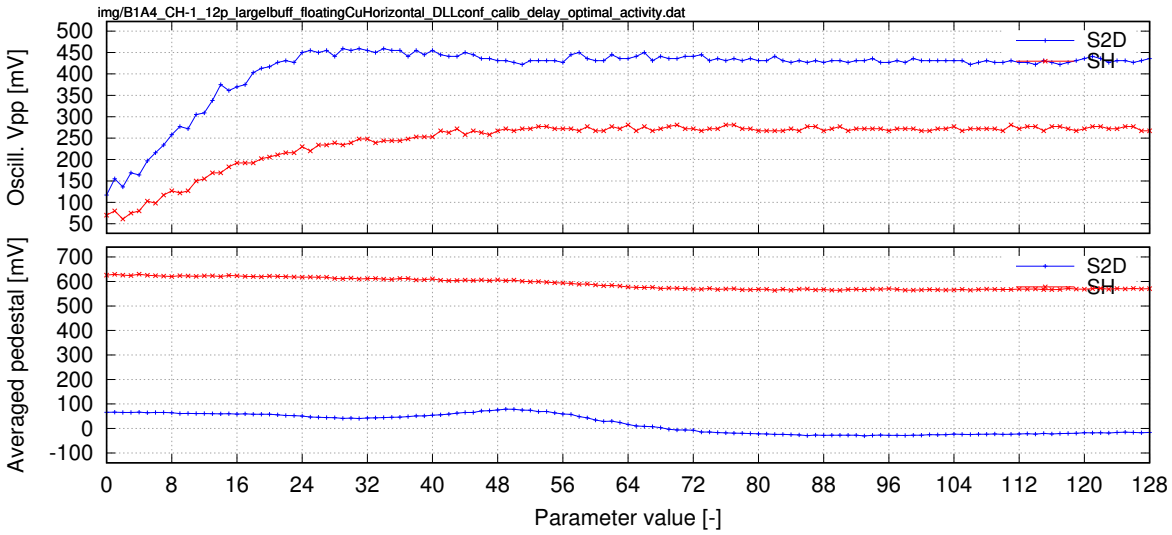

Figure 124: B1A4, channel -1, cap-PCB bonded, 12 pF capacitors; Ibuf current maximized; floating small horizontal copper foil on ASIC; Preamp GND configuration – only backside. Optimized test pulse and ADC delay. Parameter=no. of active ADCs

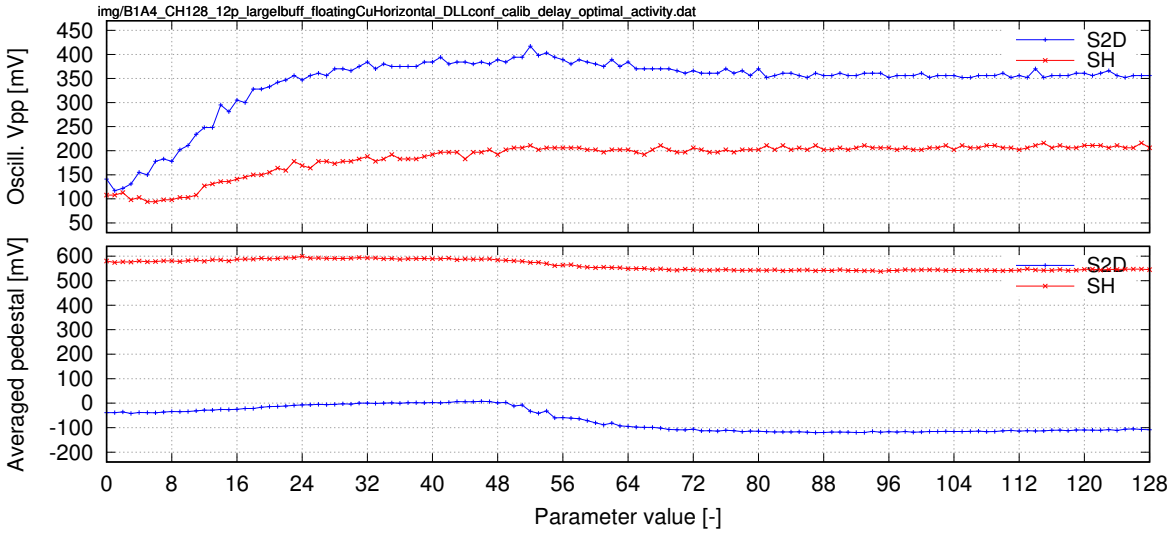

Figure 125: B1A4, channel 128, cap-PCB bonded, 12 pF capacitors; Ibuf current maximized; floating small horizontal copper foil on ASIC; Preamp GND configuration – only backside. Optimized test pulse and ADC delay. Parameter=no. of active ADCs

5.13 Cap-PCB bonded, 12 pF capacitors assembled; Ibuf current maximized; Results comparison

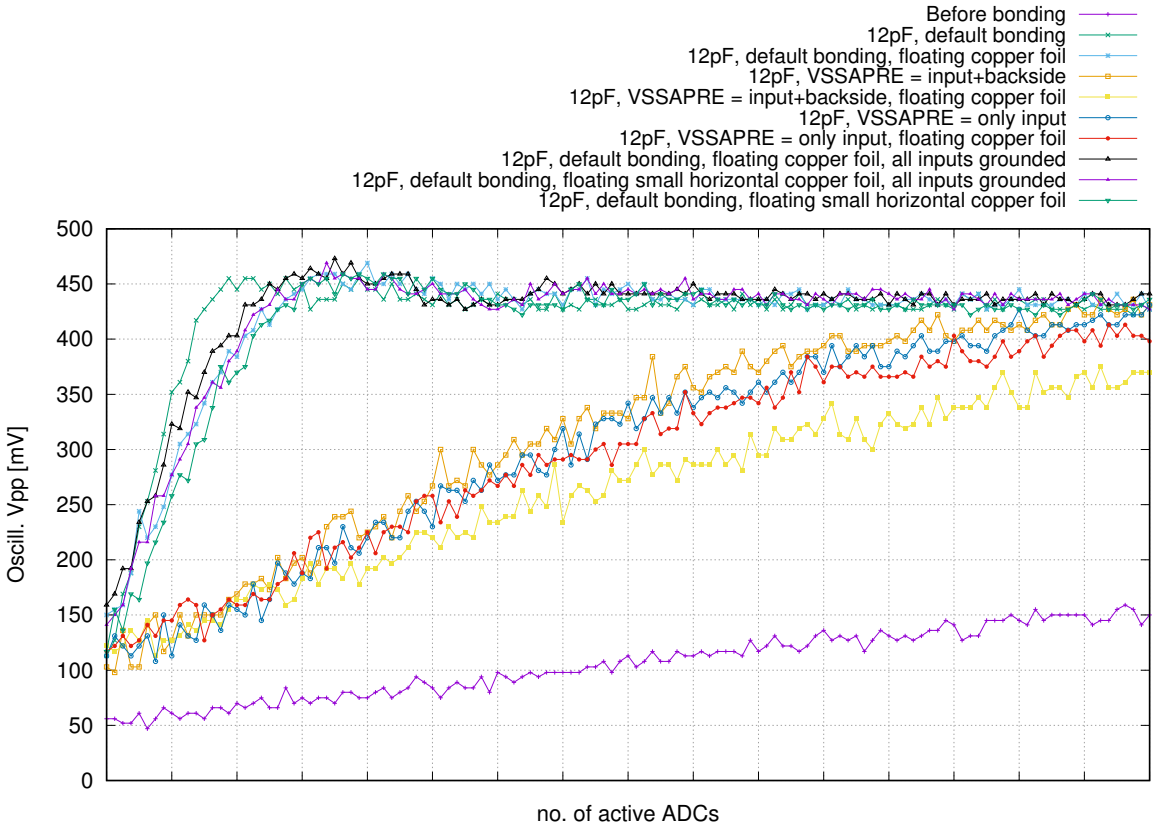

Figure 126: B1A4, channel -1, cap-PCB bonded, 12 pF capacitors; Ibuf current maximized. Optimized test pulse and ADC delay.

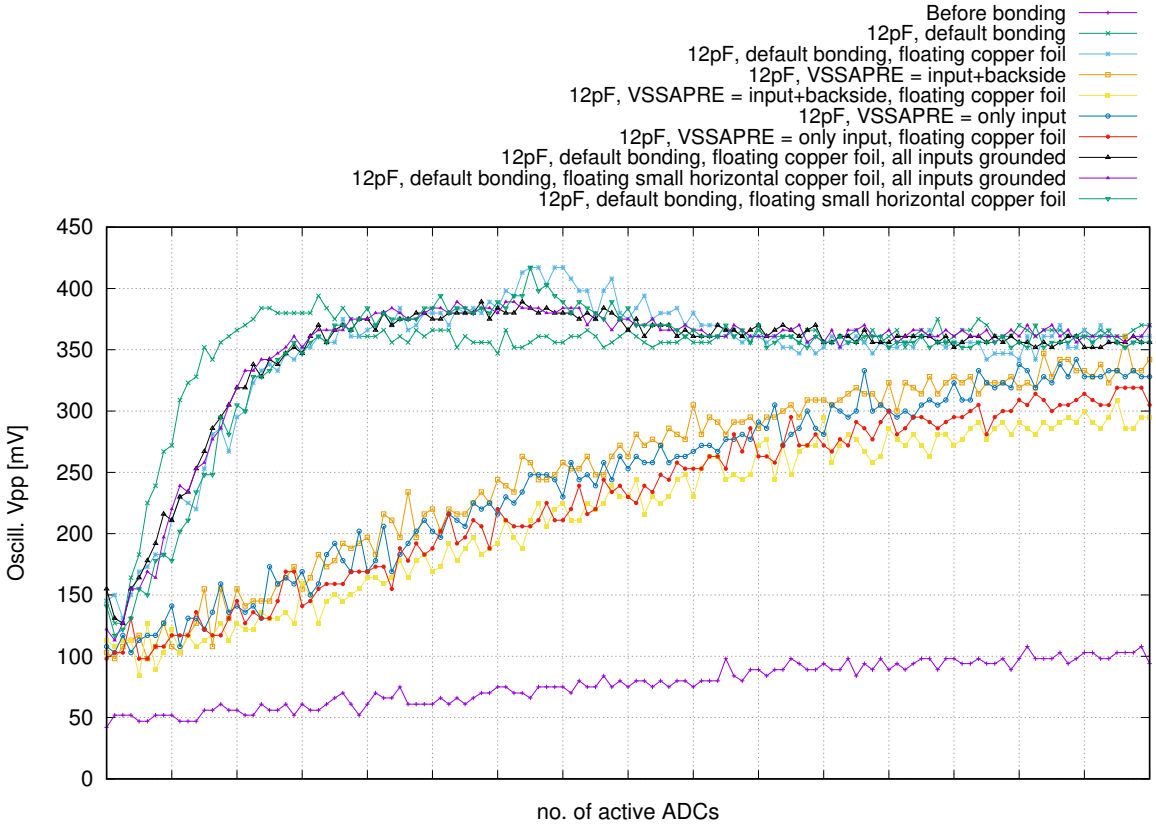

Figure 127: B1A4, channel 128, cap-PCB bonded, 12 pF capacitors; Ibuf current maximized. Optimized test pulse and ADC delay.

6 Board 1 with ASIC 5

6.1 Cap-PCB bonded, 12 pF capacitors assembled; Ibuf current maximized

Cap-PCB assembled, bonded to SALT input pads 0 and 127, two 12 pF capacitors assembled to the cap-PCB.
Ibuf current maximized.

6.1.1 Default ASIC configuration

ASIC configuration: JC configuration (tables 1 & 2).

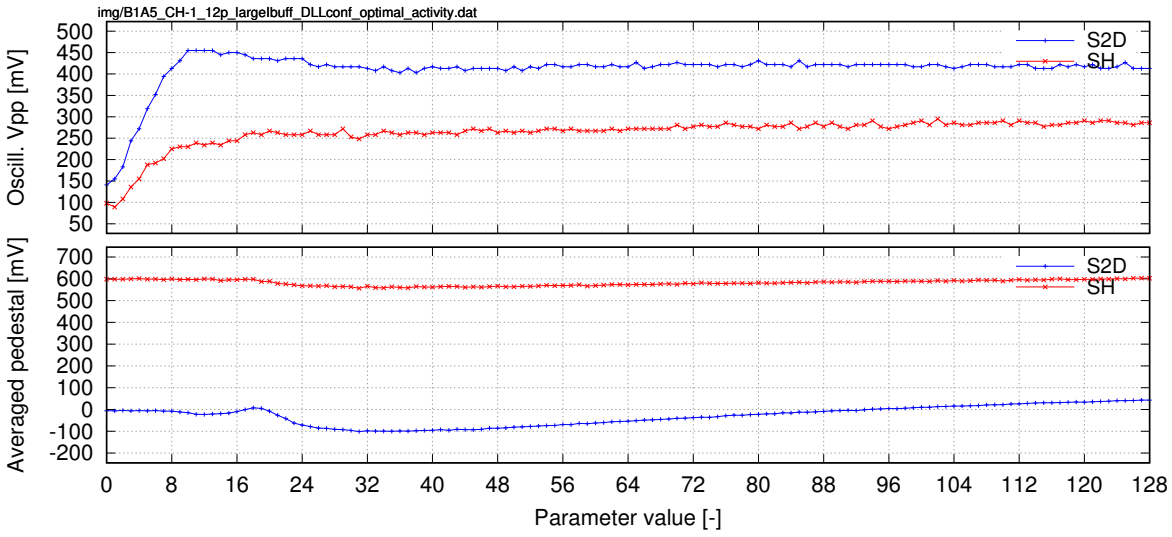

Figure 128: B1A5, channel -1, cap-PCB bonded, 12 pF capacitors; Ibuf current maximized. Parameter=no. of active ADCs

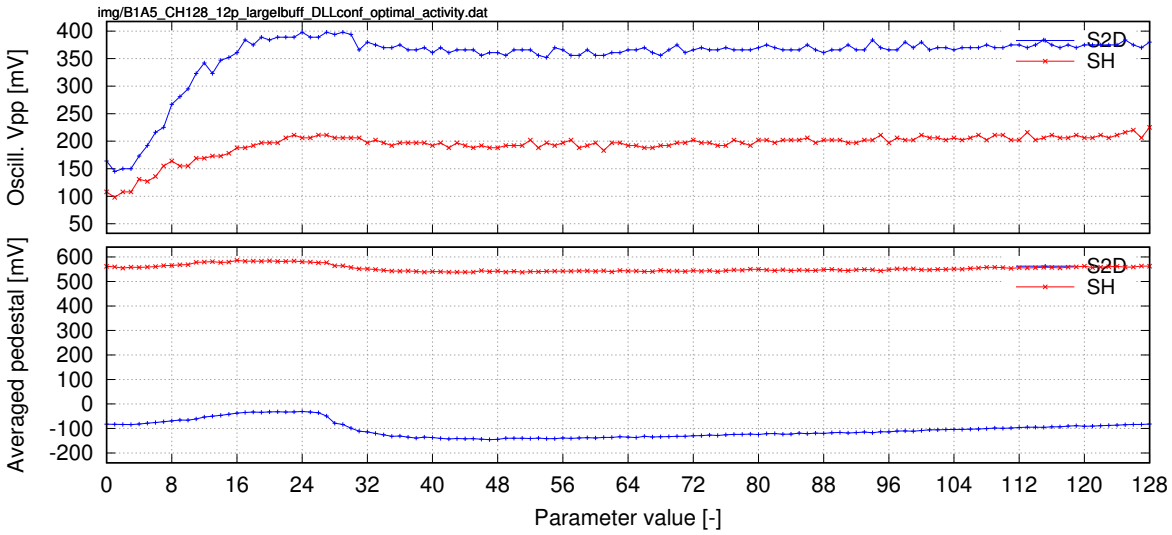

Figure 129: B1A5, channel 128, cap-PCB bonded, 12 pF capacitors; Ibuf current maximized. Parameter=no. of active ADCs

6.1.2 Optimized test pulse and ADC delay

ASIC configuration: JC configuration (tables 1 & 2) + test pulse and ADC delay optimizations (table 3).

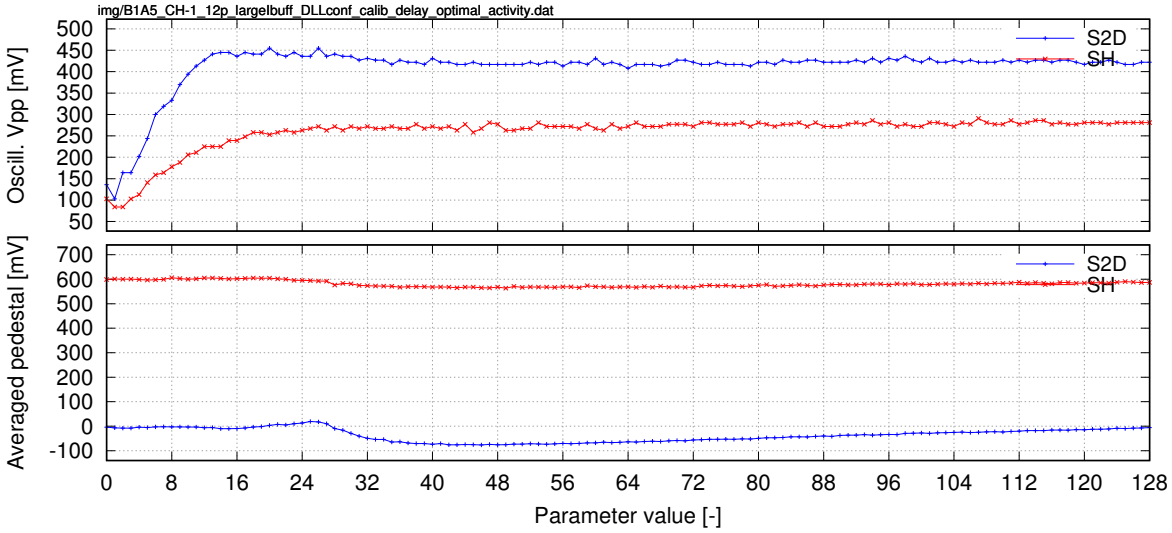

Figure 130: B1A5, channel -1, cap-PCB bonded, 12 pF capacitors; Ibuf current maximized. Optimized test pulse and ADC delay. Parameter=no. of active ADCs

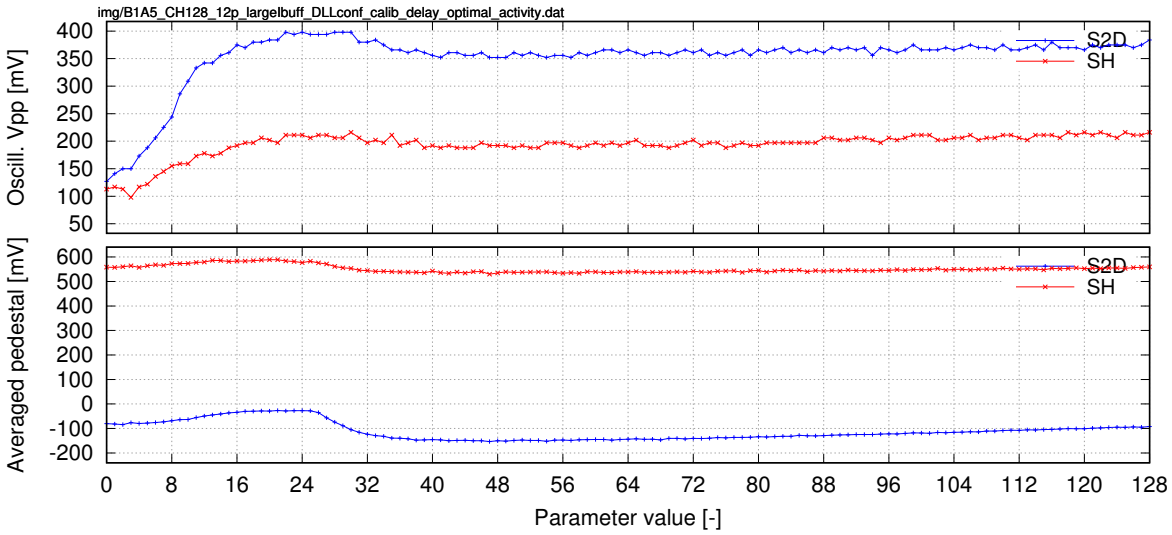

Figure 131: B1A5, channel 128, cap-PCB bonded, 12 pF capacitors; Ibuf current maximized. Optimized test pulse and ADC delay. Parameter=no. of active ADCs

6.1.3 ASIC response for EMI source

ASIC configuration: default (chip after reset), EMI source 152 over the ASIC.

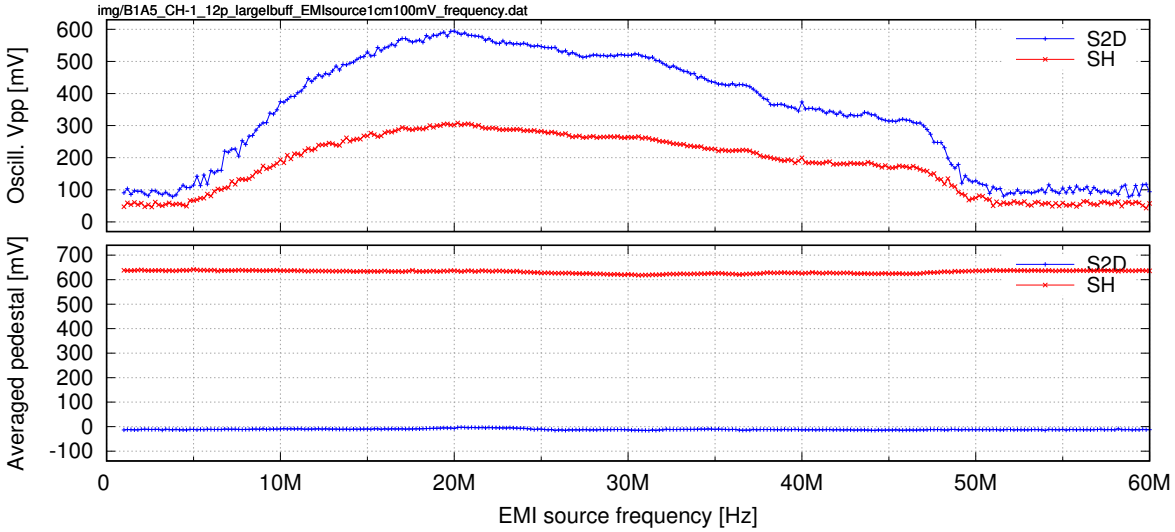

Figure 132: B1A5, channel -1, cap-PCB bonded, 12 pF capacitors; Ibuf current maximized. EMI source 1cm over ASIC, amplitude 100mV. Parameter=frequency of EMI source

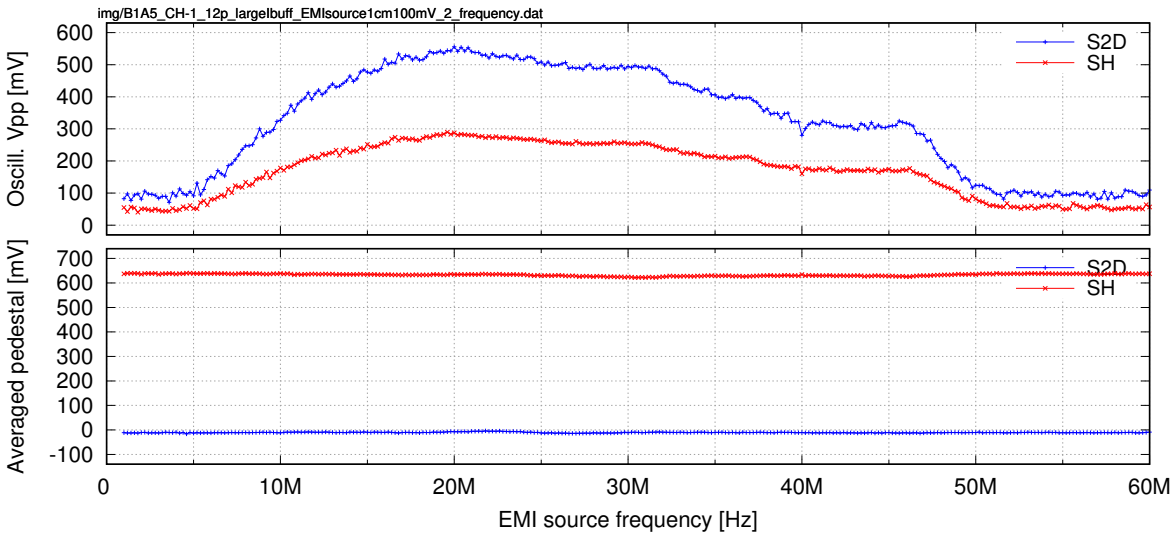

Figure 133: B1A5, channel -1 (second measurement), cap-PCB bonded, 12 pF capacitors; Ibuf current maximized. EMI source 1cm over ASIC, amplitude 100mV. Parameter=frequency of EMI source

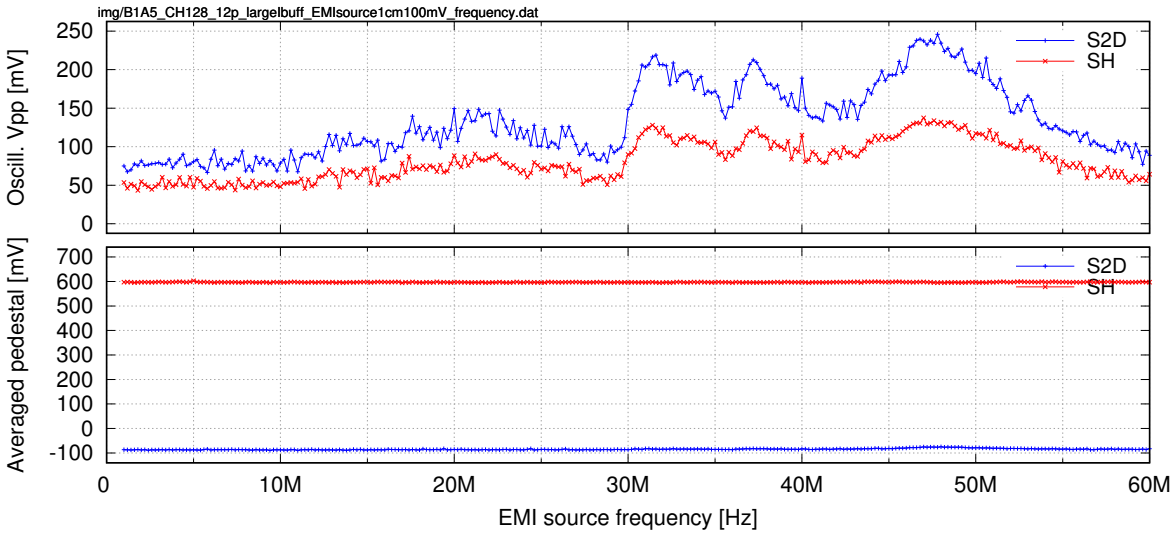

Figure 134: B1A5, channel 128, cap-PCB bonded, 12 pF capacitors; Ibuf current maximized. EMI source 1cm over ASIC, amplitude 100mV. Parameter=frequency of EMI source

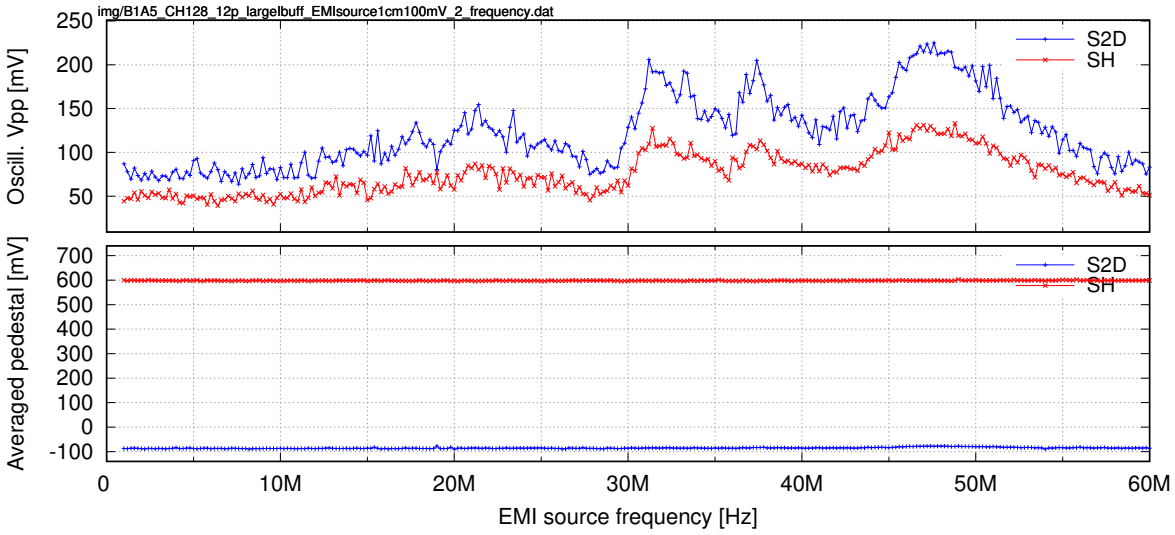

Figure 135: B1A5, channel 128 (second measurement), cap-PCB bonded, 12 pF capacitors; Ibuf current maximized. EMI source 1cm over ASIC, amplitude 100mV. Parameter=frequency of EMI source

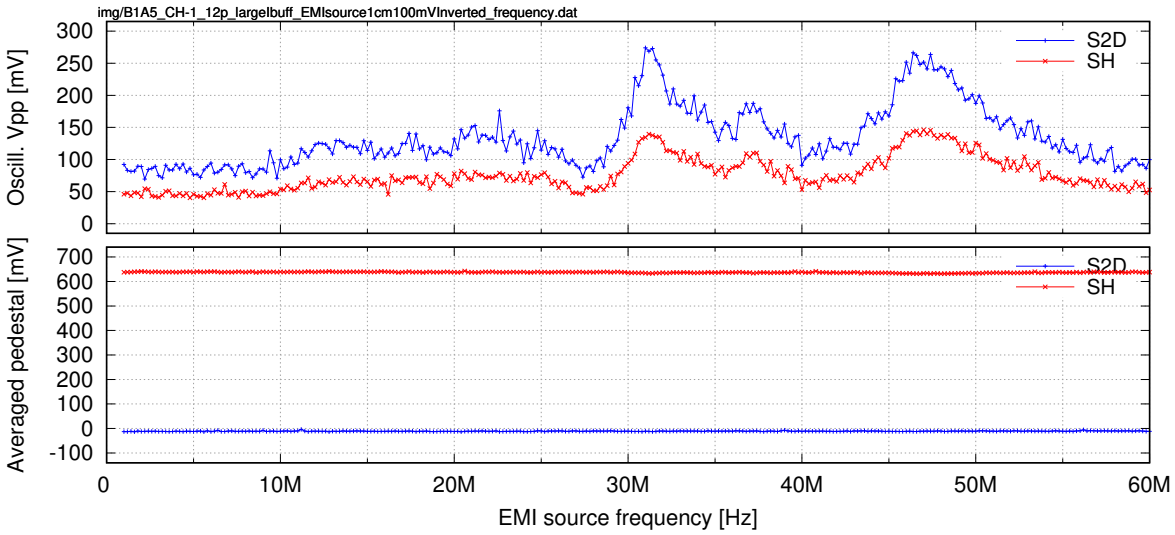

Figure 136: B1A5, channel -1 (inverted polarity of EMI source), cap-PCB bonded, 12 pF capacitors; Ibuf current maximized. EMI source 1cm over ASIC, amplitude 100mV. Parameter=frequency of EMI source

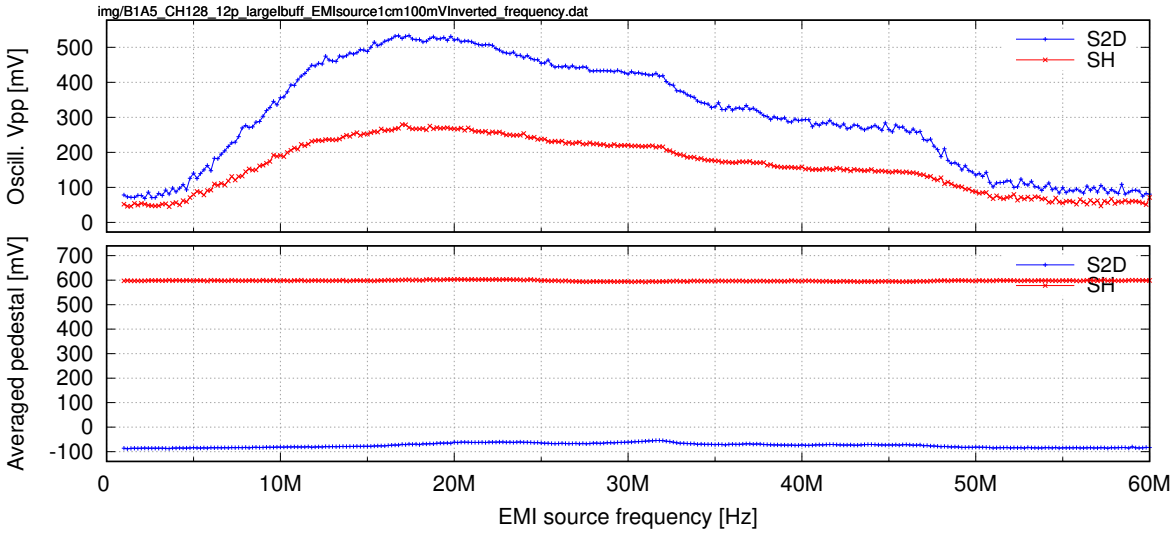

Figure 137: B1A5, channel 128 (inverted polarity of EMI source), cap-PCB bonded, 12 pF capacitors; Ibuf current maximized. EMI source 1cm over ASIC, amplitude 100mV. Parameter=frequency of EMI source

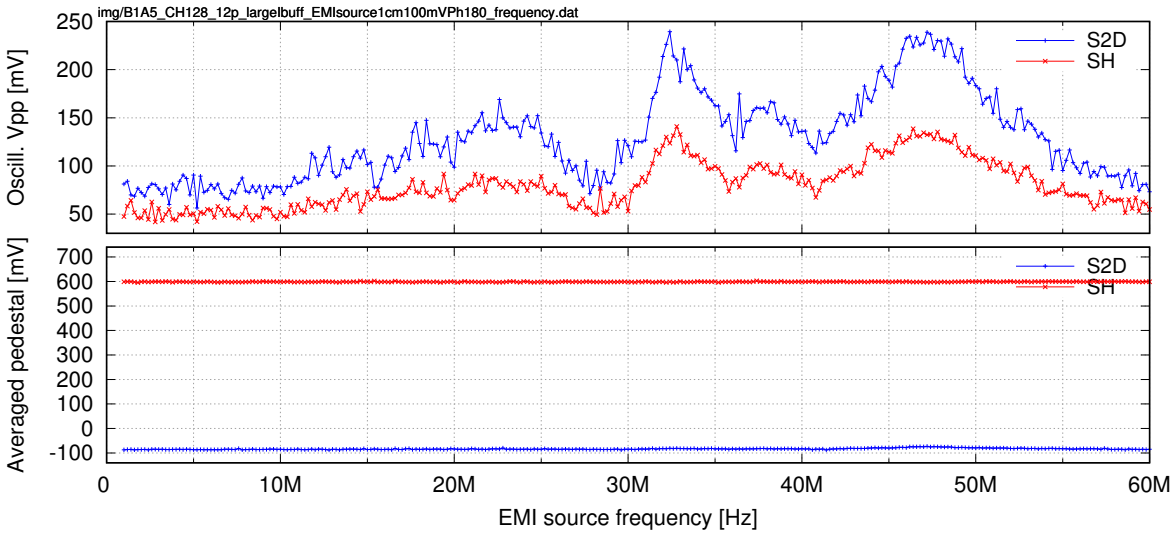

Figure 138: B1A5, channel 128 (inverted phase (180 deg.) of EMI source), cap-PCB bonded, 12 pF capacitors; Ibuf current maximized. EMI source 1cm over ASIC, amplitude 100mV. Parameter=frequency of EMI source

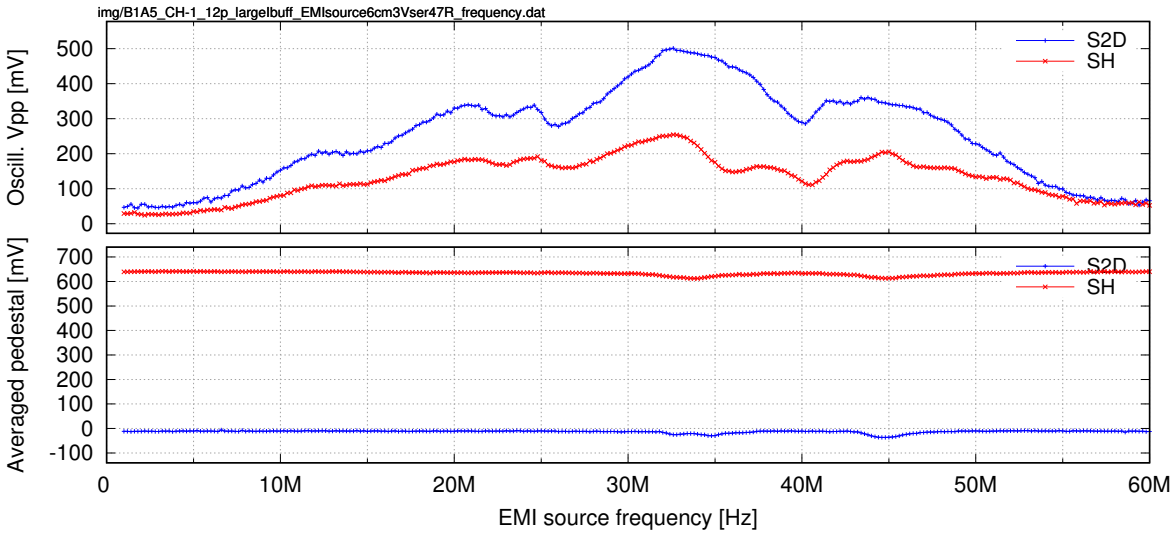

Figure 139: B1A5, channel -1, cap-PCB bonded, 12 pF capacitors; Ibuf current maximized. EMI source (47 Ω serial resistance added) 6cm over ASIC, amplitude 3V. Parameter=frequency of EMI source

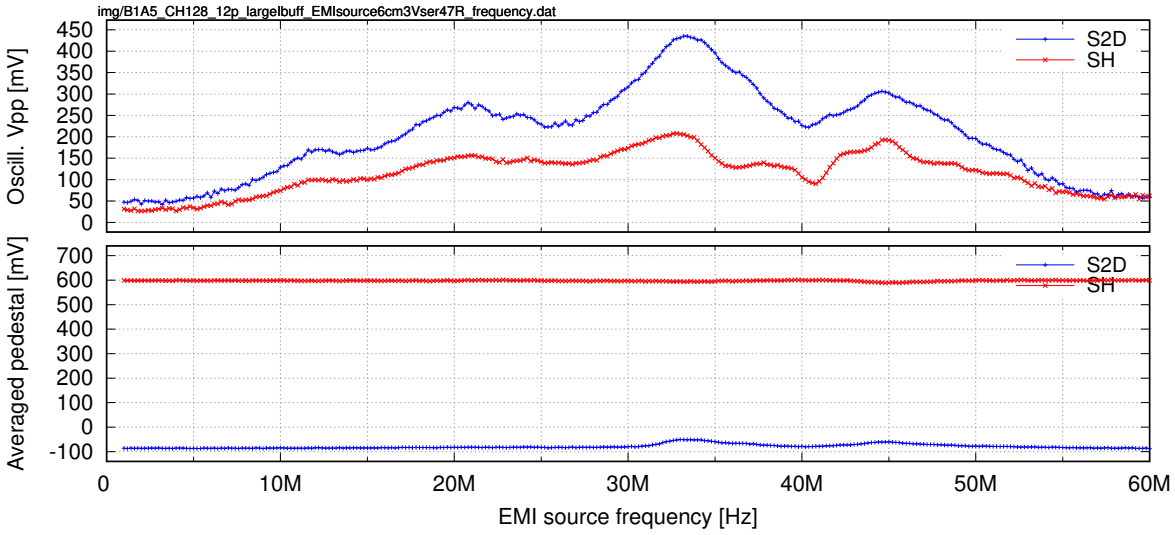

Figure 140: B1A5, channel 128, cap-PCB bonded, 12 pF capacitors; Ibuf current maximized. EMI source (47 Ω serial resistance added) 6cm over ASIC, amplitude 3V. Parameter=frequency of EMI source

6.2 Cap-PCB bonded, 12 pF capacitors assembled; Ibuf current maximized; Preamp GND configuration – input + backside

Cap-PCB assembled, bonded to SALT input pads 0 and 127, two 12 pF capacitors assembled to the cap-PCB.
Ibuf current maximized.
Preamp GND bonded from both sides - input pads + backside (default) pads.

6.2.1 ASIC response for EMI source

ASIC configuration: default (chip after reset), EMI source 152 over the ASIC.

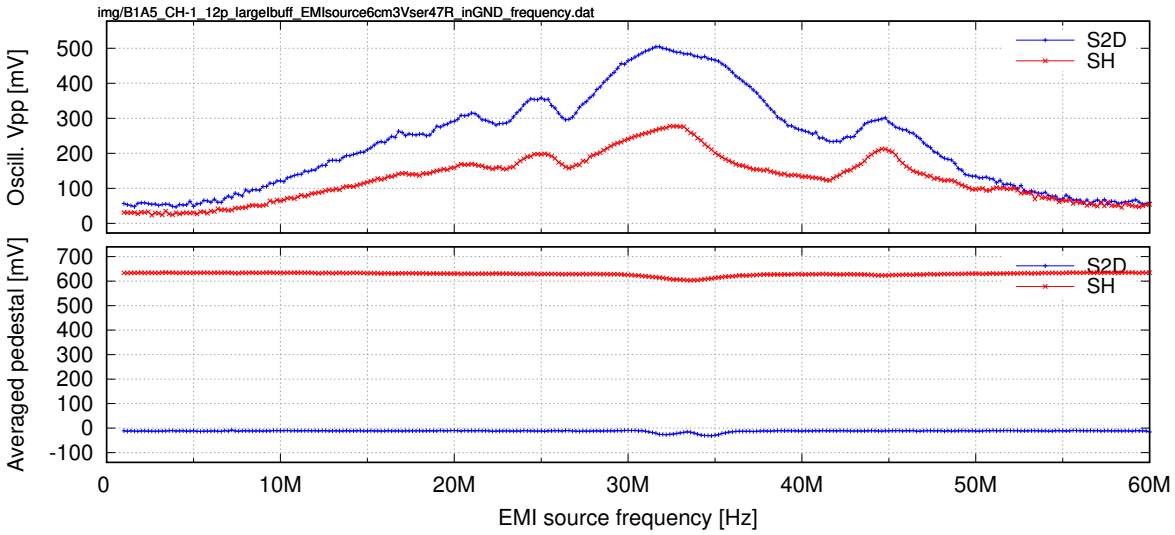

Figure 141: B1A5, channel -1, cap-PCB bonded, 12 pF capacitors; Ibuf current maximized. EMI source (47 Ω serial resistance added) 6cm over ASIC, amplitude 3V. Preamp GND configuration – input + backside. Parameter=frequency of EMI source

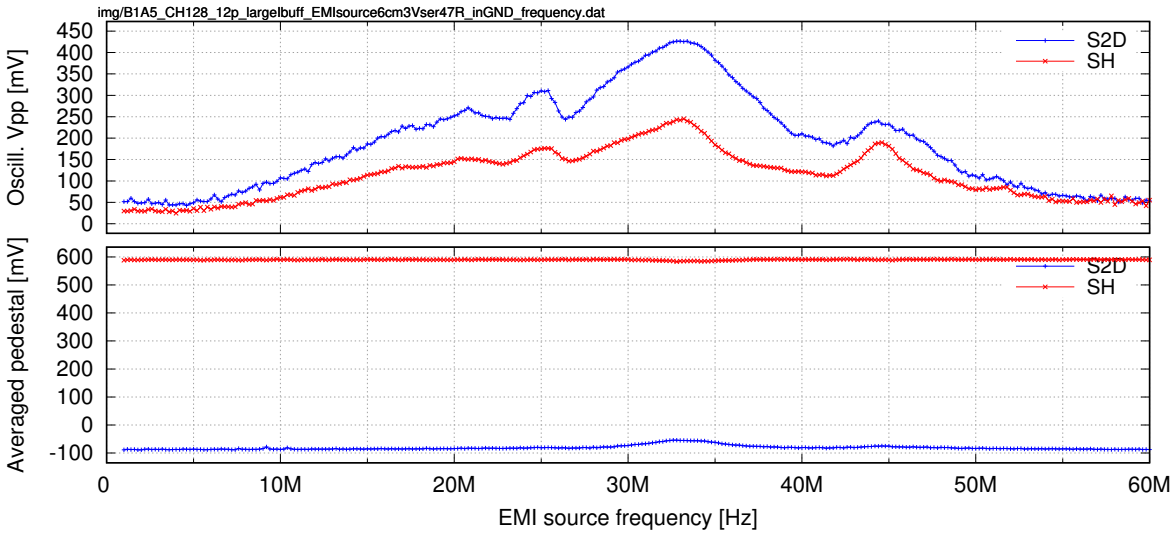

Figure 142: B1A5, channel 128, cap-PCB bonded, 12 pF capacitors; Ibuf current maximized. EMI source (47 Ω serial resistance added) 6cm over ASIC, amplitude 3V. Preamp GND configuration – input + backside. Parameter=frequency of EMI source

6.3 Cap-PCB bonded, 12 pF capacitors assembled; Ibuf current maximized; Preamp GND configuration – only input

Cap-PCB assembled, bonded to SALT input pads 0 and 127, two 12 pF capacitors assembled to the cap-PCB.
Ibuf current maximized.
Preamp GND bonded only using input pads.

6.3.1 ASIC response for EMI source

ASIC configuration: default (chip after reset), EMI source 152 over the ASIC.

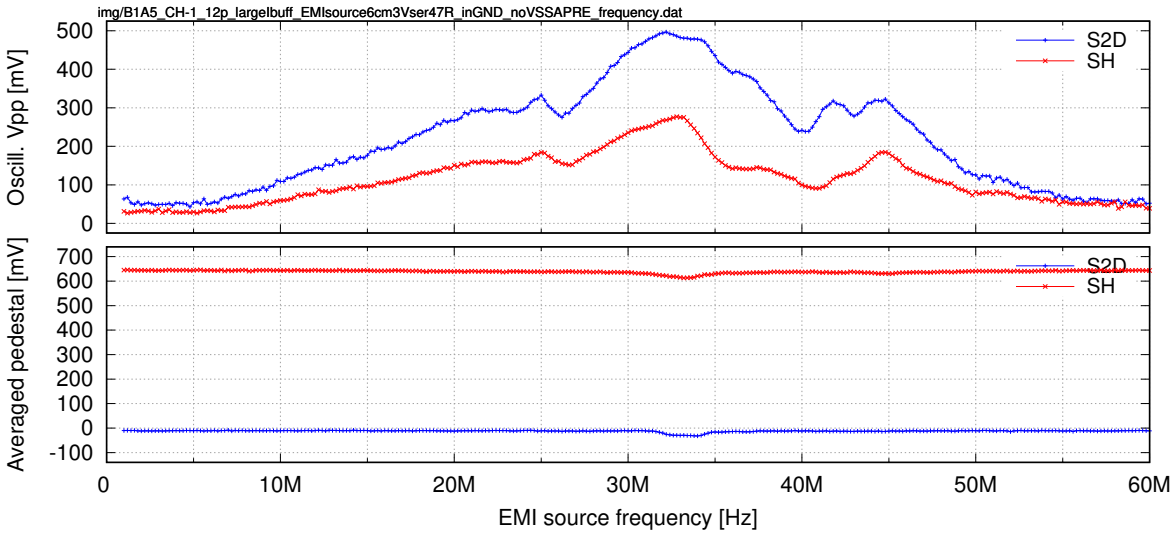

Figure 143: B1A5, channel -1, cap-PCB bonded, 12 pF capacitors; Ibuf current maximized. EMI source (47 Ω serial resistance added) 6cm over ASIC, amplitude 3V. Preamp GND configuration – only input. Parameter=frequency of EMI source

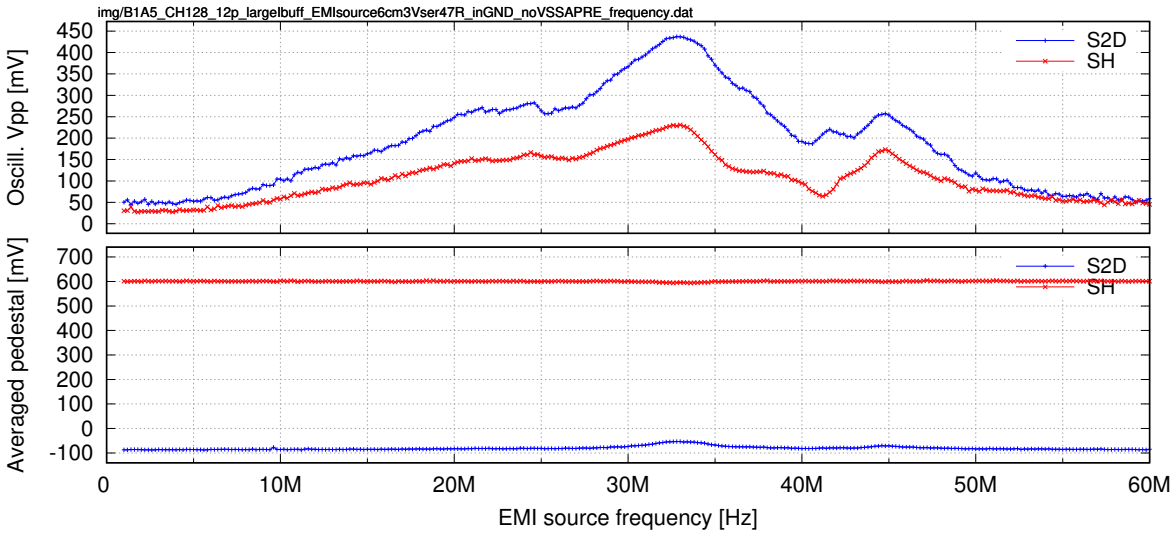

Figure 144: B1A5, channel 128, cap-PCB bonded, 12 pF capacitors; Ibuf current maximized. EMI source (47 Ω serial resistance added) 6cm over ASIC, amplitude 3V. Preamp GND configuration – only input. Parameter=frequency of EMI source

7 ASICs history

- B0A0 (Board 0, ASIC 0)
  - ASIC fully functional without cap-PCB;
  - Shortcut between inputs 0 and 128 found with cap-PCB; ESD issue wrongly suspected – short on cap-PCB found later;
  - A real ESD issue on input pads created on probe station – shortcut between middle input pads (around channel 70.) created; probe station was not ESD-safe;
  - ASIC removed.
- B1A1 (Board 1, ASIC 1)
  - ASIC fully functional without and with cap-PCB; full set of measurements done;
  - Input GND bonds added, ASIC still fully functional;
  - ASIC damaged during handling or reconnecting to test setup (boards 0 and 1 exchanging) – no I2C response, the same digital current consumption with or without clock; analogue part still working correctly. No broken bonds found, main CLK SLVS receiver probably damaged on ASIC;
  - ASIC removed.
- B0A2 (Board 0, ASIC 2)
  - Shortcut between inputs 0 and 128 found with cap-PCB; ASIC fully functional after input bonds removing;
  - Short on cap-PCB found and removed;
  - Channel 128 damaged after re-bonding inputs to modified cap-PCB; channel -1 operating correctly;
  - Backside ADC power supply scheme changed – 2.2 Ω resistor added in series;
  - Backside ADC power supply scheme changed – 1 μH inductor added in series;
  - Floating copper foil glued directly on passivation on top of the ASIC (see figure 149);
- B1A3 (Board 1, ASIC 3)
  - ASIC damaged after assembly; 800 mA of analogue current consumption measured (instead of around 200 mA); 0.55 Ω measured between VDDA and GND; bonding issues (see section 8.1) could be a possible reason;
  - Digital part functional – I2C communication working, digital current consumption depends on main CLK as expected;

  - Around 150 mV at shaper outputs measured – analogue part not working correctly;
  - No damaged, shorted or misplaced bonds found; analogue current consumption dropped to zero after all analogue power supply bonds removed – no short on PCB board, huge current consumption caused only by ASIC
  - ASIC removed.

- B1A4 (Board 1, ASIC 4)
  - ASIC fully functional without cap-PCB; ASIC corner damaged (see fig. 145);
  - Cap-PCB assembled and bonded, ASIC fully functional. Some slightly damaged bondpads found – see section 8.1;
  - Analogue current consumption typical, huge current consumption on digital power supply
  - ASIC removed.

- B1A5 (Board 1, ASIC 5)
  - Cap-PCB with 12 pF assembled and bonded, ASIC fully functional.

8 Various issues

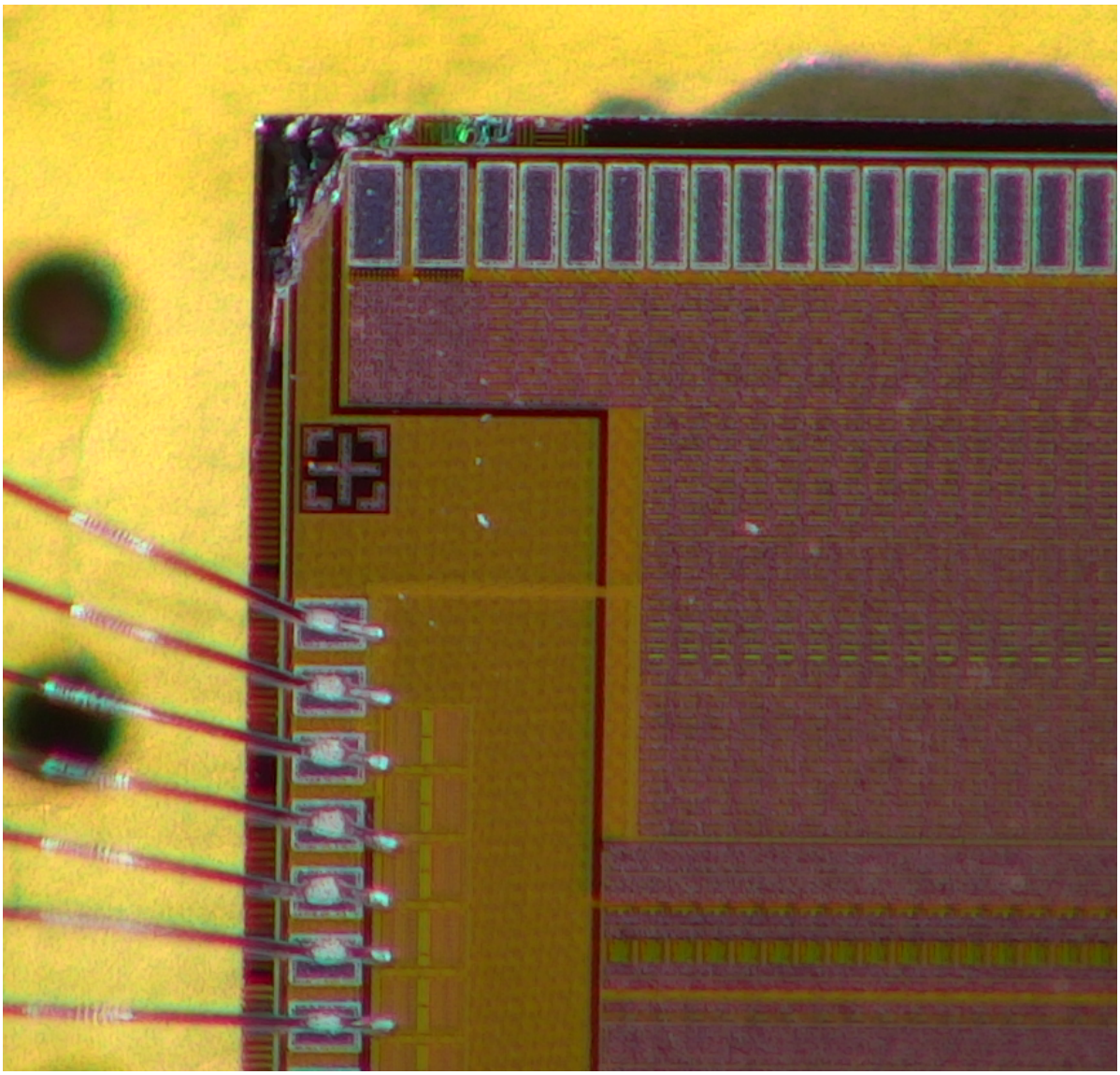

Figure 145: Damaged corner of ASIC 4

8.1 Bonding issue at AGH-UST

Bonding issue found during ASIC 4 assembly – some of the bonds are partially damaged and bondpads are deeply scratched.

Probably to much pressure used during bonding caused the bondpad surface to bend. The edge of the deflection cuts out the tail of the bonding wire, allowing the bonding needle foot to touch and scratch the bondpad surface (usually the foot should be pressed against the wire and should not touch the bondpad directly).

A very deep scratch was found on one pad at ASIC 4 (see figure 148). The scratch reaches beneath the bondpad into the structures (so called padring) located underneath. In this particular case padring seems to be untouched, however damaging it will most probably cause the shortcut between power supply and ground, which may explain the issue with ASIC 3.

For the next bonding, a modified parameters with less pressure and increased bonding time should be used.

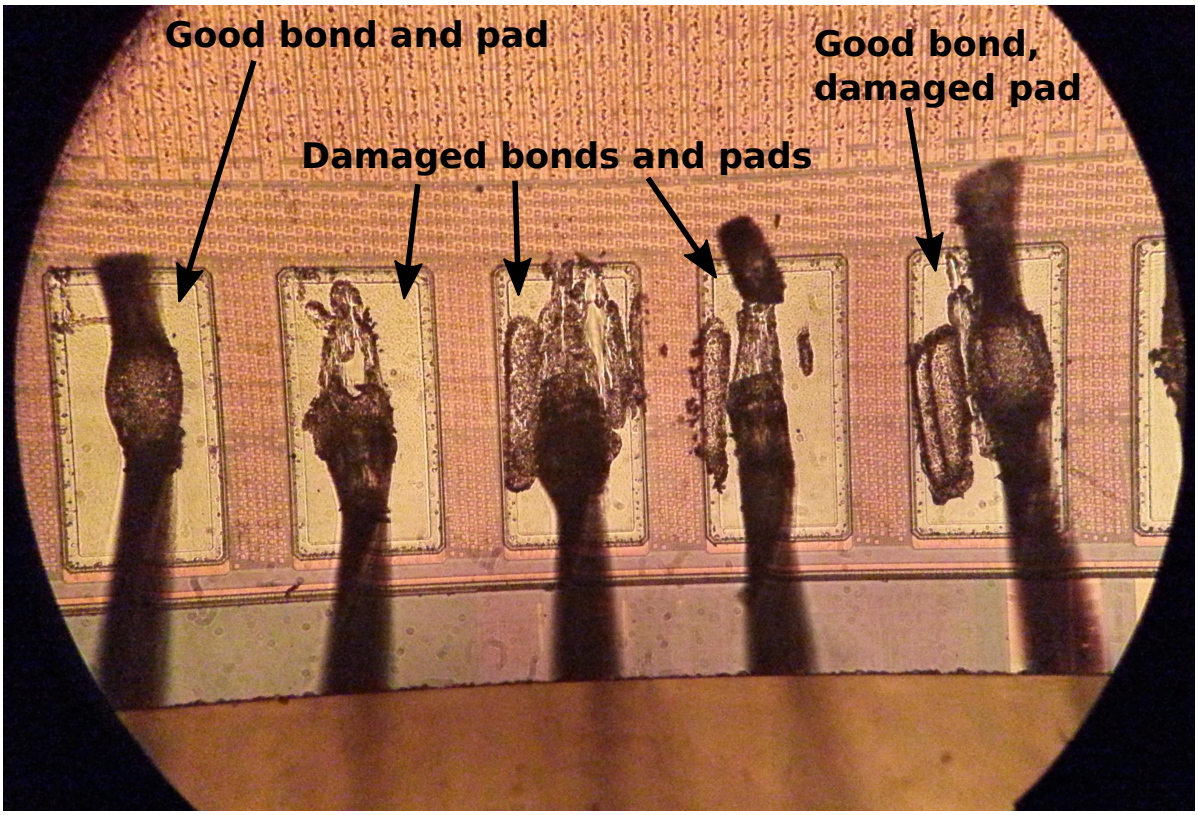

Figure 146: ASIC 4 – Good and damaged bonds and pads

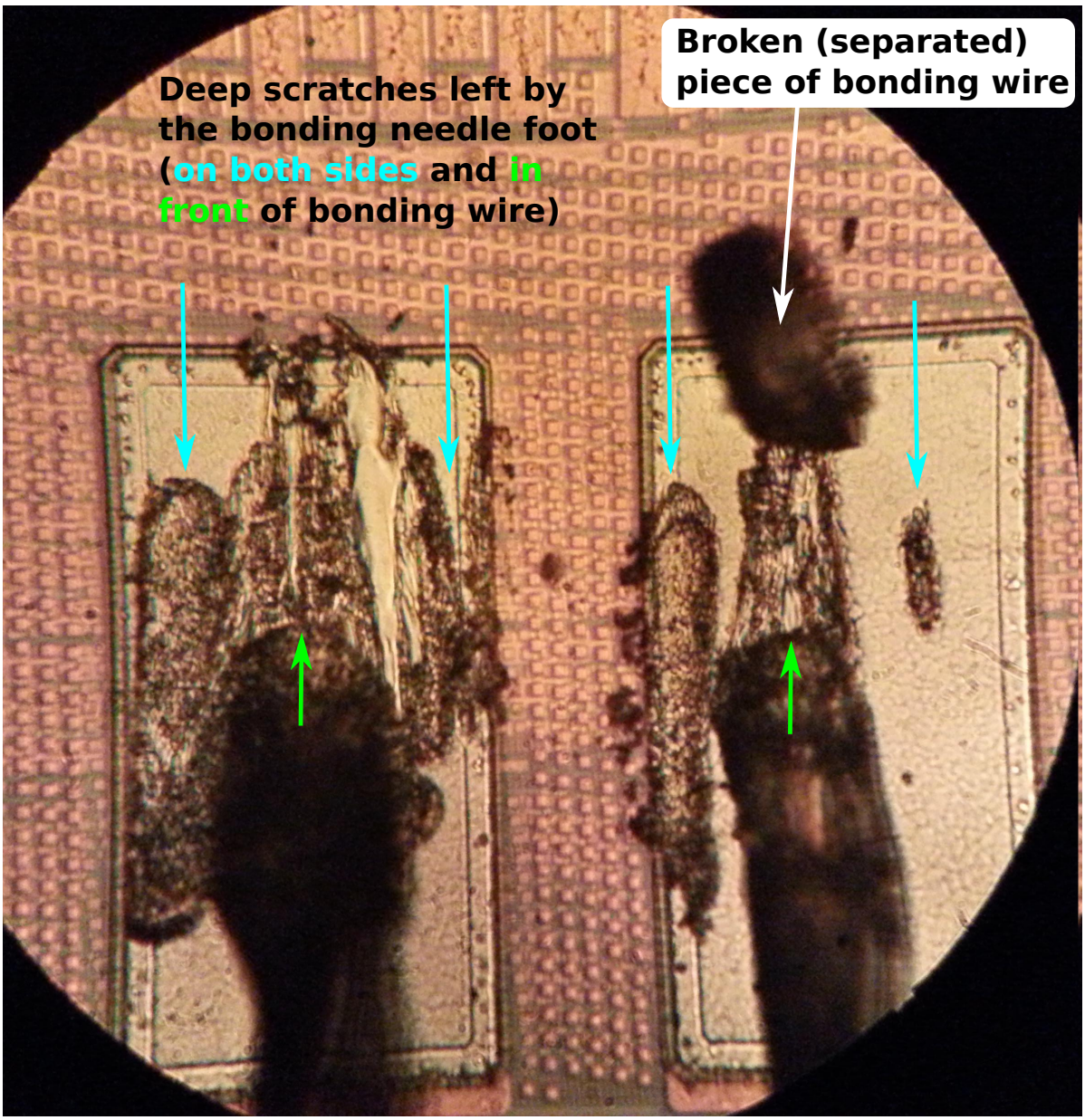

Figure 147: ASIC 4 – Damaged bonds and pads

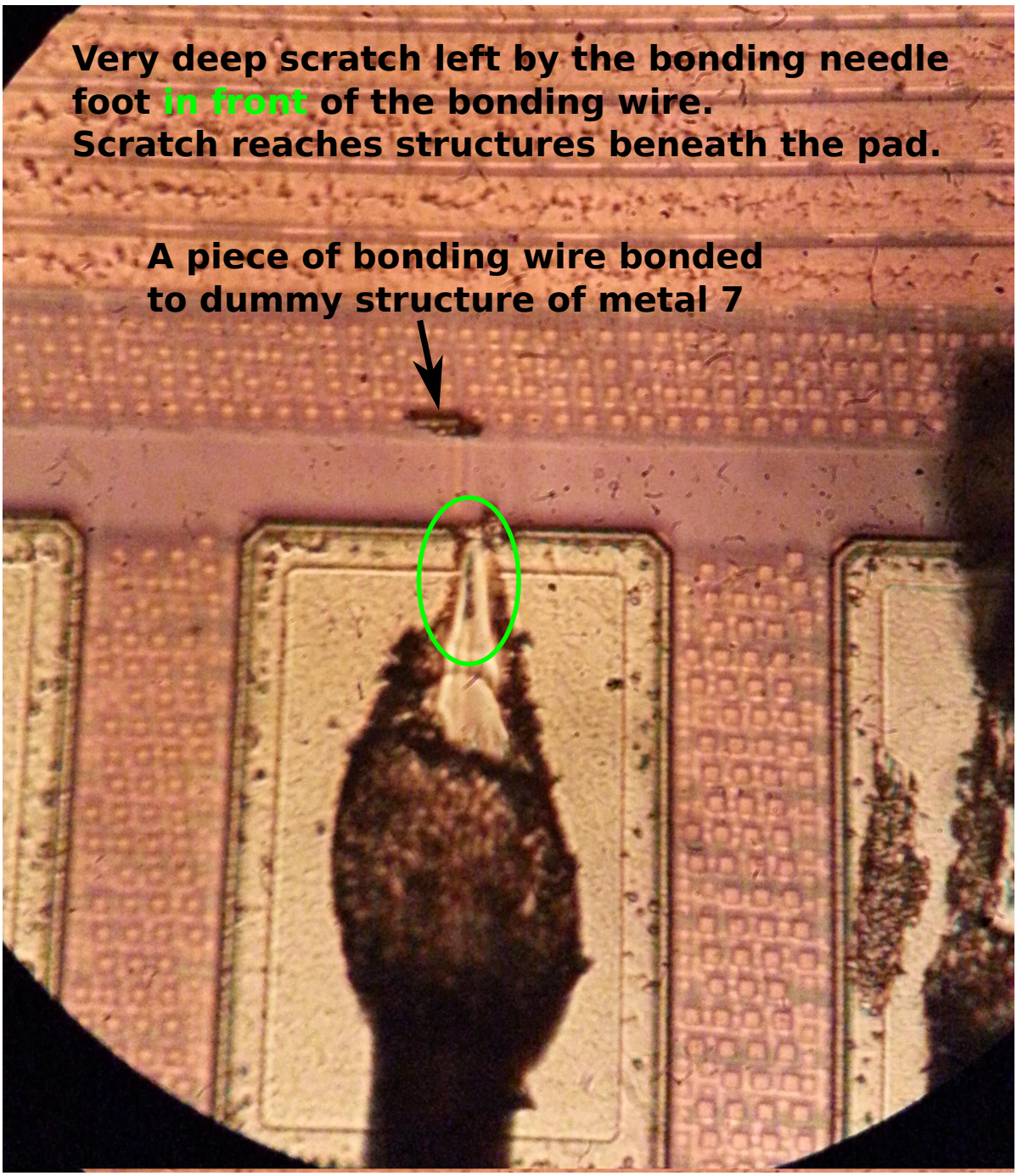

Figure 148: ASIC 4 – Very deep scratch reaching beneath the pad

8.2 Copper foil on ASIC B0A2 and 1 μH inductor assembly

Floating copper foil glued directly on passivation on top of the ASIC.
1 μH inductor assembled in series between onboard decoupling power supply capacitors

and VDDADC + VREFD bonds.

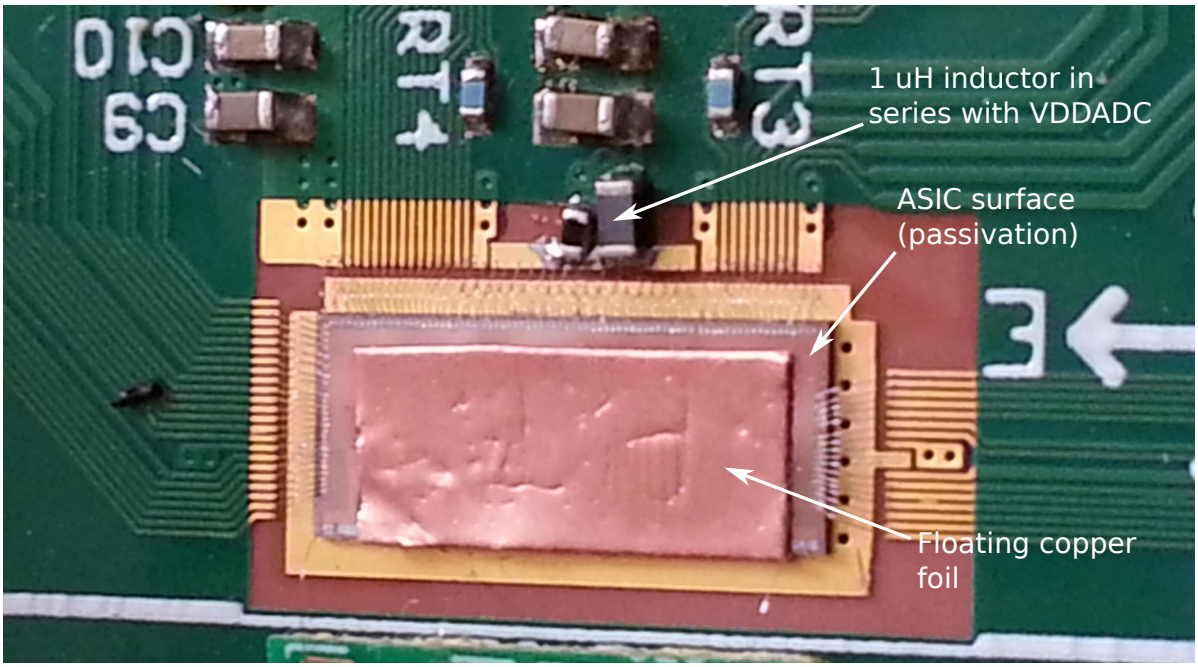

Figure 149: Copper foil on ASIC B0A2 and 1 μH inductor assembly

8.3 Copper foil on ASIC B1A4

Floating copper foil glued directly on passivation on top of the ASIC.

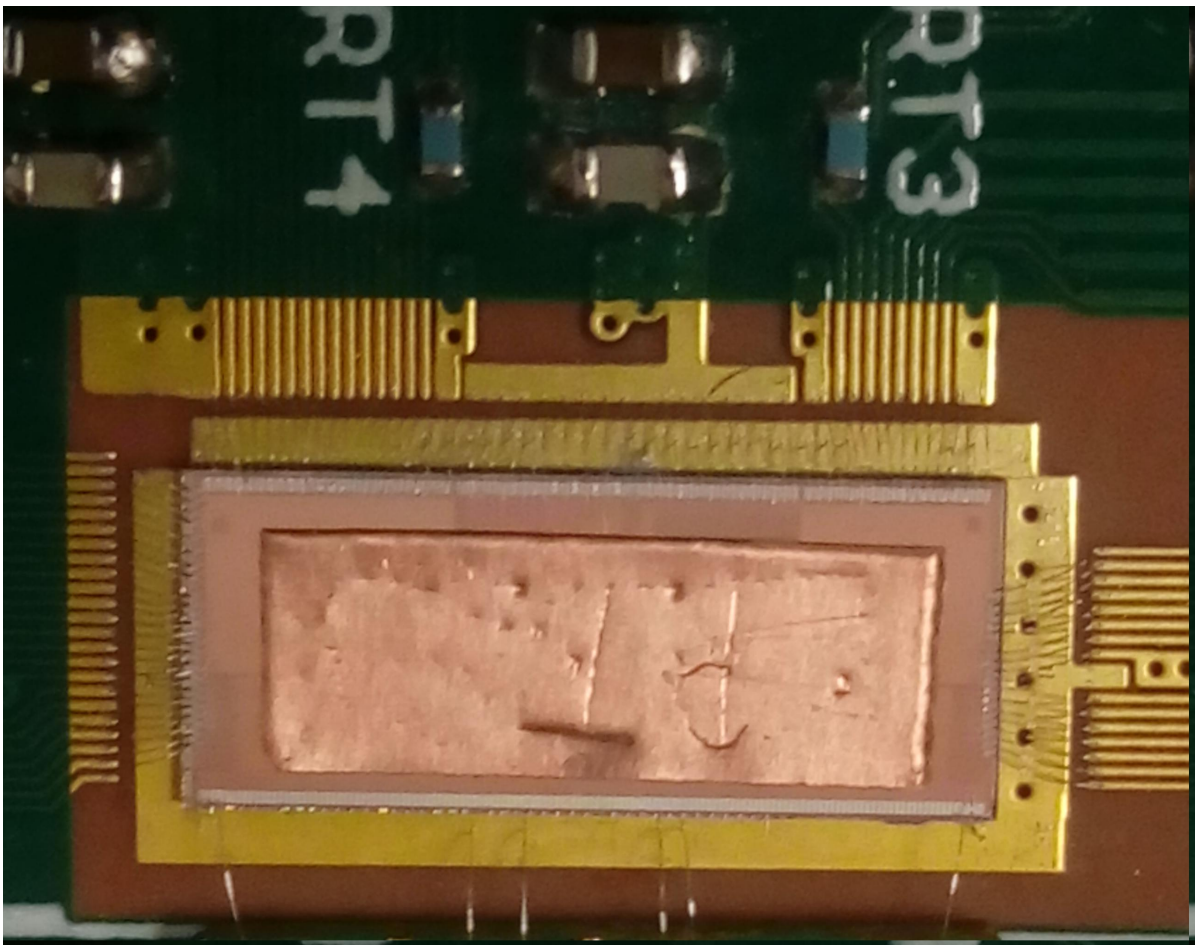

Figure 150: Copper foil on ASIC B1A4

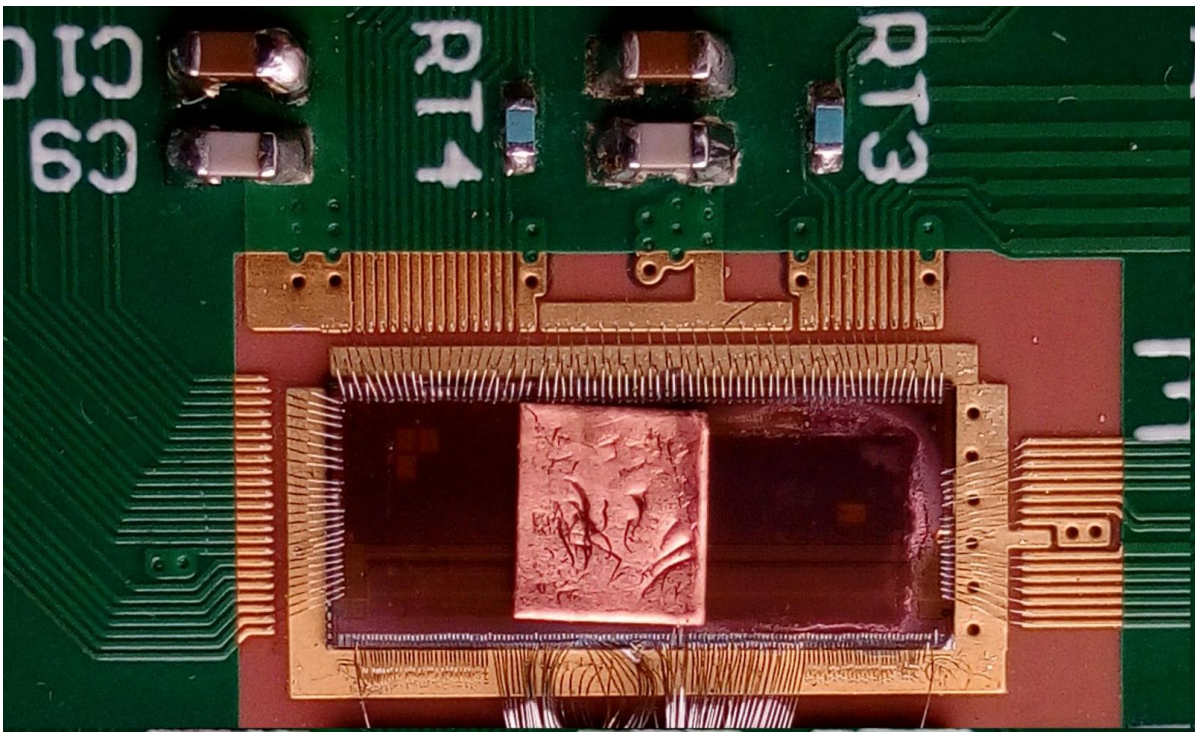

Figure 151: Small horizontal copper foil on ASIC B1A4

8.4 EMI source over ASIC B0A2

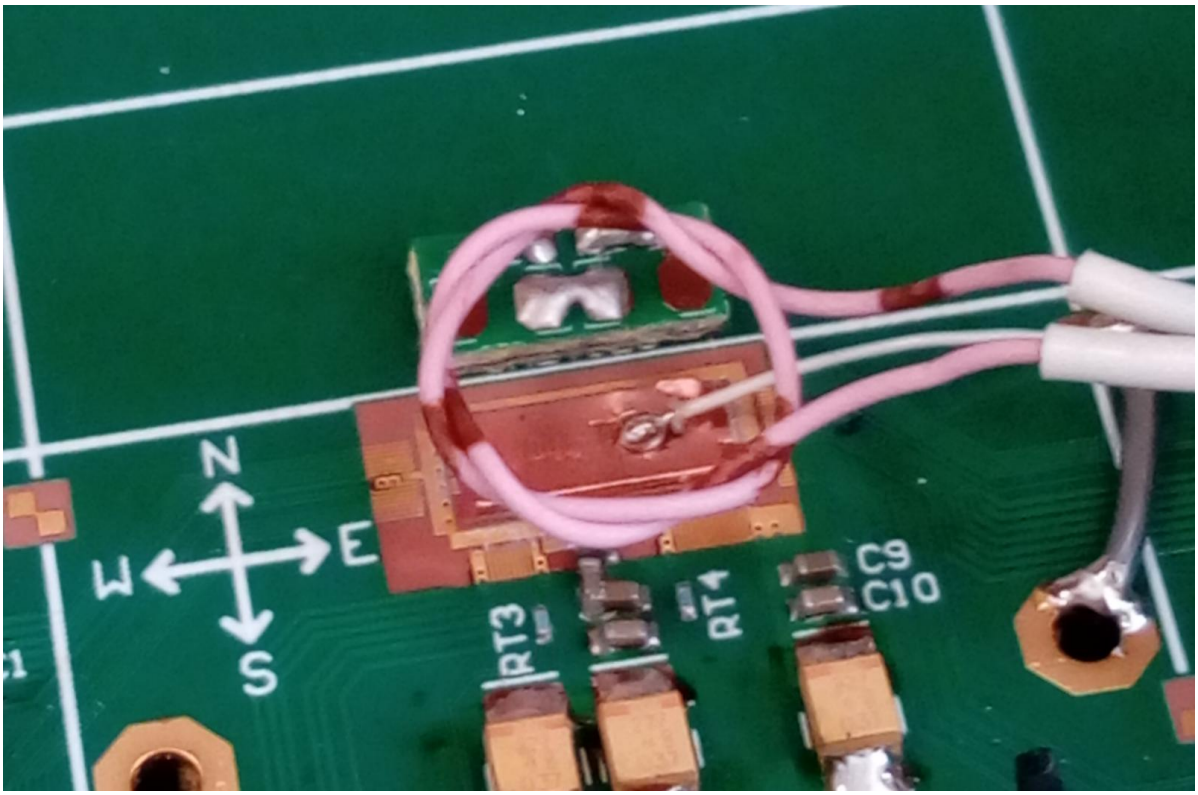

Figure 152: EMI source over ASIC B0A2

List of Figures

1 Input capacitance assembly 9
2 B0A0, channel -1, before bonding. Parameter=no. of active ADCs 10
3 B0A0, channel -1, cap-PCB bonded, 12 pF capacitors assembled. Parameter=no. of active ADCs 11
4 B0A0, channel 128, cap-PCB bonded, 12 pF capacitors assembled, **no data for oscillations**. Parameter=no. of active ADCs 12
5 B0A0, channel -1, cap-PCB bonded, capacitors removed. Parameter=no. of active ADCs 13
6 B0A0, channel 128, cap-PCB bonded, capacitors removed. Parameter=no. of active ADCs 13
7 B0A0, channel -1, cap-PCB bonded, 12 pF capacitors re-assembled. Parameter=no. of active ADCs 14
8 B0A0, channel 128, cap-PCB bonded, 12 pF capacitors re-assembled. Parameter=no. of active ADCs 14
9 B0A0, channel -1, cap-PCB bonded, 12 pF capacitors re-assembled, krum_cfg='h00. Parameter=no. of active ADCs 15
10 B0A0, channel -1, input bonds completely removed. Parameter=no. of active ADCs 16
11 B0A0, channel 128, input bonds completely removed. Parameter=no. of active ADCs 16
12 B1A1, channel -1, before bonding. Parameter=no. of active ADCs 17
13 B1A1, channel 128, before bonding. Parameter=no. of active ADCs . . . 17
14 B1A1, channel -1, dummy bond. Parameter=no. of active ADCs 18
15 B1A1, channel 128, dummy bond. Parameter=no. of active ADCs 18
16 B1A1, channel -1, Empty cap-PCB bonded. Parameter=no. of active ADCs 19
17 B1A1, channel 128, Empty cap-PCB bonded. Parameter=no. of active ADCs 20
18 B1A1, channel -1, Empty cap-PCB bonded. Optimized test pulse and ADC delay. Parameter=no. of active ADCs 20
19 B1A1, channel 128, Empty cap-PCB bonded. Optimized test pulse and ADC delay. Parameter=no. of active ADCs 21
20 B1A1, channel -1, cap-PCB bonded, 2.2 pF capacitors assembled. Parameter=no. of active ADCs 22
21 B1A1, channel 128, cap-PCB bonded, 2.2 pF capacitors assembled. Parameter=no. of active ADCs 23
22 B1A1, channel -1, cap-PCB bonded, 2.2 pF capacitors assembled. Optimized test pulse and ADC delay. Parameter=no. of active ADCs 23
23 B1A1, channel 128, cap-PCB bonded, 2.2 pF capacitors assembled. Optimized test pulse and ADC delay. Parameter=no. of active ADCs 24
24 B1A1, channel -1, cap-PCB bonded, 12 pF capacitors assembled. Parameter=no. of active ADCs 25

25 B1A1, channel 128, cap-PCB bonded, 12 pF capacitors assembled. Parameter=no. of active ADCs 26
26 B1A1, channel -1, cap-PCB bonded, 12 pF capacitors assembled. Optimized test pulse and ADC delay. Parameter=no. of active ADCs 26
27 B1A1, channel 128, cap-PCB bonded, 12 pF capacitors assembled. Optimized test pulse and ADC delay. Parameter=no. of active ADCs 27
28 B1A1, channel -1, cap-PCB bonded, 12 pF capacitors + 620 kΩ resistors assembled. Parameter=no. of active ADCs 28
29 B1A1, channel -1, cap-PCB bonded, 12 pF capacitors + 620 kΩ resistors assembled. Optimized test pulse and ADC delay. Parameter=no. of active ADCs 29
30 B1A1, channel -1, cap-PCB bonded, 12 pF capacitors + 620 kΩ resistors assembled; Ibuf current maximized. Parameter=no. of active ADCs . . . 30
31 B1A1, channel -1, cap-PCB bonded, 12 pF capacitors + 620 kΩ resistors assembled; Ibuf current maximized. Optimized test pulse and ADC delay. Parameter=no. of active ADCs 31
32 B1A1, channel -1, cap-PCB bonded, 12 pF capacitors + 820 kΩ resistors assembled; Ibuf current maximized. Parameter=no. of active ADCs . . . 32
33 B1A1, channel 128, cap-PCB bonded, 12 pF capacitors + 820 kΩ resistors assembled; Ibuf current maximized. Parameter=no. of active ADCs . . . 32
34 B1A1, channel -1, cap-PCB bonded, 12 pF capacitors + 820 kΩ resistors assembled; Ibuf current maximized. Optimized test pulse and ADC delay. Parameter=no. of active ADCs 33
35 B1A1, channel 128, cap-PCB bonded, 12 pF capacitors + 820 kΩ resistors assembled; Ibuf current maximized. Optimized test pulse and ADC delay. Parameter=no. of active ADCs 33
36 B1A1, channel -1, cap-PCB bonded, 12 pF capacitors + 820 kΩ resistors assembled; Ibuf current maximized; Preamp GND configuration – input + backside. Parameter=no. of active ADCs 34
37 B1A1, channel 128, cap-PCB bonded, 12 pF capacitors + 820 kΩ resistors assembled; Ibuf current maximized; Preamp GND configuration – input + backside. Parameter=no. of active ADCs 35
38 B1A1, channel -1, cap-PCB bonded, 12 pF capacitors + 820 kΩ resistors assembled; Ibuf current maximized; Preamp GND configuration – input + backside. Optimized test pulse and ADC delay. Parameter=no. of active ADCs 36
39 B1A1, channel 128, cap-PCB bonded, 12 pF capacitors + 820 kΩ resistors assembled; Ibuf current maximized; Preamp GND configuration – input + backside. Optimized test pulse and ADC delay. Parameter=no. of active ADCs 36
40 B1A1, DLL & PLL stability monitoring (one night); HLP active; only one PLL monitor red 37
41 B1A1, DLL & PLL stability monitoring (a weekend); HLP active 38
42 B1A1, DLL & PLL stability monitoring (four days); HLP inactive 39

43 B1A1, DLL & PLL stability monitoring (two days); HLP active, DLL CP current lowered to 'h4 . . . 40
44 B0A2, channel -1, input bond removed from channel -1. Parameter=no. of active ADCs . . . 41
45 B0A2, channel -1, input bond removed from channel -1. Optimized test pulse and ADC delay. Parameter=no. of active ADCs . . . 42
46 B0A2, channel -1, cap-PCB bonded, 12 pF capacitors; Ibuf current maximized. Parameter=no. of active ADCs . . . 43
47 B0A2, channel -1, cap-PCB bonded, 12 pF capacitors; Ibuf current maximized. Optimized test pulse and ADC delay. Parameter=no. of active ADCs . . . 44
48 B0A2, channel -1, cap-PCB bonded, 12 pF capacitors + 820 kΩ resistor assembled; Ibuf current maximized. Parameter=no. of active ADCs . . . 45
49 B0A2, channel -1, cap-PCB bonded, 12 pF capacitors + 820 kΩ resistor assembled; Ibuf current maximized. Optimized test pulse and ADC delay. Parameter=no. of active ADCs . . . 46
50 B0A2, channel -1, cap-PCB bonded, 12 pF capacitors + 820 kΩ resistor assembled; Ibuf current maximized; ADC power supply with 2.2 Ω series resistor. Parameter=no. of active ADCs . . . 47
51 B0A2, channel -1, cap-PCB bonded, 12 pF capacitors + 820 kΩ resistor assembled; Ibuf current maximized; ADC power supply with 2.2 Ω series resistor. Optimized test pulse and ADC delay. Parameter=no. of active ADCs . . . 48
52 B0A2, channel -1, cap-PCB bonded, 12 pF capacitors + 820 kΩ resistor assembled; Ibuf current maximized; ADC power supply with 1 μH series inductor. Parameter=no. of active ADCs . . . 49
53 B0A2, channel -1, cap-PCB bonded, 12 pF capacitors + 820 kΩ resistor assembled; Ibuf current maximized; ADC power supply with 1 μH series inductor. Optimized test pulse and ADC delay. Parameter=no. of active ADCs . . . 50
54 B0A2, channel -1, cap-PCB bonded, no capacitors assembled; Ibuf current maximized; ADC power supply with 1 μH series inductor. Parameter=no. of active ADCs . . . 51
55 B0A2, channel -1, cap-PCB bonded, no capacitors assembled; Ibuf current maximized; ADC power supply with 1 μH series inductor. Optimized test pulse and ADC delay. Parameter=no. of active ADCs . . . 52
56 B0A2, channel -1, cap-PCB bonded, no capacitors assembled; Ibuf current maximized; ADC power supply with 1 μH series inductor; floating copper foil on ASIC. Parameter=no. of active ADCs . . . 53
57 B0A2, channel -1, cap-PCB bonded, no capacitors assembled; Ibuf current maximized; ADC power supply with 1 μH series inductor; floating copper foil on ASIC. Optimized test pulse and ADC delay. Parameter=no. of active ADCs . . . 54

58 B0A2, channel -1, cap-PCB bonded, 12 pF capacitors assembled; Ibuf current maximized; ADC power supply with 1 μH series inductor; floating copper foil on ASIC. Parameter=no. of active ADCs 55
59 B0A2, channel -1, cap-PCB bonded, 12 pF capacitors assembled; Ibuf current maximized; ADC power supply with 1 μH series inductor; floating copper foil on ASIC. Optimized test pulse and ADC delay. Parameter=no. of active ADCs 56
60 B0A2, channel -1, cap-PCB bonded, 12 pF capacitors assembled; Ibuf current maximized; ADC power supply with 1 μH series inductor; floating copper foil on ASIC; Preamp GND configuration – input + backside. Parameter=no. of active ADCs 57
61 B0A2, channel -1, cap-PCB bonded, 12 pF capacitors assembled; Ibuf current maximized; ADC power supply with 1 μH series inductor; floating copper foil on ASIC; Preamp GND configuration – input + backside. Optimized test pulse and ADC delay. Parameter=no. of active ADCs . . 58
62 B0A2, channel -1, cap-PCB bonded, 12 pF capacitors assembled; Ibuf current maximized; ADC power supply with 1 μH series inductor; grounded copper foil on ASIC; Preamp GND configuration – input + backside. Parameter=no. of active ADCs 59
63 B0A2, channel -1, cap-PCB bonded, 12 pF capacitors assembled; Ibuf current maximized; ADC power supply with 1 μH series inductor; grounded copper foil on ASIC; Preamp GND configuration – input + backside. Optimized test pulse and ADC delay. Parameter=no. of active ADCs . . 60
64 B0A2, channel -1, cap-PCB bonded, 12 pF capacitors assembled; Ibuf current maximized; ALL power supply with 1 μH series inductor; grounded copper foil on ASIC; Preamp GND configuration – input + backside. Parameter=no. of active ADCs 61
65 B0A2, channel -1, cap-PCB bonded, 12 pF capacitors assembled; Ibuf current maximized; ALL power supply with 1 μH series inductor; grounded copper foil on ASIC; Preamp GND configuration – input + backside. Optimized test pulse and ADC delay. Parameter=no. of active ADCs . . 62
66 B0A2, channel -1, cap-PCB bonded, 12 pF capacitors assembled; Ibuf current maximized; ALL power supply with 1 μH series inductor; grounded copper foil on ASIC; Preamp GND configuration – input + backside. EMI source amplitude 100mV. Parameter=frequency of EMI source 63
67 B0A2, channel -1, cap-PCB bonded, 12 pF capacitors assembled; Ibuf current maximized; ALL power supply with 1 μH series inductor; grounded copper foil on ASIC; Preamp GND configuration – only backside. EMI source amplitude 100mV. Parameter=frequency of EMI source 64
68 B0A2, S2D response at 1 MHz of main clock. Rising edge corresponds to the ADC conversion. 12 pF + 820 kΩ at input. 65
69 B0A2, Amplitude of S2D response at 1 MHz. 12 pF + 820 kΩ at input. . 66
70 B0A2, Time structure of S2D response at 1 MHz. 12 pF + 820 kΩ at input. 67

71 B0A2, S2D response at 1 MHz of main clock. Rising edge corresponds to the ADC conversion. 0 pF; floating plane on passivation. 68
72 B0A2, Amplitude of S2D response at 1 MHz. 0 pF; floating plane on passivation. 69
73 B0A2, Time structure of S2D response at 1 MHz. 0 pF; floating plane on passivation. 70
74 B0A2, S2D response at 1 MHz of main clock. Rising edge corresponds to the ADC conversion. 12 pF; grounded plane on passivation; Preamp GND configuration – input + backside. 71
75 B0A2, Amplitude of S2D response at 1 MHz. 12 pF; grounded plane on passivation; Preamp GND configuration – input + backside. 72
76 B1A4, S2D response at 1 MHz of main clock. Rising edge corresponds to the ADC conversion. Input pads not bonded. 73
77 B1A4, Amplitude of S2D response at 1 MHz. Input pads not bonded. . . 74
78 B1A4, Time structure of S2D response at 1 MHz. Input pads not bonded. 75
79 B1A4, S2D response at 1 MHz of main clock. Rising edge corresponds to the ADC conversion. 12 pF at inputs. 76
80 B1A4, Amplitude of S2D response at 1 MHz. 12 pF at inputs. 77
81 B1A4, Time structure of S2D response at 1 MHz. 12 pF at inputs. 78
82 B1A4, S2D response at 1 MHz of main clock. Rising edge corresponds to the ADC conversion. 12 pF at inputs. Preamp GND – input + backside 79
83 B1A4, Amplitude of S2D response at 1 MHz. 12 pF at inputs. Preamp GND – input + backside 80
84 B1A4, Time structure of S2D response at 1 MHz. 12 pF at inputs. Preamp GND – input + backside 81
85 B1A4, channel -1, Before input pads bonded. Parameter=no. of active ADCs 82
86 B1A4, channel 128, Before input pads bonded. Parameter=no. of active ADCs 82
87 B1A4, channel -1, Before input pads bonded. Optimized test pulse and ADC delay. Parameter=no. of active ADCs 83
88 B1A4, channel 128, Before input pads bonded. Optimized test pulse and ADC delay. Parameter=no. of active ADCs 83
89 B1A4, channel -1, cap-PCB bonded, 12 pF capacitors; Ibuf current maximized. Parameter=no. of active ADCs 84
90 B1A4, channel 128, cap-PCB bonded, 12 pF capacitors; Ibuf current maximized. Parameter=no. of active ADCs 85
91 B1A4, channel -1, cap-PCB bonded, 12 pF capacitors; Ibuf current maximized. Optimized test pulse and ADC delay. Parameter=no. of active ADCs 85
92 B1A4, channel 128, cap-PCB bonded, 12 pF capacitors; Ibuf current maximized. Optimized test pulse and ADC delay. Parameter=no. of active ADCs 86

93 B1A4, channel 128, cap-PCB bonded, 12 pF capacitors; Ibuf current maximized; Fsmp=33 MHz. Parameter=no. of active ADCs 87
94 B1A4, channel 128, cap-PCB bonded, 12 pF capacitors; Ibuf current maximized; Fsmp=33 MHz. Optimized test pulse and ADC delay. Parameter=no. of active ADCs 88
95 B1A4, channel -1, cap-PCB bonded, 12 pF capacitors; Ibuf current maximized; Preamp GND configuration – input + backside. Parameter=no. of active ADCs 89
96 B1A4, channel 128, cap-PCB bonded, 12 pF capacitors; Ibuf current maximized; Preamp GND configuration – input + backside. Parameter=no. of active ADCs 90
97 B1A4, channel -1, cap-PCB bonded, 12 pF capacitors; Ibuf current maximized; Preamp GND configuration – input + backside. Optimized test pulse and ADC delay. Parameter=no. of active ADCs 91
98 B1A4, channel 128, cap-PCB bonded, 12 pF capacitors; Ibuf current maximized; Preamp GND configuration – input + backside. Optimized test pulse and ADC delay. Parameter=no. of active ADCs 91
99 B1A4, channel -1, cap-PCB bonded, 12 pF capacitors; Ibuf current maximized; Preamp GND configuration – only input. Parameter=no. of active ADCs 92
100 B1A4, channel 128, cap-PCB bonded, 12 pF capacitors; Ibuf current maximized; Preamp GND configuration – only input. Parameter=no. of active ADCs 93
101 B1A4, channel -1, cap-PCB bonded, 12 pF capacitors; Ibuf current maximized; Preamp GND configuration – only input. Optimized test pulse and ADC delay. Parameter=no. of active ADCs 94
102 B1A4, channel 128, cap-PCB bonded, 12 pF capacitors; Ibuf current maximized; Preamp GND configuration – only input. Optimized test pulse and ADC delay. Parameter=no. of active ADCs 94
103 B1A4, channel -1, cap-PCB bonded, 12 pF capacitors; Ibuf current maximized; floating copper foil on ASIC; Preamp GND configuration – only input. Parameter=no. of active ADCs 95
104 B1A4, channel 128, cap-PCB bonded, 12 pF capacitors; Ibuf current maximized; floating copper foil on ASIC; Preamp GND configuration – only input. Parameter=no. of active ADCs 96
105 B1A4, channel -1, cap-PCB bonded, 12 pF capacitors; Ibuf current maximized; floating copper foil on ASIC; Preamp GND configuration – only input. Optimized test pulse and ADC delay. Parameter=no. of active ADCs 97
106 B1A4, channel 128, cap-PCB bonded, 12 pF capacitors; Ibuf current maximized; floating copper foil on ASIC; Preamp GND configuration – only input. Optimized test pulse and ADC delay. Parameter=no. of active ADCs 97

107 B1A4, channel -1, cap-PCB bonded, 12 pF capacitors; Ibuf current maximized; floating copper foil on ASIC; Preamp GND configuration – input + backside. Parameter=no. of active ADCs 98
108 B1A4, channel 128, cap-PCB bonded, 12 pF capacitors; Ibuf current maximized; floating copper foil on ASIC; Preamp GND configuration – input + backside. Parameter=no. of active ADCs 99
109 B1A4, channel -1, cap-PCB bonded, 12 pF capacitors; Ibuf current maximized; floating copper foil on ASIC; Preamp GND configuration – input + backside. Optimized test pulse and ADC delay. Parameter=no. of active ADCs 100
110 B1A4, channel 128, cap-PCB bonded, 12 pF capacitors; Ibuf current maximized; floating copper foil on ASIC; Preamp GND configuration – input + backside. Optimized test pulse and ADC delay. Parameter=no. of active ADCs 100
111 B1A4, channel 128, cap-PCB bonded, 12 pF capacitors; Ibuf current maximized; floating copper foil on ASIC; Preamp GND configuration – only backside. Parameter=no. of active ADCs 101
112 B1A4, channel -1, cap-PCB bonded, 12 pF capacitors; Ibuf current maximized; floating copper foil on ASIC; Preamp GND configuration – only backside. Optimized test pulse and ADC delay. Parameter=no. of active ADCs 102
113 B1A4, channel 128, cap-PCB bonded, 12 pF capacitors; Ibuf current maximized; floating copper foil on ASIC; Preamp GND configuration – only backside. Optimized test pulse and ADC delay. Parameter=no. of active ADCs 102
114 B1A4, channel -1, cap-PCB bonded, 12 pF capacitors; Ibuf current maximized; floating copper foil on ASIC; All inputs grounded; Preamp GND configuration – only backside. Parameter=no. of active ADCs 103
115 B1A4, channel 128, cap-PCB bonded, 12 pF capacitors; Ibuf current maximized; floating copper foil on ASIC; All inputs grounded; Preamp GND configuration – only backside. Parameter=no. of active ADCs 104
116 B1A4, channel -1, cap-PCB bonded, 12 pF capacitors; Ibuf current maximized; floating copper foil on ASIC; All inputs grounded; Preamp GND configuration – only backside. Optimized test pulse and ADC delay. Parameter=no. of active ADCs 105
117 B1A4, channel 128, cap-PCB bonded, 12 pF capacitors; Ibuf current maximized; floating copper foil on ASIC; All inputs grounded; Preamp GND configuration – only backside. Optimized test pulse and ADC delay. Parameter=no. of active ADCs 105
118 B1A4, channel -1, cap-PCB bonded, 12 pF capacitors; Ibuf current maximized; floating small horizontal copper foil on ASIC; All inputs grounded; Preamp GND configuration – only backside. Parameter=no. of active ADCs106

119 B1A4, channel 128, cap-PCB bonded, 12 pF capacitors; Ibuf current maximized; floating small horizontal copper foil on ASIC; All inputs grounded; Preamp GND configuration – only backside. Parameter=no. of active ADCs107
120 B1A4, channel -1, cap-PCB bonded, 12 pF capacitors; Ibuf current maximized; floating small horizontal copper foil on ASIC; All inputs grounded; Preamp GND configuration – only backside. Optimized test pulse and ADC delay. Parameter=no. of active ADCs 108
121 B1A4, channel 128, cap-PCB bonded, 12 pF capacitors; Ibuf current maximized; floating small horizontal copper foil on ASIC; All inputs grounded; Preamp GND configuration – only backside. Optimized test pulse and ADC delay. Parameter=no. of active ADCs 108
122 B1A4, channel -1, cap-PCB bonded, 12 pF capacitors; Ibuf current maximized; floating small horizontal copper foil on ASIC; Preamp GND configuration – only backside. Parameter=no. of active ADCs 109
123 B1A4, channel 128, cap-PCB bonded, 12 pF capacitors; Ibuf current maximized; floating small horizontal copper foil on ASIC; Preamp GND configuration – only backside. Parameter=no. of active ADCs 110
124 B1A4, channel -1, cap-PCB bonded, 12 pF capacitors; Ibuf current maximized; floating small horizontal copper foil on ASIC; Preamp GND configuration – only backside. Optimized test pulse and ADC delay. Parameter=no. of active ADCs 111
125 B1A4, channel 128, cap-PCB bonded, 12 pF capacitors; Ibuf current maximized; floating small horizontal copper foil on ASIC; Preamp GND configuration – only backside. Optimized test pulse and ADC delay. Parameter=no. of active ADCs 111
126 B1A4, channel -1, cap-PCB bonded, 12 pF capacitors; Ibuf current maximized. Optimized test pulse and ADC delay. 112
127 B1A4, channel 128, cap-PCB bonded, 12 pF capacitors; Ibuf current maximized. Optimized test pulse and ADC delay. 113
128 B1A5, channel -1, cap-PCB bonded, 12 pF capacitors; Ibuf current maximized. Parameter=no. of active ADCs 114
129 B1A5, channel 128, cap-PCB bonded, 12 pF capacitors; Ibuf current maximized. Parameter=no. of active ADCs 115
130 B1A5, channel -1, cap-PCB bonded, 12 pF capacitors; Ibuf current maximized. Optimized test pulse and ADC delay. Parameter=no. of active ADCs 115
131 B1A5, channel 128, cap-PCB bonded, 12 pF capacitors; Ibuf current maximized. Optimized test pulse and ADC delay. Parameter=no. of active ADCs 116
132 B1A5, channel -1, cap-PCB bonded, 12 pF capacitors; Ibuf current maximized. EMI source 1cm over ASIC, amplitude 100mV. Parameter=frequency of EMI source 117

133 B1A5, channel -1 (second measurement), cap-PCB bonded, 12 pF capacitors; Ibuf current maximized. EMI source 1cm over ASIC, amplitude 100mV. Parameter=frequency of EMI source 117
134 B1A5, channel 128, cap-PCB bonded, 12 pF capacitors; Ibuf current maximized. EMI source 1cm over ASIC, amplitude 100mV. Parameter=frequency of EMI source 118
135 B1A5, channel 128 (second measurement), cap-PCB bonded, 12 pF capacitors; Ibuf current maximized. EMI source 1cm over ASIC, amplitude 100mV. Parameter=frequency of EMI source 118
136 B1A5, channel -1 (inverted polarity of EMI source), cap-PCB bonded, 12 pF capacitors; Ibuf current maximized. EMI source 1cm over ASIC, amplitude 100mV. Parameter=frequency of EMI source 119
137 B1A5, channel 128 (inverted polarity of EMI source), cap-PCB bonded, 12 pF capacitors; Ibuf current maximized. EMI source 1cm over ASIC, amplitude 100mV. Parameter=frequency of EMI source 119
138 B1A5, channel 128 (inverted phase (180 deg.) of EMI source), cap-PCB bonded, 12 pF capacitors; Ibuf current maximized. EMI source 1cm over ASIC, amplitude 100mV. Parameter=frequency of EMI source 120
139 B1A5, channel -1, cap-PCB bonded, 12 pF capacitors; Ibuf current maximized. EMI source (47 Ω serial resistance added) 6cm over ASIC, amplitude 3V. Parameter=frequency of EMI source 121
140 B1A5, channel 128, cap-PCB bonded, 12 pF capacitors; Ibuf current maximized. EMI source (47 Ω serial resistance added) 6cm over ASIC, amplitude 3V. Parameter=frequency of EMI source 121
141 B1A5, channel -1, cap-PCB bonded, 12 pF capacitors; Ibuf current maximized. EMI source (47 Ω serial resistance added) 6cm over ASIC, amplitude 3V. Preamp GND configuration – input + backside. Parameter=frequency of EMI source 122
142 B1A5, channel 128, cap-PCB bonded, 12 pF capacitors; Ibuf current maximized. EMI source (47 Ω serial resistance added) 6cm over ASIC, amplitude 3V. Preamp GND configuration – input + backside. Parameter=frequency of EMI source 123
143 B1A5, channel -1, cap-PCB bonded, 12 pF capacitors; Ibuf current maximized. EMI source (47 Ω serial resistance added) 6cm over ASIC, amplitude 3V. Preamp GND configuration – only input. Parameter=frequency of EMI source 124
144 B1A5, channel 128, cap-PCB bonded, 12 pF capacitors; Ibuf current maximized. EMI source (47 Ω serial resistance added) 6cm over ASIC, amplitude 3V. Preamp GND configuration – only input. Parameter=frequency of EMI source 125
145 Damaged corner of ASIC 4 128
146 ASIC 4 – Good and damaged bonds and pads 129
147 ASIC 4 – Damaged bonds and pads 130
148 ASIC 4 – Very deep scratch reaching beneath the pad 131

149 Copper foil on ASIC B0A2 and 1 μH inductor assembly 132
150 Copper foil on ASIC B1A4 133
151 Small horizontal copper foil on ASIC B1A4 134
152 EMI source over ASIC B0A2 135