# MEMSy z czym to się je

Tomasz Fiutowski

# What is Stimesi ?

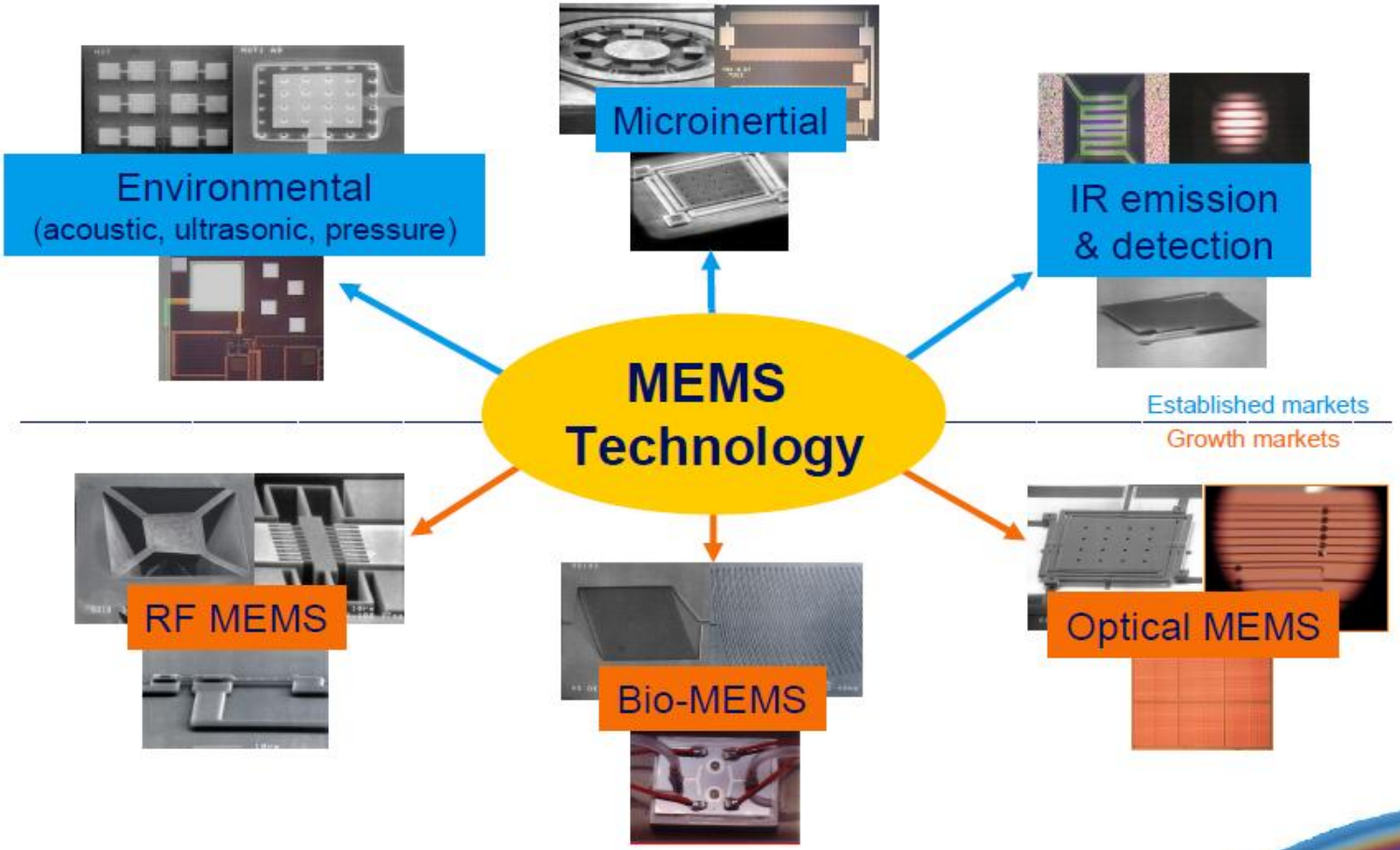
STIMESI
Stimulation Action on MEMS and SiP

- The **STIMESI** project belongs to the **EUROPRACTICE** family
  - **STIMESI** stands for **STIMulation**. It is a 4 year Framework 6 Integrated Project
- Mission

...The goal of the STIMESI Stimulation Action is to stimulate European universities and research institutes to adopt MEMS and SiP technologies in different ways...

imec MEMSCAP The Power of a Small World™ QinetiQ Infineon tronics microsystems Science & Technology Facilities Council Rutherford Appleton Laboratory

# Key MEMS Applications Areas

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# MEMS design modes

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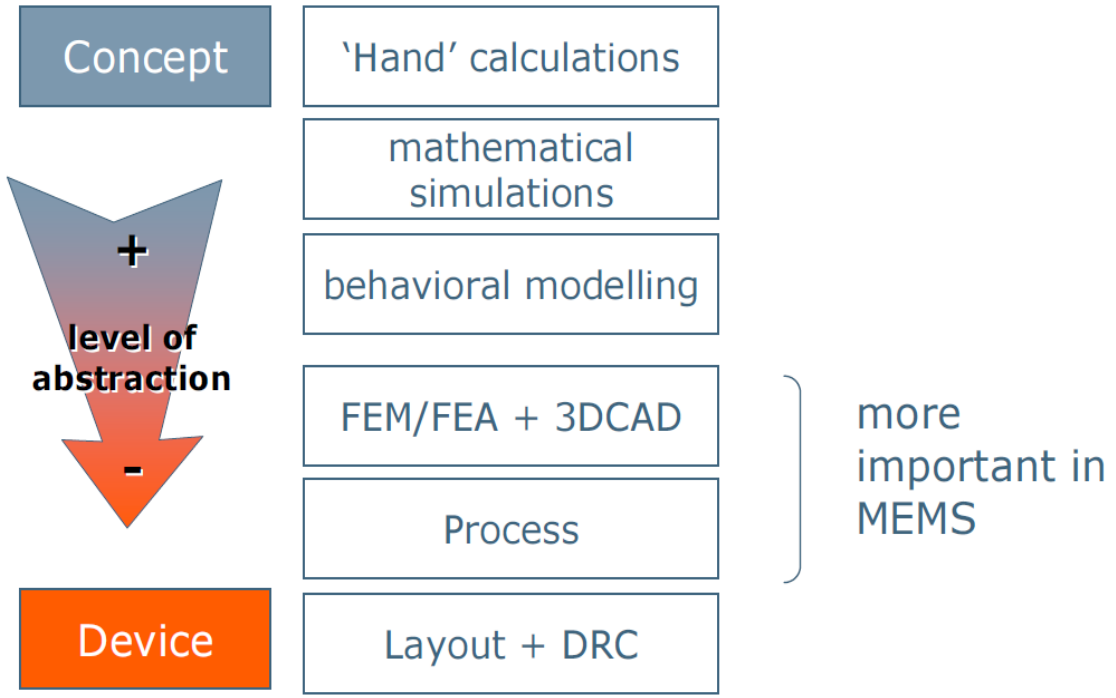

# Delivering the Stimesi Goal

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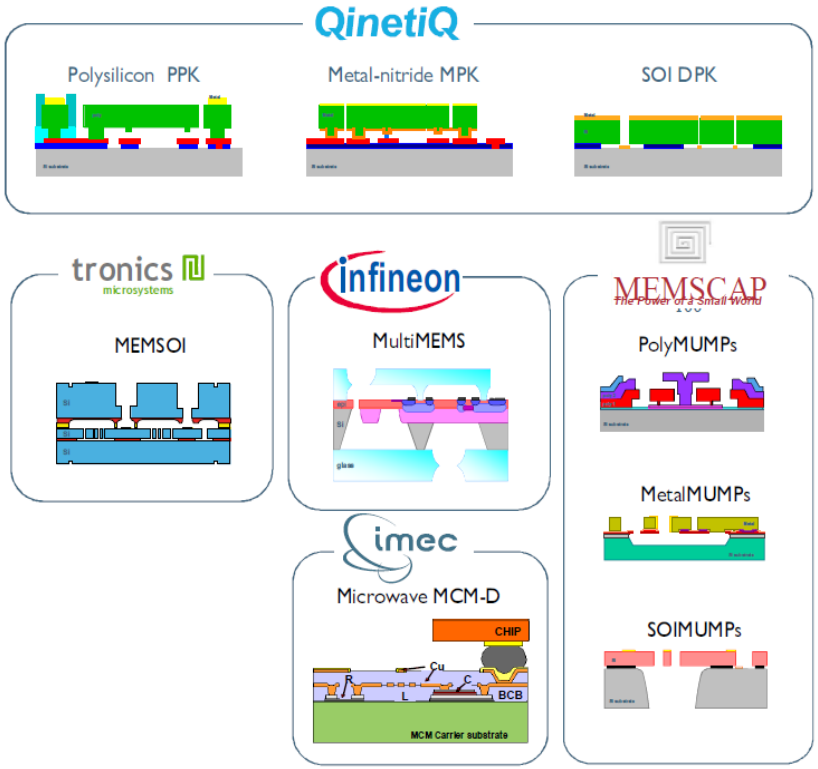
- Courses to introduce the MEMS MPW technologies within EUROPRACTICE :
  - Infineon-SensoNor MultiMEMS & Tronics MEMSOI processes
  - MEMSCAP : MUMPS (Multi-User MEMS) processes
  - QinetiQ : INTEGRAMplus Silicon MEMS Prototyping Services
  - IMEC : RF-SiP design and RF system integration
- Improved accessibility
  - improved access to CAD tools
  - MPW support for main CAD tools via dedicated software design kits
  - support MPW design via dedicated handbooks

Design access kits (process-specific)

MEMS design and simulation

System-level simulation (Electronics + MEMS)

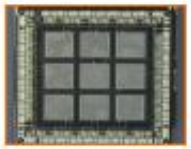
## MEMS FABRICATION

**Surface Micromachining**
- Metal-nitride
- Polysilicon

**High Aspect Micromachining**
- SOI
- Si

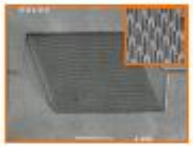
## MEMS FUNCTIONS

Microinertial



Environmental (multisensors)

Comms (RF + Optical)

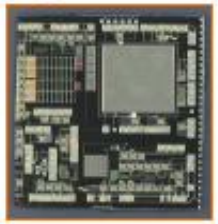


Biomedical

## ELECTRONICS

**Hybrid Integration**
- MEMS + COTS
- MEMS + ASIC

**Monolithic Integration**
- MEMS + CMOS
- MEMS + BiCMOS



MEMS Foundry

**INTEGRAM*plus* Si Service**

IC Foundry

Customer Products

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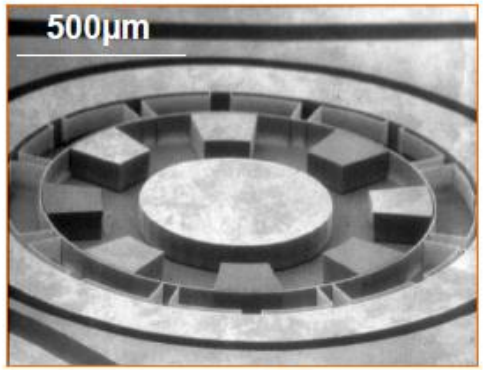
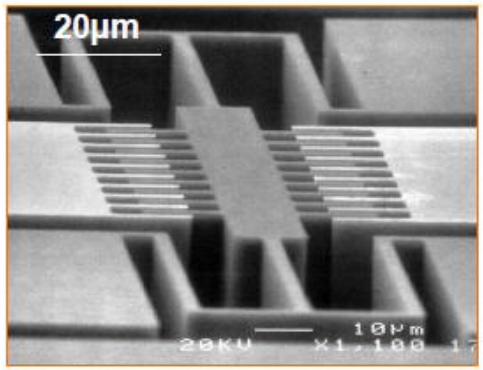
# DRIE-based SOI Micromachining

- Silicon structural layer
  - High uniformity, thick (25-50µm) layer
    - defined by qualified SOI start material
  - Low stress, single crystal layer
    - well known materials properties
    - high reliability
  - High aspect ratio features possible
  - Large devices possible




Gyroscope




Resonator

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# SOI Micromachining

**(a) Start material**

SOI substrate from vendor

**(b) Define Structural Mask**

Pattern resist using MECH1 mask

**(c) Define SOI Device Layer**

Deep dry etch (using MECH1 mask) to define structural Silicon1 layer.

**(d) Release**

Timed etch in HF to selectively remove oxide under suspended portions. Remaining buried oxide (BOX) acts as an anchor to the handle (Silicon0).

**(e) Metallisation**

Deposit metal on wafer (patterned device layer acts as a self-aligned shadow mask) for bonding and interconnect.






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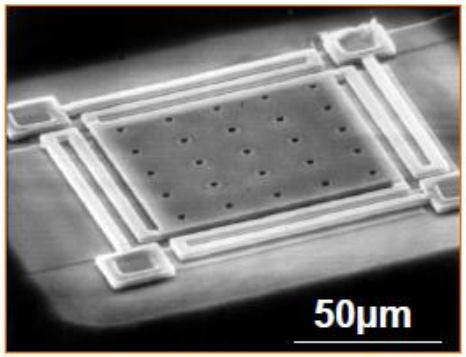
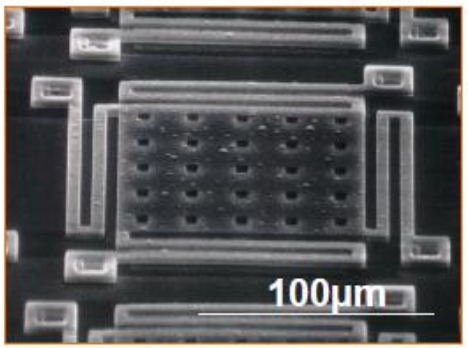
# Sacrificial Surface Micromachining

- Thin structural layer (1-2µm) with buried electrode:
  - Polysilicon (PPK)
    - Industry standard structural layer
    - Low stress gradient
    - Low stress (< -10MPa)
  - Metal/nitride (MPK)
    - Nitride with symmetric metallization
      - Engineered for similar properties to industry standard polysilicon
    - CMOS-compatible
    - Low stress gradient
    - Moderate stress (< +100MPa)




Accelerometer (PPK)




Accelerometer (MPK)

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# Polysilicon Surface Micromachining

**a. Base Layer and substrate contact**

- Base level dielectric on a silicon wafer
- Pattern with VIA0 to form substrate contact hole

**b. Fixed Polysilicon 0 Layer**

- Deposit polysilicon, pattern with FIXED0 mask and dry etch to form interconnect, substrate contact and mechanical ground

**c. Dimple and Anchor Hole Formation**

- Deposit oxide
- Pattern with DIMP1 and dry etch dimples
- Pattern with ANC1 and dry etch mechanical anchor holes

**d. Mechanical Polysilicon 1 Layer**

- Deposit polysilicon (mechanical) and oxide mask, pattern with MECH1 and dry etch

**e. Contact Hole Formation**

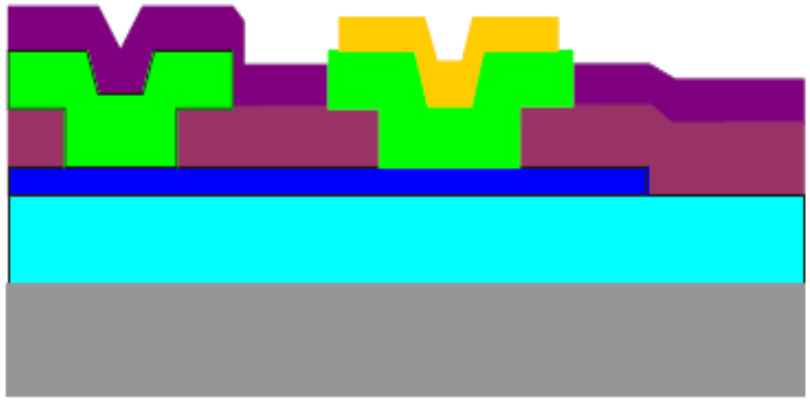
- Deposit further oxide followed by stress reduction / drive-in anneal
- Pattern with VIA1 and dry etch contact holes

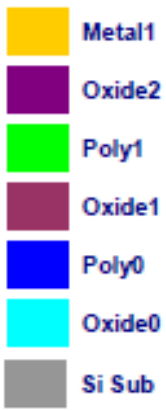
**f. Metallisation Formation**

- Pattern with MET1, evaporate and lift-off metal to form bond pads and interconnect

**g. Sacrificial Release**

- Remove sacrificial oxide in an HF-based release process to free the mechanical layer. (Note the slight undercut of the fixed Poly0 layer - nitride passivation is not typically employed).







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# Metal-Nitride Surface Micromachining

**a. Base Layer**
- Base level dielectric on a silicon wafer

**b. Substrate Contact Hole Formation**
- Pattern oxide 0 with VIA0 and dry etch

**c. Fixed Metal 0 Definition**
- Sputter metal, pattern with FIXED0 mask and dry etch to form interconnect, main registration markers and substrate contact.
- Deposit insulating dielectric, pattern with DIEL0 and dry etch

**d. Anchor Hole Formation Definition**
- Spin on polyimide (PIQ1)
- Pattern with DIMP1 and partial dry etch
- Pattern with ANC1 and dry etch anchor holes for structural layer

**e. Structural Layer Definition**
- Sputter metal (Metal 1a)
- Pattern CUTMET and etch (potential future process upgrade – dependent on customer demand )
- PECVD deposit silicon nitride (Nitride1). Pattern nitride with VIA1 and dry etch to contact Metal1a to Metal1b
- Sputter metal (Metal 1b)
- Pattern CUTMET and etch (potential future process upgrade – dependent on customer demand)
- Pattern structural metal-nitride stack with MECH1 and dry etch

**f. Sacrificial Release**
- Remove polyimide layer in a dry process


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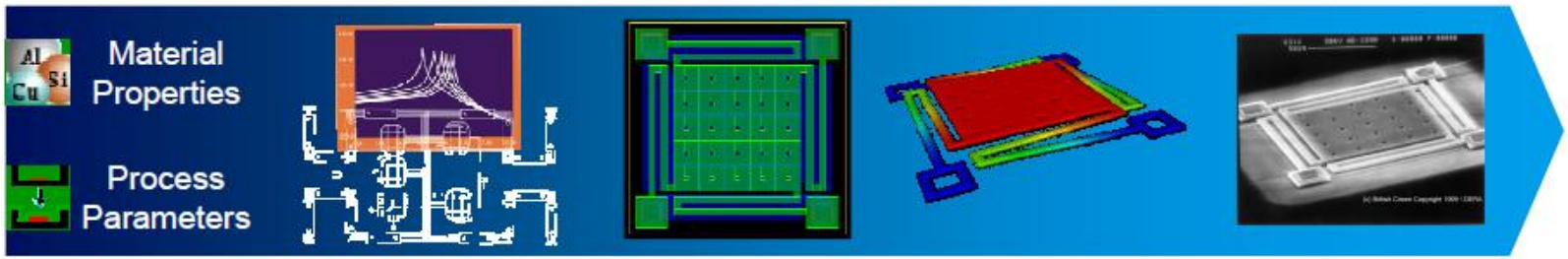
# Design for Manufacture Approach

## INTEGRAM*plus* Design Kits, Software and Processes

CoventorWare ™




ARCHITECT ™ DESIGNER ™ ANALYZER ™ Fabricate & test

Process Information

Development Cycle

| Process Data | Simulation | Layout | Extraction | |
|---|---|---|---|---|
| INTEGRAM Support Files | Behavioral simulation | 2D layout (Design Rules) | FE modelling & extraction | INTEGRAM Foundry Service |

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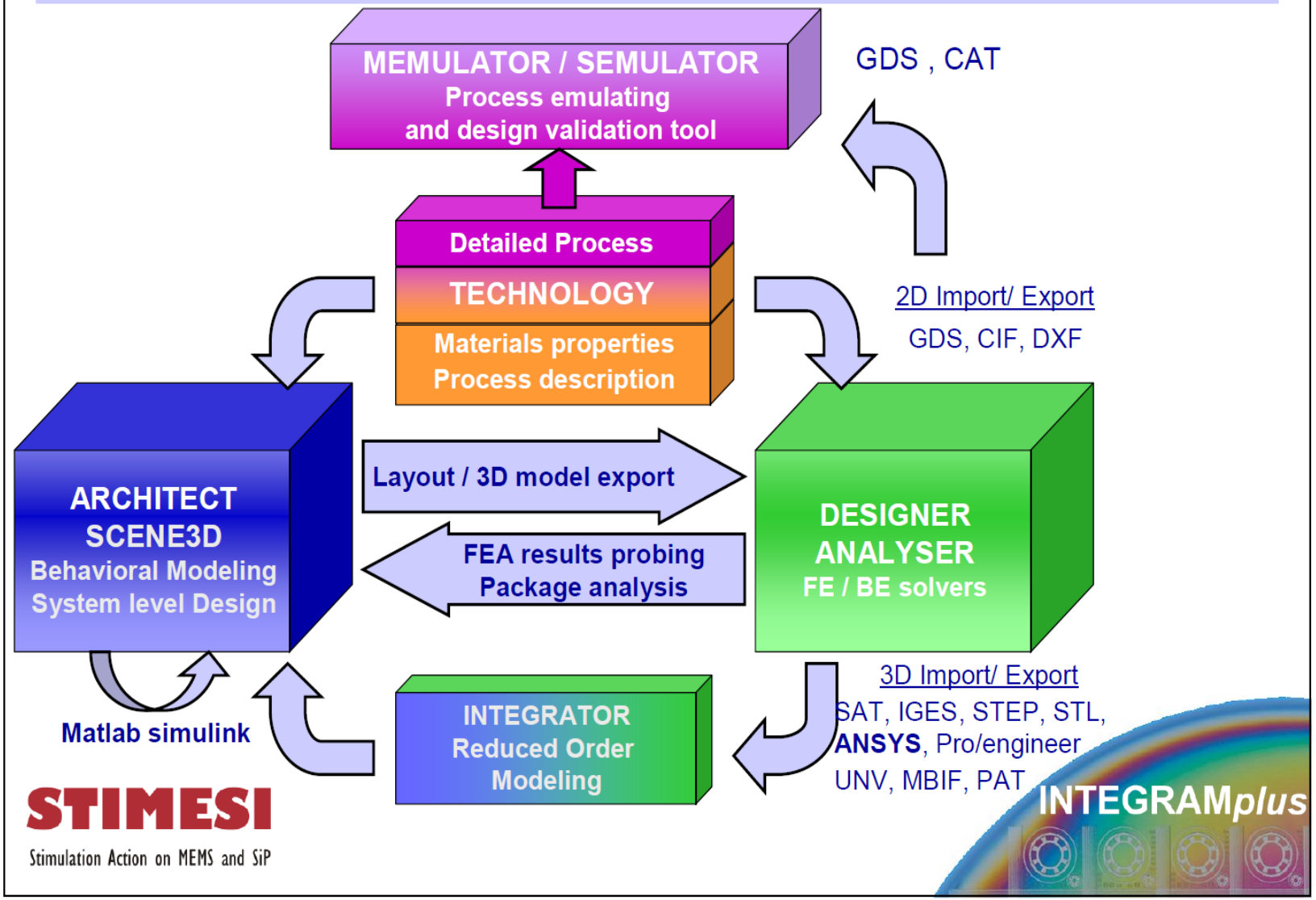
# CoventorWare Tools



# Examples of Components & Microsystems

## Based on INTEGRAM*plus* Silicon MEMS

- **SOI micromachining**
  - accelerometers, gyroscopes, magnetometers, pressure sensors…
  - microfluidics / bio-chips
  - optical switches, variable optical attenuators (VOAs), modulators
  - silicon optical bench (SiOB) including waveguides & component slots
- **Metal-nitride surface micromachining**
  - micro-ultrasonic transducer (MUT) arrays, microphones, accelerometers, micromirror arrays
  - System on a Chip (SoC): integrated MUT array, microphone, IR detector array
- **Microsystems (multi-sensors or sensors+electronics)**
  - micro-inertial measurement unit (µIMU)
  - environmental data logger, multi-sensor pods

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**N.B. Standard MPW processes are not well suited to RF MEMS**



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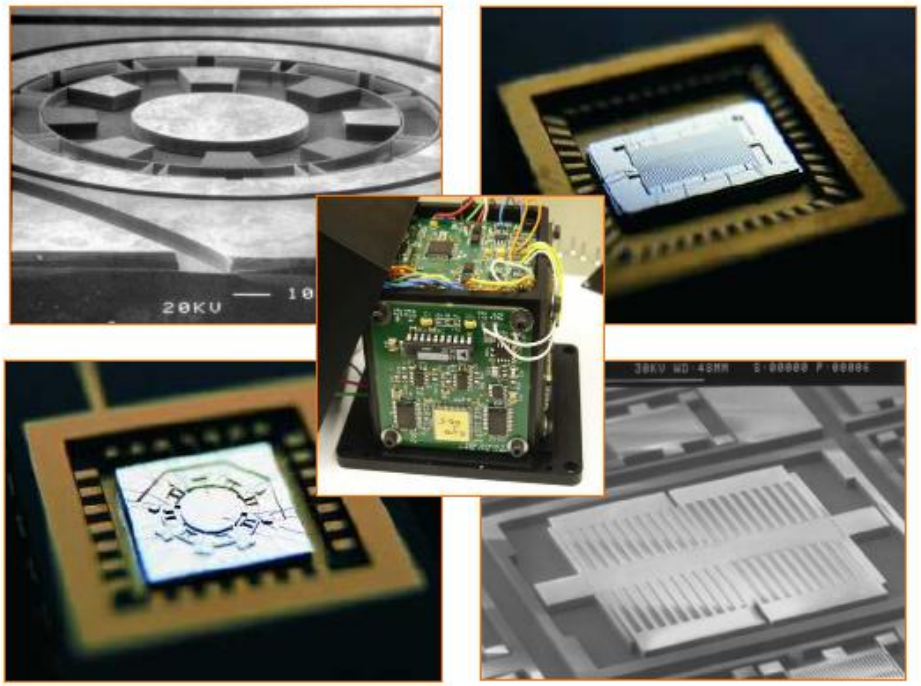
# SOI Microinertial Devices

- µ-IMU:
  - Accelerometers
  - Gyroscopes
  - Magnetometers
- Measuring:
  - Orientation
  - Shock
  - Vibration

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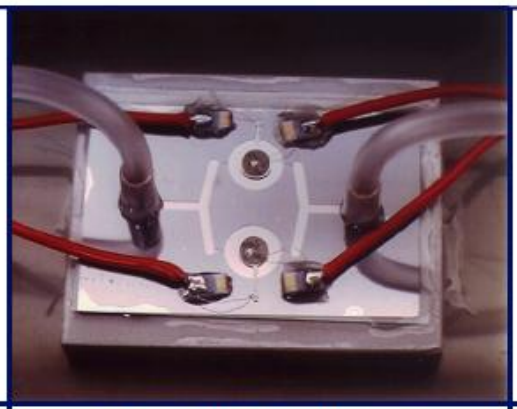
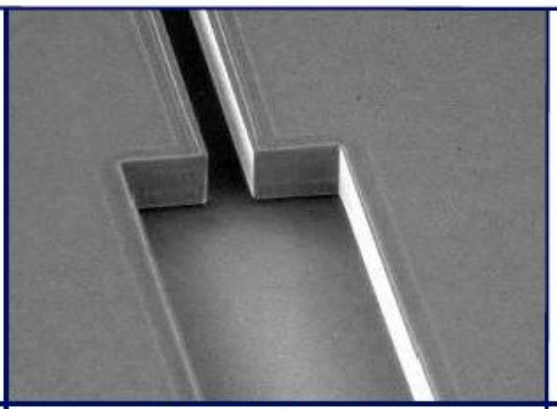
# Microfluidic (Bio-MEMS) Components

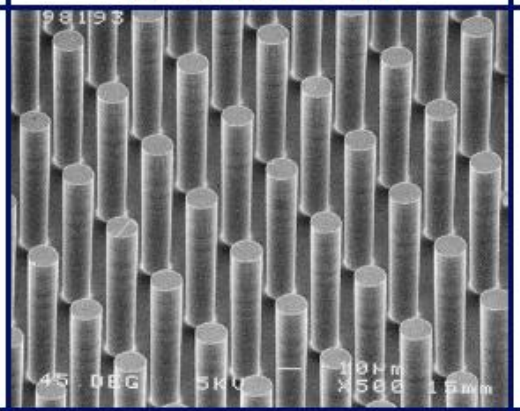

Microfluidic Chip



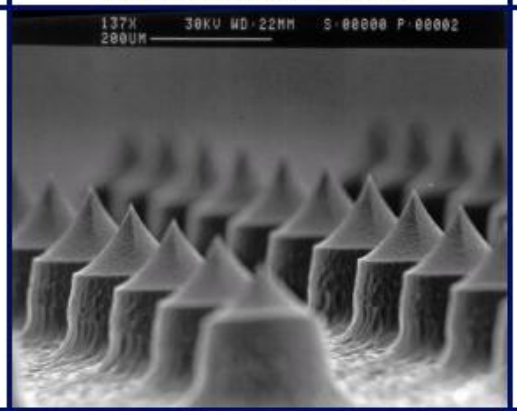
Microfluidic Pump



Hollow Waveguide



High area matrix for trapping DNA (filter)




Drug delivery (microneedles)

Automated Fluidic System

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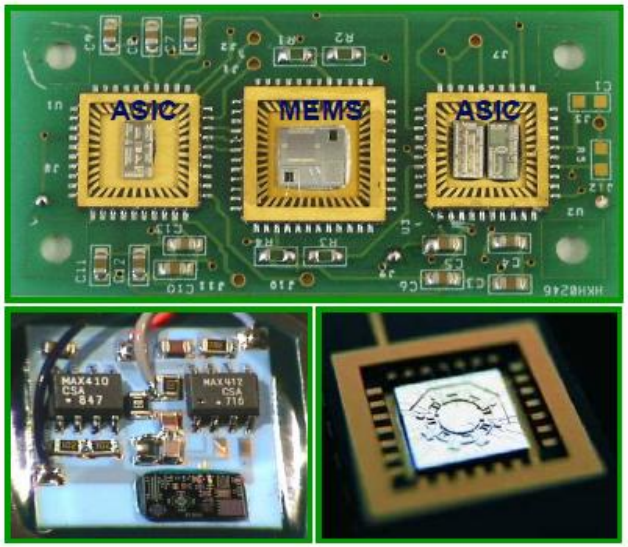
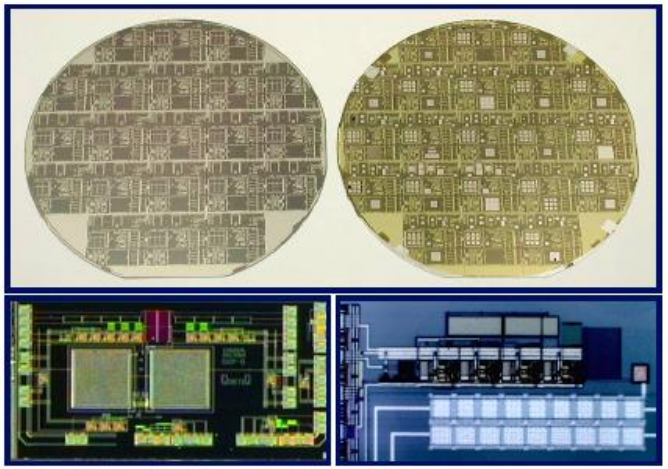
# Electronic Integration in Microsystems

- **Hybrid**
  - Flip chip / surface mount / PCB
  - System in Package (SiP) …
  - Bonded wafer / chip stacks …
  - Shorter development cycles
  - Reduced cost for lower volumes




*or*



- **Monolithic**
  - Only use if there is a real driver
  - Lowest cost in highest volumes
  - High performance / compact
  - Large area arrays
  - Robustness & design security

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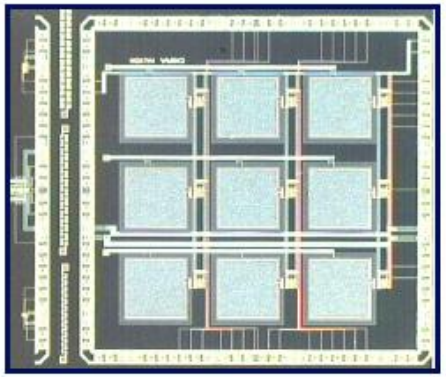
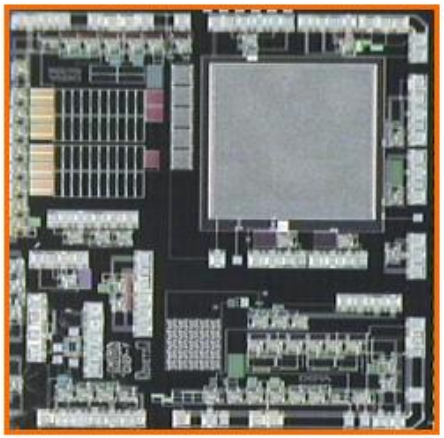
# Integrated Sensor Microsystems

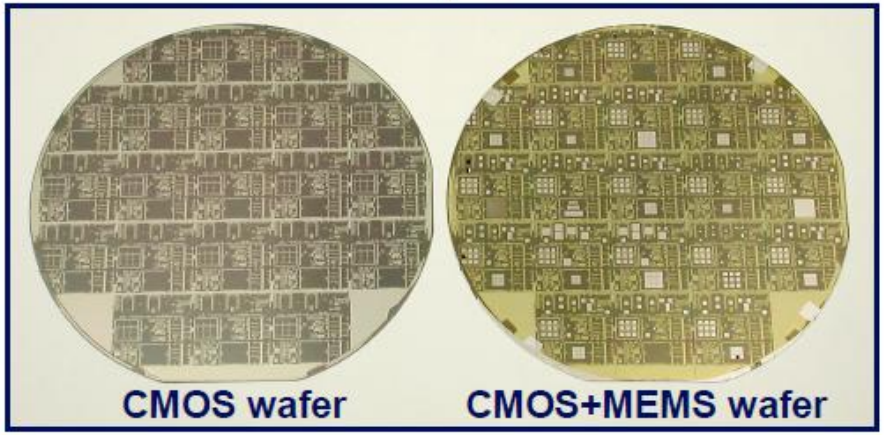
- Monolithically integrated micro-ultrasonic transducer (MUT) array + CMOS electronics
- Monolithically integrated microphone + CMOS electronics



MUT Array (left)
Packaged MUTs (right)



Microphone



CMOS wafer CMOS+MEMS wafer

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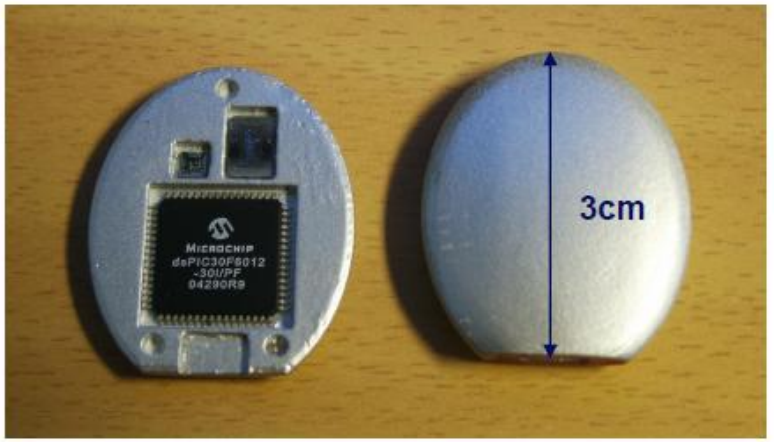
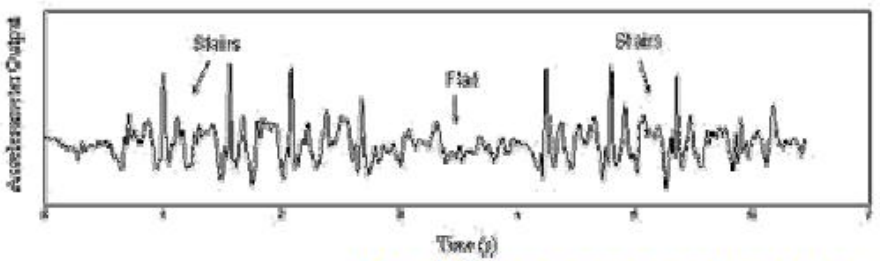
# Miniaturised Data Logger

- Unobtrusive miniature design
  - 2 integrated MEMS chips + microcontroller
- Multi-sensor integration
  - based on standard MEMS sensor modules
- Embedded processing




**Monitoring personal motion**

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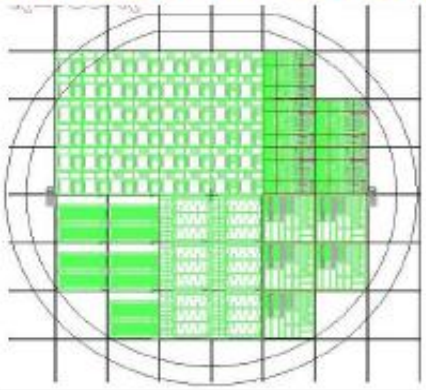
# Multi-Project Wafer (MPW) Runs

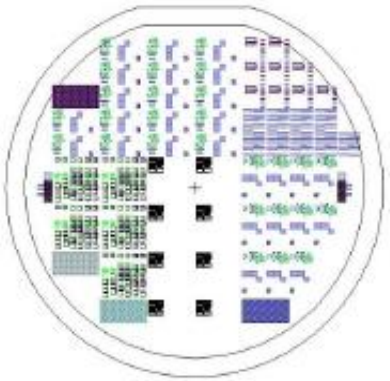
- Mask and run costs shared between customers for lowest cost of entry
  - multiple customer designs on each wafer
  - results in a small number of die (20) for each customer
- Processes tightly specified
  - designs must not risk impacting die for other customers
  - fixed die size (4.5mm user area) / no scope for process variations
- Past Examples:

**SOI micromachining (DPK)**



- Accelerometers, gyroscopes & magnetometers
- VOAs, switches & waveguides
- Resonators
- Test modules

**Metal-Nitride Surface Micromachining (MPK)**



- Accelerometers
- Ultrasonic sensors
- Switches & varactors
- Micromirrors arrays
- Test modules

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# Single Project Wafer (SPW) Runs

- Small batch size in standardised process sequence to control cost
  - single customer design per wafer
    - cost depends on number of wafers ordered (1-2)
    - additionally benefit from sharing batch processes with SPW wafer submissions from other customers
    - shared batch costs with MPW runs
    - MEMS-only process
  - results in a moderate number of die (<140) to customer

# Single Project Wafer (SPW) Run Benefits

- Lower unit cost per chip than MPW
- Added process flexibility
  - variable die size (3.0 - 9.2mm)
  - additional standard process options
    - e.g. tuning of structural layer thicknesses
  - improved process control as single customer design
    - e.g. tune photolithography for customer-specified geometry

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# Custom MEMS Runs

- Full batches in custom process sequence
  - single customer design per batch
    - 8 – 12 wafers / batch typically
    - use standard process steps where possible to minimise cost and associated process development time
    - MEMS-only process
  - results in a large number of die (>500) or whole wafers to customer

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# Custom MEMS Run Benefits

- Lowest unit cost per chip
- Maximum flexibility
  - variable die size (3.0 - 9.2mm)
  - fine tuning of process sequence and steps
    - combined standard process steps / sequences
    - new process sequences
      - associated process development where required
  - CMOS integration option
    - post-process MEMS on standard CMOS
- Flexible scheduling
  - not tied to MPW schedule

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# Standard Process Specifications

| MULTI-PROJECT WAFER | MPK | DPK | PPK |
|---|---|---|---|
| Structural layer | Metal-nitride | SOI | Polysilicon |
| Structural layer thickness | 2.4um | 25 or 50um | 2um |
| Number of chips | 20 | 20 | 20 |
| Active Chip Area Dimensions | 4.5 x 4.5mm | 4.5 x 4.5mm | 4.5 x 4.5mm |
| **SINGLE-PROJECT WAFER** | | | |
| Structural layer thickness | 1.4 or 2.4um | 25, 50, 100um | 2.0 or 1.0um |
| Number of chips | Up to 140 | Up to 140 | Up to 140 |
| Active Chip Area Dimensions | <9.2 x 9.2mm<br>>3 x 3mm | < 9.2 x 9.2mm<br>>3 x 3mm | <9.2 x 9.2mm<br>>3 x 3mm |

- A minimum of 2 slots are scheduled during the year for MPW and SPW runs
  - includes dicing of chips and/or the release of the MEMS structures using critical point drying (CPD) where required
    - approx. 20 released chips for MPW
    - approx. 40 released chips for SPW + remainder unreleased
      - alternative of wafer scale release (part-sawn)

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# INTEGRAM*plus* Run Schedule and Prices

| PPK Schedule (MPW: €7k / SPW: POA) | | | |
|---|---|---|---|
| **PPK Run No.** | **Latest Order Date** | **Data Files Received** | **Delivery Date** |
| PPK 08/02 | 3 Dec. 2008 | 24 Dec. 2008 | 30 Mar. 2008 |
| PPK 09/01 | 11 May 2009 | 1 June 2009 | 24 Aug. 2009 |

| DPK Schedule (MPW: €5.5k / SPW: POA) | | | |
|---|---|---|---|
| **DPK Run No.** | **Latest Order Date** | **Data Files Received** | **Delivery Date** |
| DPK 08/02 | 3 Dec. 2008 | 24 Dec. 2008 | 30 Mar. 2008 |
| DPK 09/01 | 11 May 2009 | 1 June 2009 | 24 July 2009 |

| MPK Schedule (MPW: €15k / SPW: POA) | | | |
|---|---|---|---|
| **MPK Run No.** | **Latest Order Date** | **Data Files Received** | **Delivery Date** |
| MPK 08/02 | 3 Dec. 2008 | 24 Dec. 2008 | 30 Mar. 2008 |
| MPK 09/01 | 11 May 2009 | 1 June 2009 | 24 Aug. 2009 |

- Design files must be submitted in GDSII or TDB format
- Orders are subject to written acceptance and will be acknowledged
- Price is based on Sterling: Euro exchange rate at time of presentation (excluding does not include insurance, local taxes and duties) and is subject to change without notice
- MPW (Multi Project Wafer) is a shared wafer with multiple designs. Approximately 20 die per customer design will be supplied. Each die is approximately 4.7mm x 4.7mm. There are limited number of slots on a schedule run which will be filled on first accepted first served basis.
- QinetiQ reserves the right not to launch a scheduled process run should there be an insufficient number of customer designs. At least one process run will be run every calendar year with customers for cancelled scheduled runs included on the next scheduled process run.

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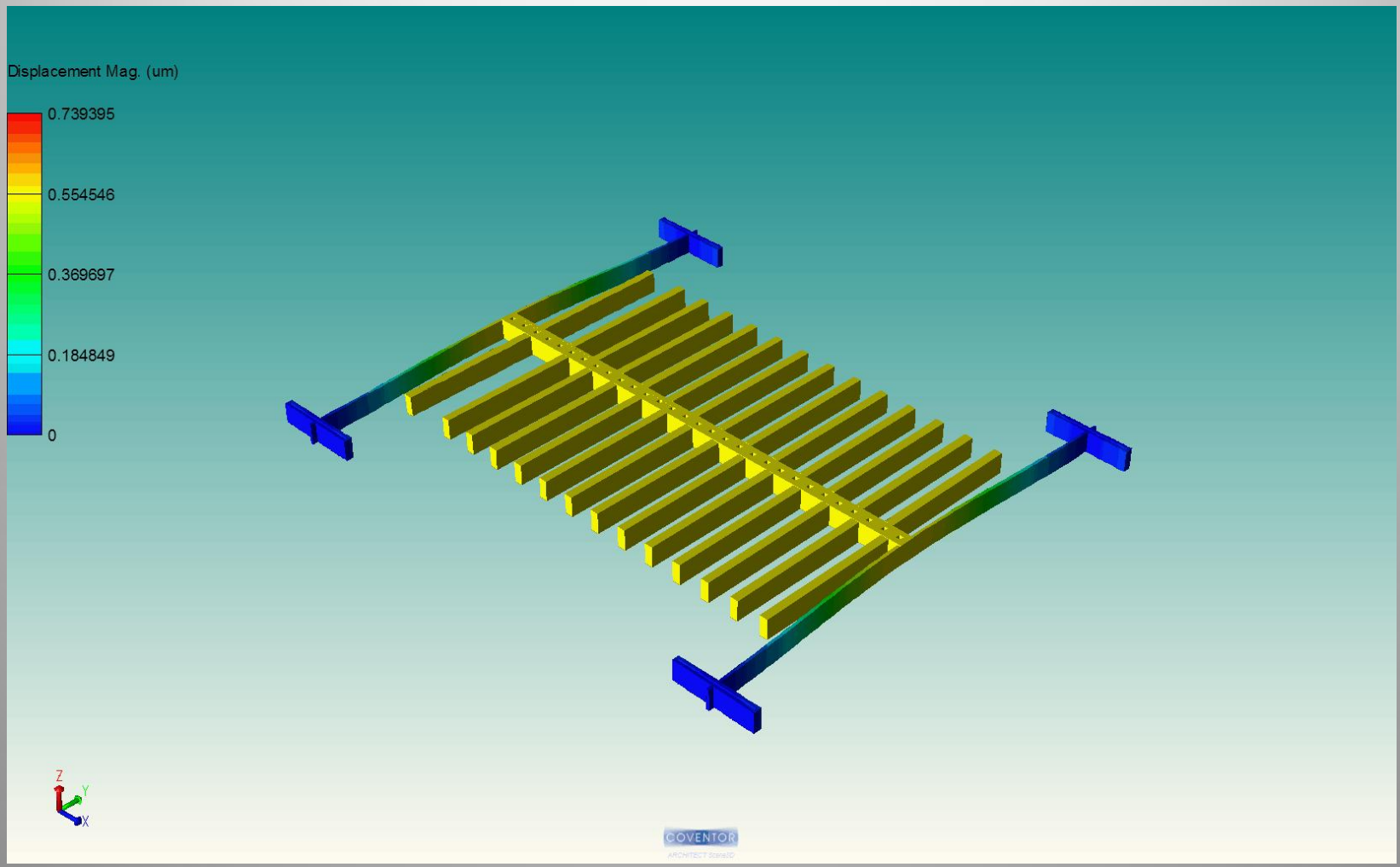
Displacement Mag. (um)
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0.554546
0.369697
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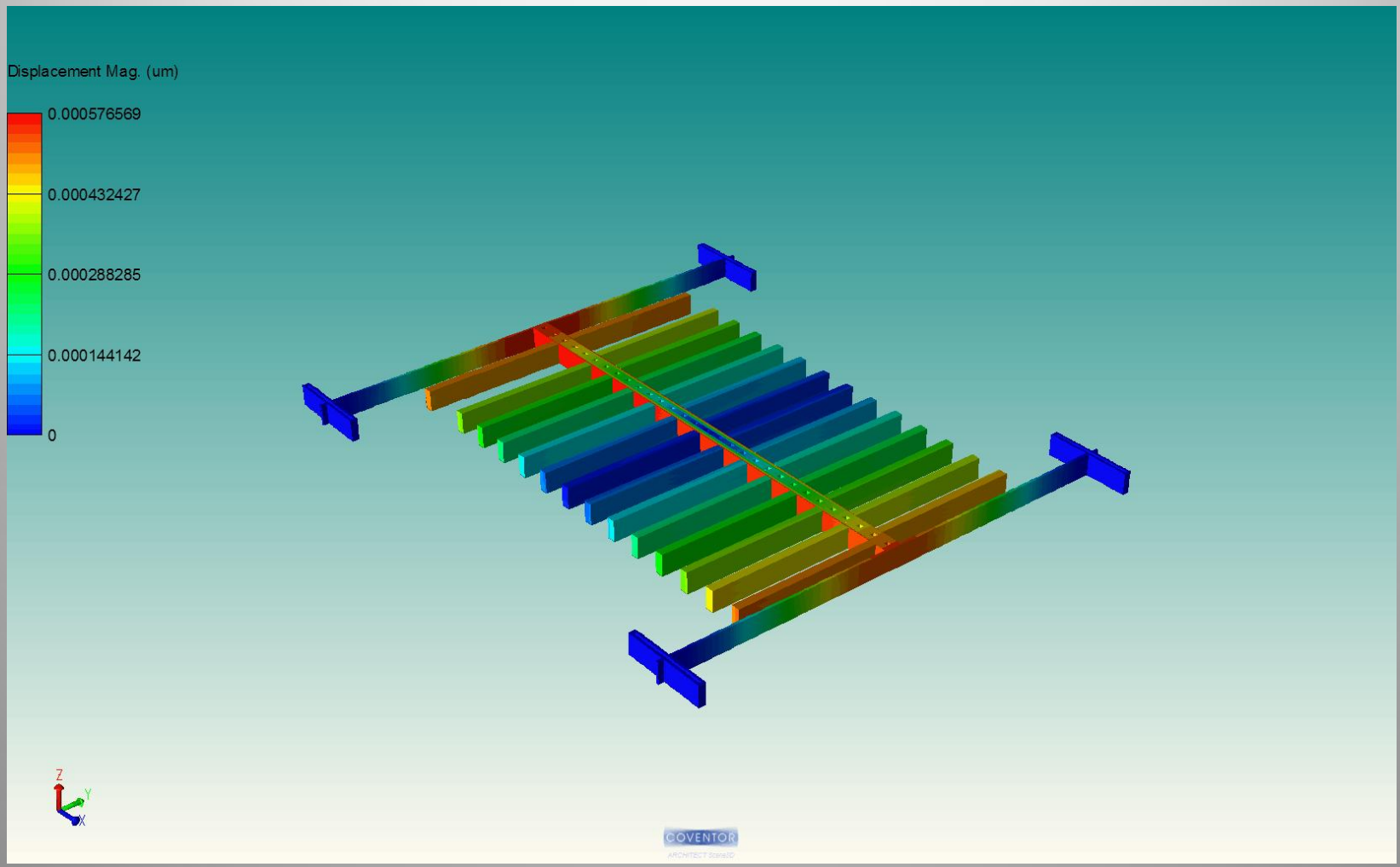
COVENTOR


Displacement Mag. (um)
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0
Z
Y
X
COVENTOR