Characterization and Modeling of Transistor Variability in Advanced CMOS Technologies

Cecilia Maggioni Mezzomo, Aurélie Bajolet, Augustin Cathignol, Regis Di Frenza, and Gérard Ghibaudo

***Abstract*—This paper aims at reviewing the results that we have obtained during the last ten years in the characterization and modeling of transistor mismatch in advanced complementary metal–oxide–semiconductor (CMOS) technologies. First, we review the theoretical background and modeling approaches that are generally employed for analyzing and interpreting the mismatch results. Next, we present the experimental procedures and methodologies that we used for characterizing the transistor matching. Then, we discuss typical matching results that were obtained on modern CMOS technologies and analyze the main variability (mismatch) sources. Finally, we conclude by summarizing our findings and giving some recommendations for future technologies.**

***Index Terms*—Characterization, matching, metal–oxide–semiconductor field-effect transistor (MOSFET), modeling.**

I. Introduction

THE CONTINUOUS miniaturization of silicon integrated circuits results in increasing variations in transistor parameters, which can be detrimental for analog and logic applications. Despite the efforts for controlling the extrinsic process variations, there exist intrinsic sources of dispersion in devices, which arise from stochastic variations inherent to the discrete nature of dopant impurities, point defects, or, more generally, random character of processing steps. As already emphasized in the 1970s, these stochastic variations become increasingly important as the device dimensions are scaled down, e.g., giving rise to threshold voltage variance varying as the reciprocal transistor area. This transistor mismatch might have significant impact not only on analog circuits but also on logic circuits, e.g., static random access memory (SRAM) or inverters. Thus, the variability issues are of paramount importance for current and future complementary metal–oxide–semiconductor (CMOS) technologies.

The mismatch in MOS transistors has been studied for more than three decades. One of the first investigations of the fluctuation effects was made in 1972 by Hoeneisen and Mead [1]. They noticed that possible limitations for the metal–oxide–semiconductor field-effect transistor (MOSFET) technology are due to the unpredictability in the threshold voltage because of substrate doping fluctuations. This problem was then discussed in 1975 by Keyes [2]. Using a discretization of the channel region, Keyes [2] formalized a model of predicting the amplitude of Vt variations, but without considering the operation of the transistor. McCreary [3] showed the dimensional dependency of metal–oxide–semiconductor (MOS) capacitance, which was explained by Shyu *et al.* [4]. At this point, the mismatch factors were already grouped as stochastic and systematic. The stochastic nature is associated with the standard deviations of a distribution, whereas systematic mismatch is related to its mean value. In a subsequent work, Shyu *et al.* [5] presented a more complete mismatch model for MOS capacitors and MOS transistors. It included the fluctuations in the physical dimensions of the active zone and in the process parameters as error's sources. The dimensional dependency equations presented in the Shyu *et al.*'s work were confirmed afterward. It is in 1986 that Lakshmikumar *et al.* [6] presented a paper exclusively about mismatch on MOS transistors. Lakshmikumar *et al.* experimentally observed the dimensional dependence for the mismatch in MOS devices. In 1989, one of the most cited papers in the field was published by Pelgrom *et al.* [7]. Different from the previous works, which start the analysis from the causes, their study makes a generically mathematical treatment of the mismatch between two transistors, where a parameter pp spatially varies. This paper explicitly demonstrates the dimensional dependence of electrical parameter fluctuations in MOS transistors. It points out that the standard deviation of δp is inversely proportional to the square root of the transistor area. Based on Pelgrom's law, several contributions have been made. The discrete model formalized by Keyes was rediscussed by Mizuno *et al.* [8]–[10], where they experimentally verified that the Vt mismatch is given by a Gaussian function and this distribution results from the doping fluctuations in the depletion region. The doping fluctuations then became very significant for the mismatch studies, particularly due to the decreasing feature sizes [11]–[15]. Other important contributions came from the mismatch atomistic simulations performed by Asenov's group at Glasgow University since the end of the 1990s [16]–[21].

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Other effects related to doping were studied, e.g., the halo or pocket implantation [22]–[25].

The measurement methodology, test structure, and layout issues on mismatch have extensively been studied by Tuinhout since 1994 [26]–[35]. The mismatch in the drain current was also thoroughly investigated. It has been represented by a contribution of the mismatch in the threshold voltage and gain factor. Bastos and Drennan [36]–[38] focused on the modeling of the drain current. Croon [39] also gave his contribution to its modeling.

Another source of intrinsic parameter fluctuations is the line edge roughness (LER). Since 2000, the LER and width gate roughness (LWR) have become critical factors for the mismatch study [40]–[44]. LER has caused little worry, because the critical dimensions of MOSFETs were orders of magnitude larger than the roughness. However, with the shrinking of transistors, LER does not accordingly scale, becoming a larger fraction of the gate length.

The impact of gate material has also been studied, particularly the effect of polysilicon granularity fluctuations [45]–[47]. Finally, note that, among this important list of fluctuations sources, Cathignol *et al.* [48] identified the percentage of each contribution for the 45-nm technology. They showed that the principal physical sources of fluctuations are the random discrete dopants (RDDs), the LER, and the polysilicon grain (PSG), where more than 60% of the mismatch is due to the RDD.

This paper aims at reviewing the results that we have obtained during the last ten years in the characterization and modeling of transistor mismatch in advanced CMOS technologies. This paper is organized as follows. In Section II, we summarize the theoretical background and modeling approaches that are generally employed for analyzing and interpreting the mismatch results. In Section III, we present the experimental procedures and methodologies that we used for characterizing the transistor matching. In Section IV, we present typical matching results that were obtained on modern CMOS technologies and discuss the main variability (mismatch) sources. Finally, we conclude by summarizing our findings and giving some recommendations for both technology and circuit design.

II. Theoretical Background and Modeling Aspects

A. Channel Mismatch

There are essentially two methods for the modeling of threshold voltage mismatch in MOS transistors. On one hand, following pioneering works [1], [2], [6], there is a nonlocal approach, in which the threshold voltage fluctuations in the whole device volume or surface stem from the random number of discrete entities controlling the Vt. These entities can be the channel or polysilicon gate doping impurities, the interface/oxide charges, and the material granularities. The randomness of these numbers are governed by a Poisson distribution law, implying that their variance is equal to their mean value [1], [2], [6]. On the other hand, following Shyu [5] and Pelgrom [7], a local approach can be adopted, in which a parameter p is characterized by a continuous distribution with space and a specific noise power intensity A_p, independent of the device surface area. Therefore, in the local approach, the variance of parameter p for a device with surface $W.L$ takes the form [7]

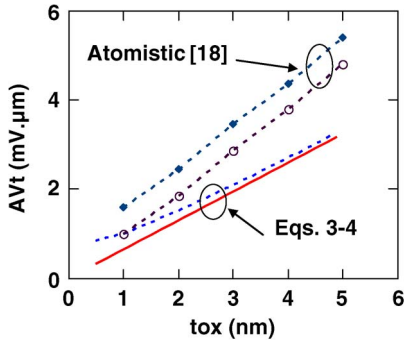

Fig. 1. Gate oxide thickness dependence of matching parameter $\mathrm{A_{Vt}}$, as given by the analytical models [see (3) and (4)] and atomistic simulations [18] (the parameters are $\mathrm{N}_a = 5 \times 10^{18}/\mathrm{cm}^3$ and $\mathrm{N}_d = 10^{20}/\mathrm{cm}^3$).

$$\sigma_p^2 = \frac{A_p^2}{WL}. \tag{1}$$

This equation is now known as the Pelgrom scaling law for matching.

Equation (1) can also be derived for the threshold voltage using the nonlocal approach by considering the random numbers of channel impurities controlling the depletion charge under the gate, yielding [6], [9], [12]

$$\sigma_{\mathrm{Vt}}^2 = \frac{1}{C_{\mathrm{ox}}^2}\frac{qQ_d}{4WL} \tag{2}$$

where Q_d is the channel depletion charge, and $\mathrm{C_{ox}}$ is the gate oxide capacitance per unit area. Equation (2) allows us to obtain the Vt matching parameter for the channel as [6], [9], [12]

$$A_{\mathrm{Vtch.}} = \frac{t_{\mathrm{ox}}}{\varepsilon_{\mathrm{ox}}}\frac{\sqrt[4]{2q\varepsilon_{\mathrm{si}}N_a(2\Phi_f - V_b)}}{2} \tag{3}$$

where $\varepsilon_{\mathrm{ox,si}}$ is the oxide/silicon permittivity, $\mathrm{t_{ox}}$ is the gate oxide thickness, N_a is the channel doping concentration, V_b is the body bias, and $\Phi_f = \mathrm{kT/q.\ln(N}_a/\mathrm{n}_i)$ is the Fermi potential (with kT/q being the thermal voltage and n_i the intrinsic carrier concentration).

B. Polysilicon Gate Mismatch

In the case of polysilicon gate, the contribution to matching can be derived by considering that there is an extra potential drop at the oxide/poly interface, equal to $2\Phi_f.\mathrm{N}_a/\mathrm{N}_d$ (with N_d being the polydoping concentration), giving rise to an additional term in Vt. Again assuming a Poisson law distribution for the number of dopants in the gate polysilicon depletion layer yields the global $\mathrm{A_{Vt}}$ parameter [45]

$$A_{\mathrm{Vt}} = \sqrt{\frac{t_{\mathrm{ox}}^2}{\varepsilon_{\mathrm{ox}}^2}\cdot\frac{qQ_d}{4} + (2.\Phi_f - V_b)\cdot\frac{N_a}{N_d}\cdot\frac{q}{Q_d}}. \tag{4}$$

The variations of the matching parameter $\mathrm{A_{Vt}}$, with the gate oxide thickness given by (3) and (4) and provided by atomistic simulations [18], are shown in Fig. 1, indicating that such

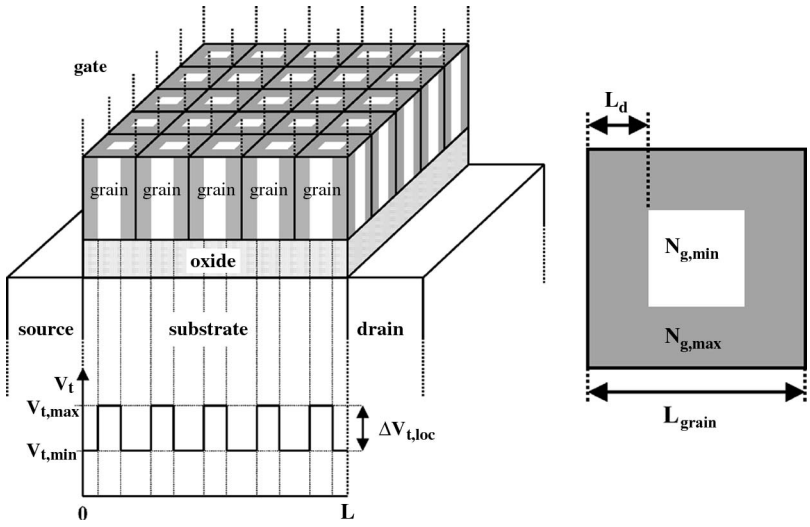

Fig. 2. Schematic of nonuniform doping distribution in squared geometry polysilicon grains [45].

analytical models give reasonable trends. Based on atomistic simulations, Asenov [18] has proposed an empirical compact formula for the matching parameter

$$A_{\mathrm{Vt}} = 3.2 \times 10^{-3} \cdot N_a^{0.4} \cdot \left(t_{\mathrm{ox}} + \frac{\varepsilon_{\mathrm{ox}}}{\varepsilon_{\mathrm{si}}} \cdot t_{\mathrm{pol}} \right) \quad (\mathrm{mV}.\mu\mathrm{m} \text{ for } \mathrm{N}_a, \mathrm{t_{ox}}, \text{ and } \mathrm{t_{pol}} \text{ in cgs units}) \quad (5)$$

where $\mathrm{t_{pol}}$ is the depletion layer width in the polysilicon gate.

As experimentally demonstrated, the polysilicon gate can strongly impact MOS transistor matching performances [49]. Indeed, the preferential dopant diffusion along grain boundaries (GBs) could lead to nonuniform dopant concentration in the gate and, in turn, to local threshold voltage variations. Based on these considerations, a Vt matching model has been developed, taking into account the nonuniform dopant concentration in each grain ($\mathrm{N}_{d,\min}$ and $\mathrm{N}_{d,\max}$) and the random number of grains in the gate for a simplified squared geometry (see Fig. 2) [45]. This model further assumes a local Vt variation between $\mathrm{V}_{t,\min}$ and $\mathrm{V}_{t,\max}$ correlated to the maximum and minimum polydoping levels, respectively, finally yielding for the global $\mathrm{A_{Vt}}$ parameter [45]

$$A_{\mathrm{Vt}} = \sqrt{A_{\mathrm{Vtch}}^2 + A_{\mathrm{Vt,Ngrain}}^2} \quad (6)$$

with

$$A_{\mathrm{Vt,Ngrain}} = (2 \cdot \Phi_f - V_b) \cdot \left(\frac{N_a}{N_{d,\min}} - \frac{N_a}{N_{d,\max}} \right) \cdot \left(2 \cdot L_d - 4 \cdot L_d^2 \cdot \sqrt{N_{\mathrm{grain}}} \right) \quad (7)$$

where L_d is the characteristic distance of dopant enhancement in the grain (see Fig. 2).

More recently, an analysis of the impact of a single GB in the poly-Si gate on MOS devices has been proposed [46]. It has been demonstrated that a single GB in the polygate can induce a significant threshold voltage shift ΔVt, depending on the GB interface charge and position along the channel. By taking into account such an elementary ΔVt induced by a single grain and the random number of grains in the gate, the matching parameter $\mathrm{A_{VtGB}}$ contributed by the GB distribution has been evaluated as [46]

$$A_{\mathrm{VGBt}} = \frac{8}{3} \frac{\varepsilon_{\mathrm{si}} Pin^{3/2}}{\sqrt{q \varepsilon_{\mathrm{si}} Nd}} \quad (8)$$

where Pin is the Fermi pinning potential at the GB. This potential, which depends on the trap density $\mathrm{N_{it}}$ at the GB, saturates around 0.4–0.5 V for Nit = 3–5 $\times 10^{14}$/eVcm^2, giving $\mathrm{A_{VtGB}}$ values in the range 1–1.7 mV.μm for $\mathrm{N}_d = 5 \times 10^{18}$–$10^{20}$/cm^3 [46] in reasonable agreement with atomistic simulation results [47], [48].

C. Pocket or Halo Mismatch

The use of pockets and halos in modern CMOS technologies for short channel effect (SCE) control should lead to an increase of the mismatch. The modeling of mismatch in devices with pocket implants has first been conceived based on the weighted summation of the variances associated with the channel and pocket regions, which yields, using (2), the matching parameter $\mathrm{A_{Vtpoc}}$ given by [23], [25]

$$A_{\mathrm{Vpoc}\cdot} = \sqrt{\frac{1}{C_{\mathrm{ox}}^2} \frac{qQ_{\mathrm{dpoc}}}{4} \cdot \frac{2L_{\mathrm{poc}}}{L} + \frac{1}{C_{\mathrm{ox}}^2} \frac{qQ_{\mathrm{dch}}}{4} \cdot \frac{L - 2L_{\mathrm{poc}}}{L}} \quad (9)$$

where $\mathrm{Q_{dpoc(ch)}}$ is the pocket (channel) depletion charge, and $\mathrm{L_{poc}}$ is the pocket length (with the constraint $2\mathrm{L}_p < \mathrm{L}$). Equation (9) allows for explaining, to some extent, the increase of matching parameter at a short channel length for devices with pockets [23], [25].

However, this model has shown strong limitations in sub-65-nm CMOS technologies, where a very high-doping-level contrast exists between the low-doped channel and the heavily doped pocket regions [50]. Indeed, it cannot explain the abnormal increase of V_t mismatch observed for intermediate gate lengths. Thus, an improved matching model for devices with pockets has been developed in the linear regime, considering a series three-transistor approach [51]. In this case, it has been

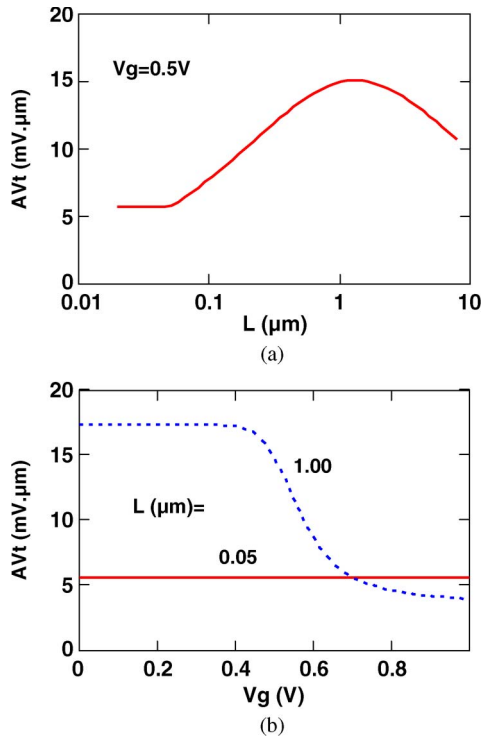

Fig. 3. Variations of matching parameter A_{Vt} with (a) gate length and (b) gate voltage as obtained from (10) (main parameters: $N_a = 3 \times 10^{16}/cm^3$, $N_{poc} = 2 \times 10^{17}/cm^3$, and $t_{ox} = 1.5$ nm).

shown that the whole device matching parameter can be expressed as (10), shown at the bottom of the page, where $R_{tot} = R_{ch} + 2.R_{poc}$ is the whole transistor resistance, R_{ch} (R_{poc}) is the channel (pocket) resistance, and A_{ch} (A_{poc}) is the channel (pocket) local V_t matching parameter. This model, which is continuous from weak to strong inversion, allows for evaluating the matching parameter not only in strong inversion as shown in (9) but also around and below the threshold. It also explains the increase and then the decrease of the matching parameter as a function of gate length and its gate voltage dependence, as illustrated in Fig. 3 and inferred by the experiments (see Section IV) [50], [51].

D. Drain Current Mismatch

The drain current matching has first been modeled by simply accounting for V_t fluctuations and additional gain factor mismatch, yielding [6], [36], [52]

$$\frac{\sigma^2_{Id}}{I_d^2}. = \left(\frac{g_m}{I_d}\right)^2 \cdot \sigma^2_{Vt} + \frac{\sigma^2_\beta}{\beta^2} \tag{11}$$

where g_m is the transconductance.

A more general drain current mismatch model has recently been developed based on a low-frequency noise approach [53]. To this end, the impact of a local Vt shift δV_t in a portion of the channel, of area δa, on the relative drain current change (due to a weak local conductivity variation $\delta\sigma$) has been evaluated as in RTS calculations [53] as

$$\frac{\Delta Id}{Id} = \frac{\delta a}{WL} \cdot \frac{\delta\sigma}{\sigma} = \frac{1}{\sigma}\frac{\partial\sigma}{\partial Vt} \cdot \frac{\delta a}{WL} \cdot \delta Vt. \tag{12}$$

Integrating these fluctuations over the channel surface yields the drain current variance

$$\sigma^2_{\frac{\Delta Id}{Id}} = \int \left(\frac{\partial \ln(\mu_{eff} Q_i)}{\partial Vt}\right)^2 \cdot \frac{A^2_{Vt}}{WL} \cdot dxdy \tag{13}$$

where A_{Vt} is the local V_t mismatch parameter, μ_{eff} is the mobility, and Q_i is the inversion charge. Within the gradual channel approximation, accounting for current conservation along the channel enables the drain current variance to be equated to

$$\sigma^2_{\frac{\Delta Id}{Id}} = \int_0^{Vd} \left(\frac{\partial \ln(\mu_{eff} Q_i)}{\partial Vt}\right)^2 \cdot \frac{A^2_{Vt}}{WL} \cdot \mu_{eff} \cdot Q_i \cdot dUc \Big/ \int_0^{Vd} \mu_{eff} \cdot Q_i \cdot dUc. \tag{14}$$

This model therefore allows the drain current mismatch not only to be evaluated in the linear regime, as with (11), but also to be a function of drain voltage in the nonlinear region [53]. Fig. 4 shows typical variations of the matching parameter $A_{Vt} \equiv \sigma_{\Delta Vt}\sqrt{WL} = (\sigma_{\Delta Id}/I_d)/(g_m/I_d).\sqrt{WL}$ as a function of drain voltage V_d obtained using (14) for the following three cases: 1) V_t fluctuations and constant mobility; 2) V_t fluctuations and universal mobility law with effective electric field $\mu_{eff}(E_{eff})$; and 3) δV_t and correlated mobility $\mu_{eff}(E_{eff})$ fluctuations. Note the strong impact of correlated mobility fluctuations on the matching behavior with drain voltage. This point will be illustrated in Section IV.

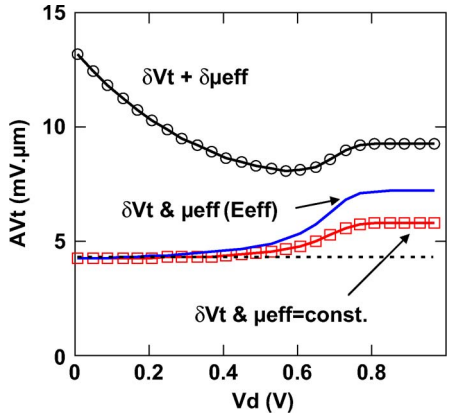

Fig. 4. Variation of normalized matching parameter A_{Vt} with drain voltage Vd (parameters: $Na = 1017/cm^3$, tox = 1.5 nm, L = 0.2 μm, and Vg − Vt = 0.5 V).

$$A_{Vt}(Vg) = \sqrt{\left(\frac{\partial R_{ch}}{\partial Vg}/\frac{\partial R_{tot}}{\partial Vg}\right)^2 \frac{A^2_{ch}.L}{(L-2L_{poc})} + 2\left(\frac{\partial R_{poc}}{\partial Vg}/\frac{\partial R_{tot}}{\partial Vg}\right)^2 \frac{A^2_{poc}.L}{L_{poc}}} \tag{10}$$

III. Experimental Procedures and Methodologies

A. General Remarks

The experimental methodology for matching characterization consists of measuring a pair of identically designed devices, as symmetrical as possible, separated by a (quasi) minimal design rule and placed in the same environment. For each device, an electrical parameter p is characterized. Considering δp (δp = Δp or Δp/p), the difference of parameter p measured between the two paired devices, matching the characterization studies, result in evaluating both the mean δp and the standard deviation $\sigma(\delta \mathrm{p})$ from δp Gaussian distribution.

Once the extraction has been done, data filtering is the first step to get rid of erroneous values. For this step, a recursive filter is used to eliminate all values outside the $\pm 3\sigma$ interval. To ensure an acceptable statistical accuracy of matching measurements, at least 70 pairs of transistors are measured. Then, the systematic (mean δp) and stochastic ($\sigma(\delta \mathrm{p})$) mismatch can be obtained. In this paper, we are interested in the stochastic mismatch, which represents the local process fluctuations. To avoid systematic mismatch, specific design techniques are used, e.g., the presence of polydummies on each side of the MOS transistor [31].

In our case, the threshold voltage parameter Vt is extracted by the Id–Vg extrapolation method at the maximum of transconductance, with |Vg| varying from 0 V to 1.1 V by 25-mV steps, constant |Vd| = 50 mV, and 1.1 V, depending on the technology supply voltage.

B. Improved Procedure for A_{Vt} Extraction

As previously indicated, transistor matching follows the dimensional scaling law [see (1)]. Considering the electrical parameter p, matching characterization consists of measuring Δp for n pairs of transistors and $\mathrm{n_{geo}}$ geometries. Then, from such measurements, Δp dispersion is estimated $\sigma_{\Delta p}$ for each geometry, and finally, A_p is evaluated by linear regression using the scaling law equation. Therefore, the knowledge of the A_p dispersion σ_{Ap} is essential for a correct physical analysis based on such matching parameter data.

The classical methodology of estimating A_p relies on the use of conventional linear regression applied to $\sigma_{\Delta p}$ versus $1/\sqrt{WL}$ data plots. Note that linear regression is usually forced to intercept the origin, because the mismatch converges to zero as the area increases. This classical methodology is illustrated in Fig. 5(a).

Therefore, for a given device area $\sigma_{\Delta p}$ is estimated from a limited number of samples, which gives rise to a source of dispersion. It can be shown from basic statistics that the variance of $\sigma_{\Delta p}$ estimator due to sampling limitation is given by [54]

$$\mathrm{var}(\sigma_{\Delta p})_{\mathrm{sampling}} = \frac{\sigma_{\Delta p}^2}{2(n_{\mathrm{pairs}} - 1)}. \tag{15}$$

Because $\sigma_{\Delta p}$ is not precisely known due to the finite number of samples, A_p is therefore subjected to a random uncertainty

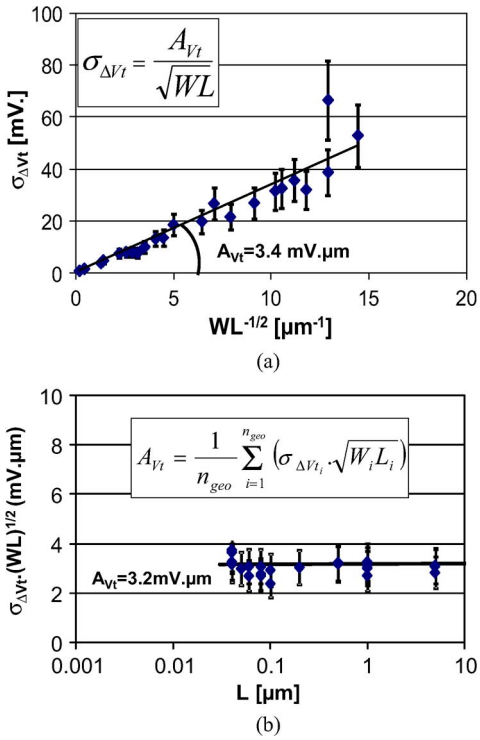

Fig. 5. (a) Typical $\sigma_{\Delta \mathrm{Vt}}$ versus $1/\sqrt{WL}$ plot for the classical $\mathrm{A_{Vt}}$ extraction from linear regression. (b) $\sigma_{\Delta \mathrm{Vt}}.\sqrt{WL}$ versus the L plot for $\mathrm{A_{Vt}}$ extraction from the new procedure.

whose variance has been calculated as [54]

$$\sigma_{\mathrm{Ap}}^2\big|_{\mathrm{class}} = \frac{\sum_{i=0}^{n_{\mathrm{geo}}-1} (1/\sqrt{W_i L_i})^2 \sigma_{\Delta p_i}^2}{2(n_{\mathrm{pairs}} - 1)\left[\sum_{i=0}^{n_{\mathrm{geo}}-1} (1/\sqrt{W_i L_i})^2\right]^2}. \tag{16}$$

To minimize this sampling dispersion, a new methodology has been proposed for A_p evaluation. In fact, it has been suggested to weight each $\sigma_{\Delta \mathrm{pi}}$ by the inverse of the variance before computing the linear least square fit. This method is equivalent to evaluating A_p for each geometry as $A_{\mathrm{pi}} = \sigma_{\Delta \mathrm{pi}}.\sqrt{W_i L_i}$. It was proved that the mean value and variance of A_p are given by [54]

$$A_p = \frac{1}{n_{\mathrm{geo}}} \sum_{i=1}^{n_{\mathrm{geo}}} \left(\sigma_{\Delta p_i} \cdot \sqrt{W_i L_i}\right) \tag{17}$$

$$\sigma_{\mathrm{Ap}}^2\big|_{\mathrm{new}} = \frac{\sum_{i=0}^{n_{\mathrm{geo}}-1} \left(\sigma_{\Delta p_i} \cdot \sqrt{W_i L_i}\right)^2}{2(n_{\mathrm{pairs}} - 1) n_{\mathrm{geo}}^2}. \tag{18}$$

It was shown that the ratio between (18) and (16) is always lower than one (the Cauchy–Schwarz inequality), i.e., as shown in Fig. 5(b), this new procedure induces less sampling errors than the classical linear regression plot. For instance, for the data in Fig. 5, the error in $\mathrm{A_{Vt}}$ (chosen, in this case, at three times the standard deviation of the estimated $\mathrm{A_{Vt}}$) determination is decreased from 0.11 mV.μm to 0.07 mV.μm by using this procedure.

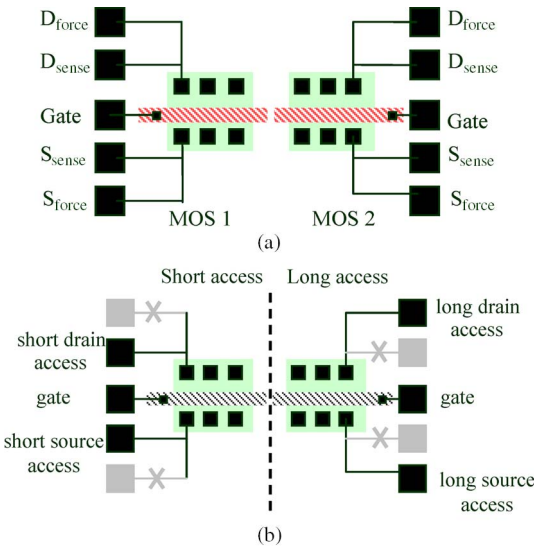

Fig. 6. (a) Dedicated mismatch test structure using the Kelvin method. (b) Schematic of the Kelvin test structure used as the standard mismatch structure. Left: Definition of conventional structure with short access. Right: Definition of conventional structure with long access.

C. Limitations of Dedicated Test Structures

The usual test structures for matching measurements consist of paired transistors. One question that has been raised is the possible impact of series-parasitic resistances in the extraction of the MOSFET matching parameters. To study this effect, a dedicated mismatch test structure based on the four-terminal Kelvin method has been proposed. Recently, Kuroda *et al.* [55], [56] has studied the characterization of transistor performance using Kelvin test structures on fully depleted silicon-on-insulator (SOI) MOSFET. They analyzed the short-channel-transistor intrinsic current–voltage characteristics and the quantitative effects of the series-parasitic resistance in the device performance. Next, Terada *et al.* [57] used the Kelvin test structure on MOSFET devices to study the drain current variation under high gate voltage. Their analysis is made using arrays circuits, which were also used in [58]. Then, Mezzomo *et al.* [59] analyzed the extraction of threshold voltage, gain factor, and drain current local fluctuations using a dedicated test structure based on the Kelvin method on transistor pair configuration (see Fig. 6).

The difference between the Kelvin mismatch test structure and the standard method is that the drain and the source have two connections called force and sense terminals. These two additional terminals allow the measurement of the effective biasing applied to the device. In addition, an algorithm is used to correct the transistor biasing by compensating for the potential drops caused by the parasitic resistances.

To observe if external access resistances have an effect in transistor mismatch, the Kelvin mismatch test structure is used in the following three different ways [see Fig. 6(b)]: 1) as Kelvin mismatch structure, where it has force and sense terminals to the drain and to the source, and an algorithm is then used to compensate for the potential drops; 2) as conventional structure with short access, where the closest drain/source connections to transistor channel are used; and 3) as conventional structure with long access, where the longest drain/source connections to the transistor channel are used. In this case, the access resistances are higher than in the second case.

TABLE I
TRANSISTOR GEOMETRIES FOR NMOS AND PMOS DEVICES AND THEIR RESPECTIVE OXIDE THICKNESS AND DRAIN BIAS CONDITIONS

W (μm)	L (μm)	Tox (A°)	V_{dd} (V)
10	0.15	17	1.1
5	0.15	17	1.1
10	0.27	32	1.8

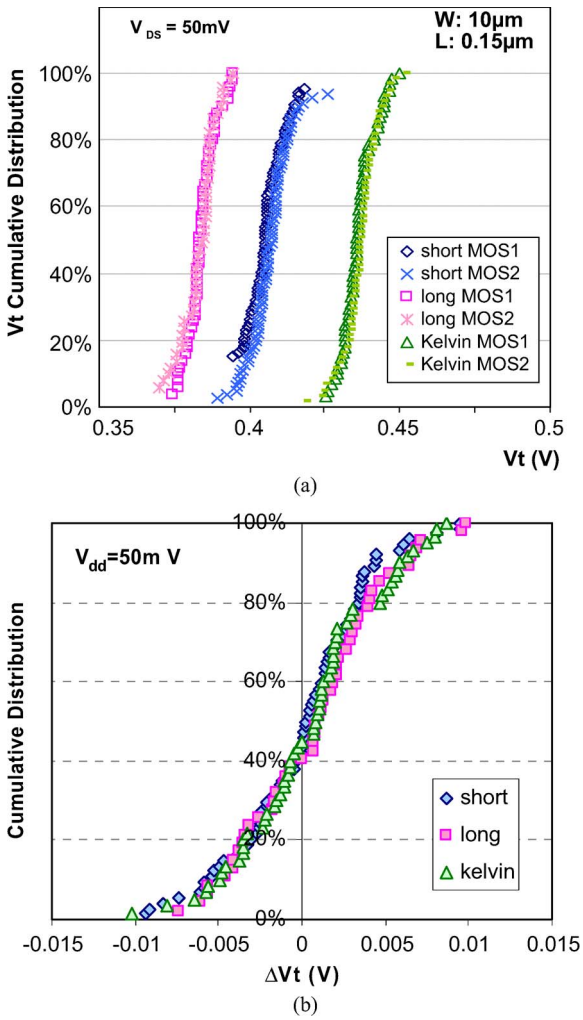

Fig. 7. (a) Cumulative distribution of Vt for transistors 1 (MOS1) and 2 (MOS2) for the conventional structure using short and long access and Kelvin structures. (b) Cumulative distribution of ΔVt for the conventional structure using short and long access and Kelvin structures.

The threshold voltage and the drain current mismatch are then characterized and discussed. Both n-channel MOSFET (NMOS) and p-channel MOSFET (PMOS) devices have been measured for three different geometries, as shown in Table I.

The Vt experimental results for the three studied test structures are shown in Fig. 7(a) for the NMOS transistor with the highest W/L ratio. It points out that Vt values are not the same for the conventional and Kelvin test structures. This case demonstrates that Vt extraction is affected by external access resistances. The conventional structure with long paths has the lowest Vt, because it has the highest access resistance; thus, the highest voltage drops. Analyzing the Vt local fluctuations,

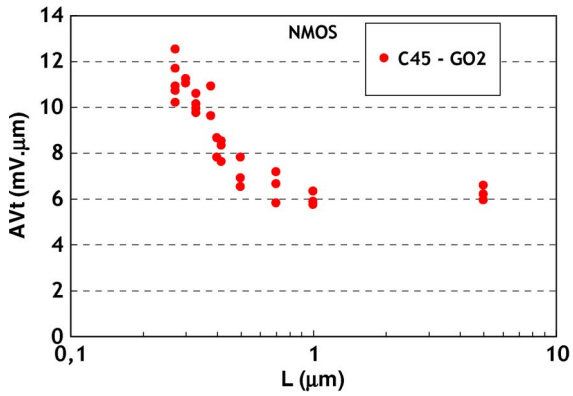

Fig. 8. Variation of matching parameter A_{Vt}, with the channel length illustrating SCE.

although there is a Vt shift between the test structures, the mismatch of Vt is not affected [see Fig. 7(b)]. It is possible to notice the ΔVt curves that correspond to the three test structures are superimposed. These same tendencies have been observed for NMOS and PMOS devices.

The relative drain current fluctuations have also been analyzed. It has been shown that the external access resistances have more effect in devices with high current and, thus, with a high W/L ratio. Moreover, it is has been found that, as Id increases, the drain current matching was underestimated, particularly for the structure with higher access resistances when not using the Kelvin method. However, for this 45-nm technology, these discrepancies are, in general, not significant. Therefore, the use of the conventional test structure is generally appropriate for matching studies in the current technology. However, the external access resistances have to carefully be taken into account for a high W/L ratio.

IV. Matching Results and Discussions

A. Threshold Voltage Mismatch

Threshold voltage mismatches have been characterized for the sub-65-nm bulk-MOSFET from the STMicroelectronics technology. According to the matching scaling equation (1), the threshold voltage mismatch should be inversely proportional to the square root of the active transistor surface [7]. Therefore, the normalized mismatches $A_{Vt} = \sigma(\Delta V_t)\sqrt{WL}$ have been analyzed as a function of gate length or gate area for different MOS transistor architectures. One example of the gate length dependence of the matching parameter A_{Vt} is shown in Fig. 8, illustrating SCEs with a huge increase at a small channel length.

For transistors with pocket implants from the 65-nm technology, it should be noticed in Fig. 9(a) that, for small gate lengths, Pelgrom's law is followed, i.e., A_{Vt} is nearly constant. For longer gate lengths, the normalized mismatch increases, i.e., the scaling law is no longer verified. This anomalous matching effect is progressively eliminated by decreasing the pocket implant dose, as shown in Fig. 9(a). For the 45-nm technology [Fig. 9(b)], the same behavior occurs at a small length, and then, the mismatch passes through a maximum before decreasing for the longest transistors, which is in good agreement with the model in (10).

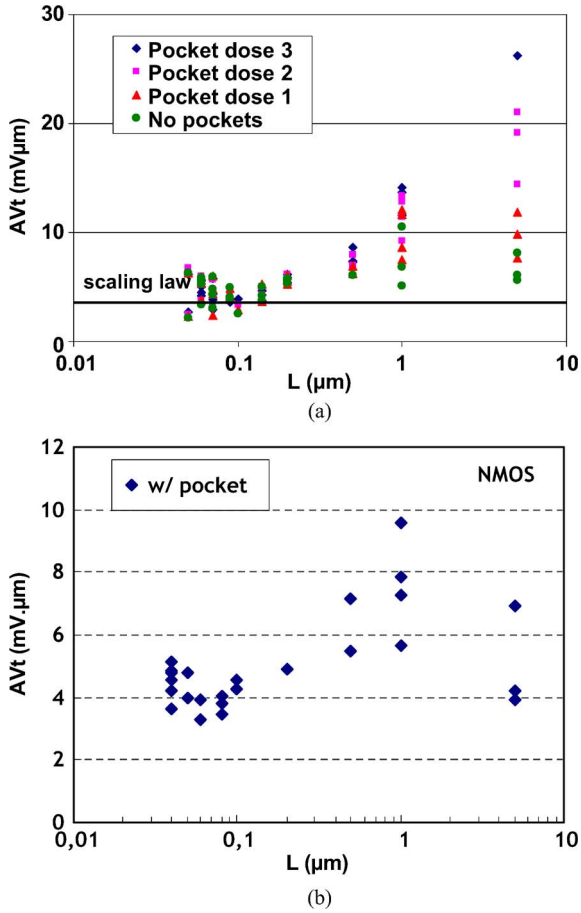

Fig. 9. Variation of matching parameter A_{Vt} with channel length for transistors with pocket implants from (a) 65-nm (various doses) and (b) 45-nm CMOS technologies.

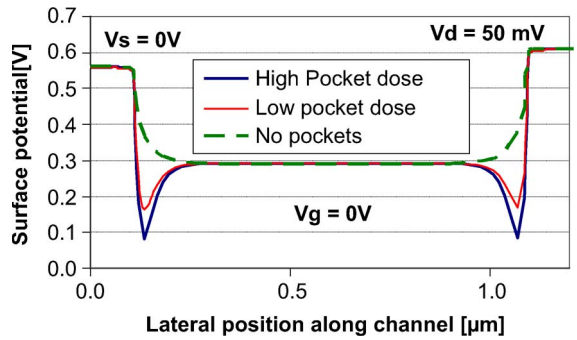

Fig. 10. Surface potential for various pockets doses at Vd = 50 mV, Vs = 0 V, and Vg = 0 (cf., [50]).

Contemporaneously, Johnson *et al.* [60] similarly showed that for 65-nm transistors with pocket implants, the matching parameter increases with an increasing channel length and is the largest for devices with the largest lengths. The key reason for this phenomenon had been pointed out in [15], which mentioned a shrunk control area for longer devices with strong-enough halos. For the 65-nm heavily doped pocket MOSFET technology, Cathignol *et al.* [50] proposed a qualitative physical-based model and have explained this anomalous behavior. They showed that the rather-long devices present strong potential barriers at both the source and the drain, giving these barriers a major role in Vt controlling (see Fig. 10). Because

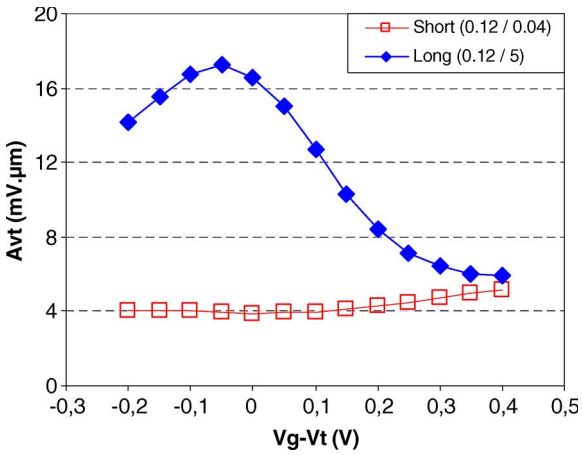

Fig. 11. Gate voltage variation of matching parameter from weak to strong inversion regions at Vd = 50 mV.

the potential barriers totally control Vt independent of the gate length, the Vt mismatch is also independent on the length, and the mismatch keeps constant with an increasing length. Thus, if the mismatch is normalized by the square root of the transistor area, it increases with an increasing length. In addition, it was shown that this effect is highly dependent on the gate bias: indeed, although the level is quite severe below and around the threshold voltage, it is significantly lowered as the device gets in stronger inversion.

The unexpected increase of mismatch for long devices has also been reported in [61] for a 32-nm high-k metal gate technology. This result confirms that this effect is induced by pocket implants.

On the 45-nm technology [51], the mismatch decreases for very long transistors, as shown in Fig. 9(b). For very long lengths, the source and drain pockets are outspread, making the channel area much bigger than the pocket area. Then, because the channel area has a weak doping, the Vt fluctuations decreases. This behavior has well been interpreted by the model in (10) (see Fig. 3) based on a series three-transistor approach [51]. Note that the simple strong inversion model in (9) cannot reproduce this behavior. For short transistors, the pocket resistances are predominant, controlling the total resistance of the transistor. For L $>$ 0.1 μm, the pocket regions become separated, and a nonhomogeneous channel is formed. For relatively long transistors, the pocket resistances are still predominant, and then, fluctuations increase with an increasing length. For very long transistors, the mismatch decreases due to vanishing pocket resistance contributions. In this case, the channel resistance is predominant. Then, the mismatch tends to channel fluctuations.

B. Mismatch From Weak to Strong Inversion Regions

The mismatch has been also analyzed as a function of gate voltage from weak to strong inversion regions in such MOS devices with pockets. Fig. 11 shows typical gate voltage variations of matching parameter for short and long channels. For the short channel (W/L = 0.12 μm/0.04 μm), the matching parameter is almost independent of Vg, as it would be in devices without pocket implants. This condition is because the pocket regions overlap, and therefore, the channel is uniformly doped. In contrast, for the longest transistor (W/L = 0.12 μm/5 μm), the channel is strongly nonhomogeneous, and an increase of mismatch is observed when the gate voltage decreases.

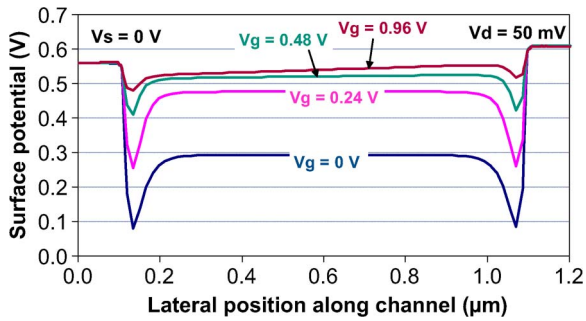

Fig. 12. Impact of gate voltage on surface potential for an NMOS transistor with high pocket dose implanted (cf., [50]).

This peculiar matching behavior as a function of gate bias has been explained by additional potential barriers near the source and drain regions due to pocket implants [50]. Fig. 12 shows the surface potential as a function of the lateral position along the channel for various gate voltages. As gate biasing becomes higher, the barrier height decreases, and its ability to control the current flow becomes lower, making the device with pocket implants similar to a device without pocket. Note that this mismatch gate voltage dependence has semiquantitatively been well accounted for by the series three-transistor model in (10) [51].

C. Mismatch From Linear to Saturation Regions

Mismatch analysis has been performed only in the linear regime. In this section, the mismatch characteristics from linear to saturation regions are investigated. To this end, drain current mismatch has been measured as a function of drain voltage and then normalized into the Vt matching parameter as $\sigma(\Delta V_t) = \sigma(\Delta I_d/I_d)/(g_m/I_d)$. Then, devices with and without pocket implants have been characterized (see Fig. 13). Note that, in agreement with the model presented in Section II [see Fig. 4 and (14)], a significant dependence for small drain bias conditions is observed, particularly for high gate bias. Only the case that considers correlated doping-mobility fluctuations can interpret the real characteristic of transistors with a homogeneous channel. For devices with pocket implants, a clear hump is observed in the nonlinear region due to the presence of heavily pocket implants, which is not explained by the model in (10) and is valid only for uniformly doped channel devices [51].

D. Impact of the Polysilicon Structure

The polysilicon structure has been shown to significantly impact the transistor mismatch [45], [49], [62]. Here, we illustrate this effect on the matching results obtained on large area devices (W $>$ 1.4 μm, L $>$ 0.5 μm) to minimize the impact of SCE, pockets, or polysilicon LER on matching characteristics. Table II gives some details about the variations in gate

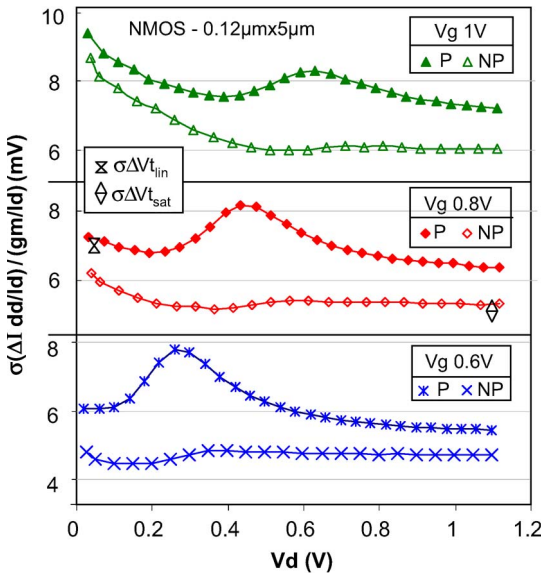

Fig. 13. Gate fluctuations for the transistor with and without pocket implants. The Vt fluctuations extracted in the linear ($\sigma(\Delta \mathrm{Vt_{lin}})$, Vd = 50 mV) and the saturation ($\sigma(\Delta \mathrm{Vt_{sat}})$, Vd = 1.1 V) regions are also represented.

TABLE II
MATCHING PARAMETER $\mathrm{A_{Vt}}$ FOR DIFFERENT POLYSILICON GATE ENGINEERING

Gate engineering	$\mathrm{A_{Vt}}$ (mV.µm)	
	NMOS	PMOS
Process A: amorphous Si deposition + furnace anneal	6.08	11.2
Process B: amorphous Si deposition + RTO anneal	5.31	4.52
Process C: poly-Si deposition + RTO anneal	3.46	2.85

processes A, B, and C. In Fig. 14, we observe that the gate process can significantly influence the V_t mismatch. The first drop of MOSFET mismatch is observed when furnace anneal is replaced by rapid thermal oxidation (RTO). Moreover, MOS transistor matching performances are enhanced when amorphous Si deposition is replaced by polycrystalline deposition. This matching improvement has clearly been related to the reduction of PSG size, which induces better gate dopant uniformity [62]. The body bias dependence of the matching has also been studied (see Fig. 15) and relatively well explained by the model in (7) [45] and not in (4), clearly emphasizing the prevailing role of GB number fluctuations.

E. Correlation Between Matched Transistors

Note that the link between mismatch $\sigma(\Delta \mathrm{p})$ and device correlation $\rho(\mathrm{p}_1, \mathrm{p}_2)$ is given by (19), assuming $\sigma(\mathrm{p}_1) \approx \sigma(\mathrm{p}_2) = \sigma(\mathrm{p})$, which is verified by

$$\sigma^2(\Delta p) = 2\sigma^2(p)\left(1 - \rho(p_1, p_2)\right). \tag{19}$$

When spacing increases, gradients at the die level induce a decrease of device correlation and, consequently, a degradation of matching. The correlation value is also function of device

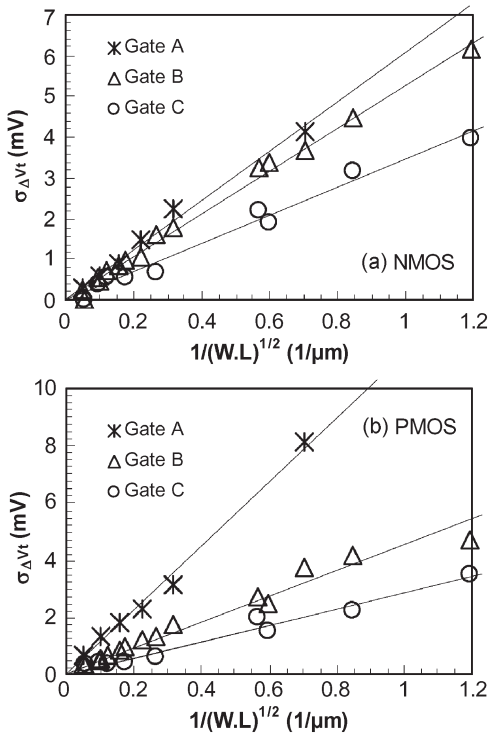

Fig. 14. Threshold voltage mismatch for (a) NMOS and (b) PMOS transistors versus $1/(\mathrm{W.L})^{1/2}$ for gate processes A, B, and C ($\mathrm{V}_b = 0$ V) (symbols = experimental data, lines = linear regression).

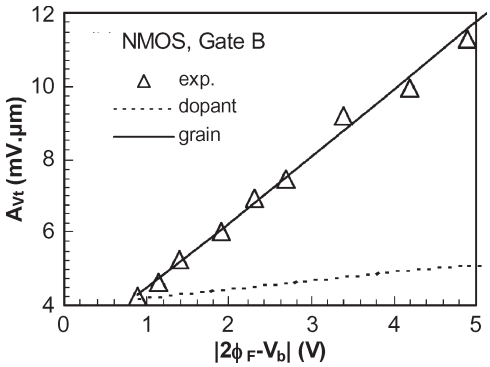

Fig. 15. Evolution of matching parameter $\mathrm{A_{Vt}}$ with bulk bias for gate process B and [dashed line = random variations of the dopant number in the channel and the gate (4), and solid line = random variations of the dopant number in the channel and grain number in the gate (7)].

area: devices get more correlated as their area increase, and the variance of their mismatch is therefore lower than twice the variance of a single device. Starting from few assumptions with regard to the contribution of local and global fluctuations to mismatch, Cathignol [63] expressed device correlation as a function of device area and spacing.

It is considered that p_1 and p_2 are the sums of a local (x) and a position-dependent (z) contribution, i.e.,

$$\begin{aligned} p_1 &= A/\sqrt{2WL} \cdot x_1(0,1) + z_1(p_{10}, G) \\ p_2 &= A/\sqrt{2WL} \cdot x_2(0,1) + z_2(p_{20}, G) \end{aligned} \tag{20}$$

where $\mathrm{x}(\mu, \sigma)$ and $\mathrm{z}(\mu, \sigma)$ are normally distributed with mean μ and standard deviation σ, A is the mismatch coefficient of the Pelgrom model [7], i.e., (1), W and L are the device width and

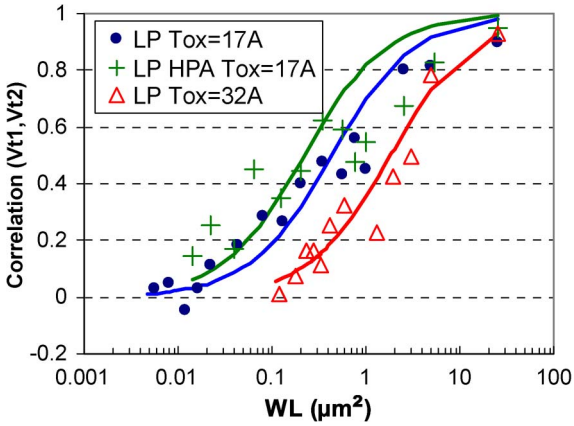

Fig. 16. Experimental and modeled correlation between threshold voltages of both devices of a matched pair as a function of device area for several CMOS technologies.

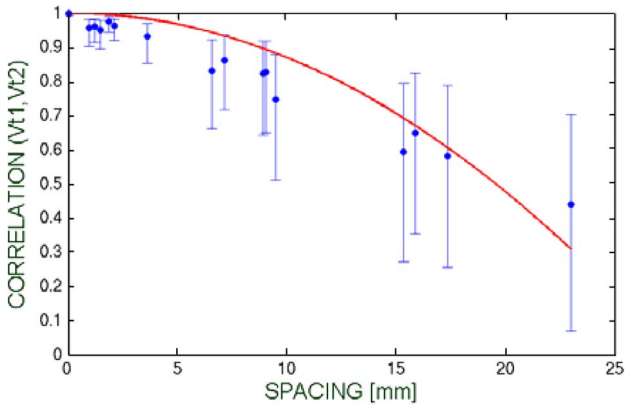

Fig. 17. Experimental Vt correlation versus spacing for p-channel transistor pairs from the 45-nm technology (device area = 450 μm^2) with 99% confidence bars. The solid line represents the model in (23), with coefficients A = 4.8 mV.μm, G = 2.18 mV, and S = 0.11 mV/μm.

length, respectively, z_1 and z_2, which are position dependent, represent the simplicity $z_{r1\theta1}$ and $z_{r2\theta2}$, where r and θ are the coordinates of the two devices on the wafer, $p_{10}(p_{20})$ is the average of $p_1(p_2)$ on the considered wafer, x_1 and x_2 are not correlated, because they describe a random process, z and x are not correlated, because they depict fluctuations that act on different scales, and the correlation between z_1 and z_2 depends on the transistor geometry and spacing.

At minimum spacing, z_1 and z_2 are physically very close (at the wafer scale), and the correlation between z_1 and z_2 can be considered equal to one. Therefore, the covariance of p_1 and p_2 is given by (21). Finally, using the (p_1, p_2) correlation definition and due to (20) and (21), the (p_1, p_2) correlation is given by (22)

$$\mathrm{cov}(p_1, p_2) = G^2 \tag{21}$$

$$\rho(p_1, p_2) = \frac{2G^2WL}{A^2 + 2G^2WL}. \tag{22}$$

In practice, G^2 can be determined using (21), and it can experimentally be verified that it is independent of the device area. The experimental and modeled correlation between both threshold voltages of matched pair devices at minimum spacing is shown in Fig. 16 for several technologies. Note that the area range where the transition from null to full correlation happens is quite device dependent.

We have studied the matching of paired transistors separated by the minimum-size feature. However, in real circuits, this might not be the case; therefore, it is necessary to know the effect of correlation at longer ranges. Based on previous works by Pelgrom [7] and Oehm [64], Cathignol [63] has demonstrated that the correlation coefficient for parameters p_1 and p_2, presented in (22) and including the spacing dependency, can be approximated as follows for not very small spacing d:

$$\rho(p_1, p_2) = \frac{G^2WL}{A^2/2 + G^2WL} - \frac{S^2d^2WL}{A^2 + 2G^2WL} \tag{23}$$

where A is the matching parameter as in (1), d is the spacing between p_1 and p_2, and S is the gradient of p with space. According to (23), the device correlation behaves as a quadratic function of spacing. A good agreement between the model in (23) and the experimental data is exemplified in Fig. 17. It should be emphasized that (23) clearly reveals that the highest values of correlation and, thus, the best matching are reached for minimum-spaced pairs, whereas as spacing increases, correlation and matching tend to degrade due to wafer-level fluctuations. It also shows that the degradation with spacing can be even more pronounced on large-area pairs, because their correlation starts at higher values for minimum spacing (see the area impact of correlation at minimum spacing in Fig. 16).

A full characterization of mismatch versus spacing, e.g., using the spectral model described in [64] or based on the model in (23) (with the parameters A_{Vt}, G_{Vt}, and S_{Vt}), would require too many test structures, including several geometries and spacings. However, standard minimum-spaced test structures can provide some very useful guidelines about the geometries that may be affected by spacing. For such geometries, the maximum degradation may affect their matching performance. If correlation at minimum spacing is not zero, we use the simple idea, which consists of noting that the worst case mismatch is obtained when the correlation drops to a zero value and the mismatch becomes [63]

$$\sigma^2_{\Delta P}(d)_{\mathrm{MAX}} = 2\sigma^2_P. \tag{24}$$

Therefore, the spacing impact can be quantified by the so-called mismatch maximum increase coefficient (MMIC), defined as [63]

$$MMIC = \frac{1}{\sqrt{1 - \rho_0(P_1, P_2))}} \tag{25}$$

where ρ_0 is the correlation at minimum spacing. Then, the MMIC coefficient can be measured as a function of the device area (see Fig. 18), providing a way of estimating the worst case mismatch, because $\sigma_{\Delta P}(d)_{\mathrm{MAX}} = MMIC \times \sigma_{\Delta P}(d \to 0)$.

F. Evolution of the Matching Parameter With Miniaturization

The matching has been characterized for several years in successive CMOS technologies, starting from the 0.5-μm

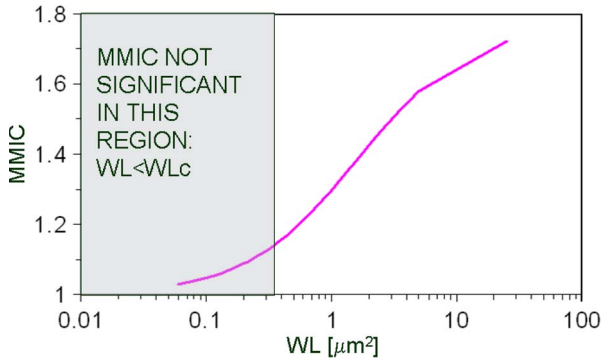

Fig. 18. MMIC versus device area for the threshold voltage of thin oxide p-channel transistor pairs from the 45-nm CMOS technology.

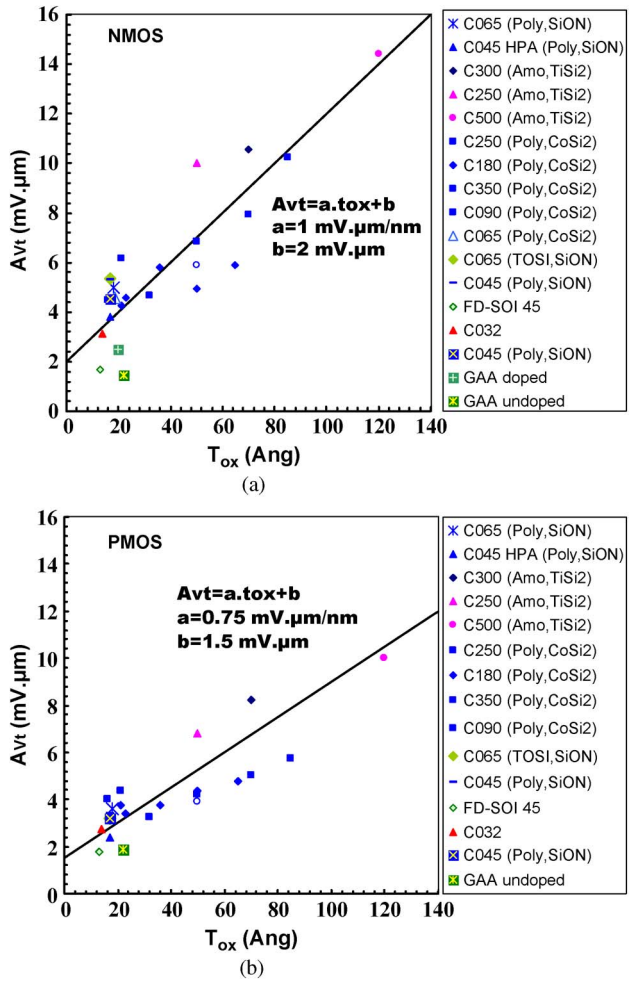

Fig. 19. Evolution of matching parameter A_{Vt} with gate oxide thickness for (a) NMOS and (b) PMOS as obtained from various CMOS technologies from 0.5 μm to 32 nm.

generation to the recent 32-nm prototype. Fig. 19 shows the recapitulation of all these results for the matching parameter A_{Vt} as a function of gate oxide thickness t_{ox} (EOT). Most data come from bulk devices, but some points are from gate-all-around (GAA) and fully depleted silicon-on-insulator (FD-SOI) technologies. Note that the data points fall on a straight $A_{Vt} = a.t_{ox} + b$, which is in good agreement with the modeling results in Fig. 1 and, in particular, with (5) obtained

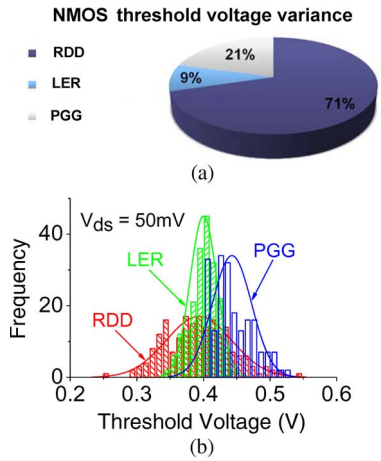

Fig. 20. (a) Breakdown of various sources to global mismatch and (b) associated histogram of mismatch sources for 45-nm LP MOS devices (cf., [48]).

from atomistic simulations [18]. The slope a is typically about 1 and 0.75 mV.μm/nm, whereas the intercept b is around 2 and 1.5 mV.μm, respectively, for NMOS and PMOS. It should also be noted that the matching parameter for undoped and metal-gate GAA and FD-SOI devices are significantly reduced compared to bulk devices [65]. In addition, note the improvement in matching for the 32-nm generation due to the suppression of polygate. This feature clearly demonstrates that the channel/gate dopant fluctuations bring an important contribution to matching, which allows us to foresee strong benefits from the undoped channel and metal-gate thin-film technologies, e.g., FD-SOI, double-gate MOS (DG-MOS), GAA, and FinFETs.

G. Diagnostic of Mismatch Sources in 45-nm Devices

A quantitative evaluation of the contributions of different sources of statistical variability, including the contribution from the polysilicon gate, has been realized on a low-power bulk NMOS from a 45-nm technology generation. This condition has been achieved based on a joint study that includes both experimental measurements and "atomistic" simulations on the same fully calibrated device [48]. The position of the Fermi-level pinning in the polysilicon bandgap that takes place along GBs [see (8)] was evaluated (here, around 200 mV), and the polysilicon gate granularity (PGG) contribution was compared to the contributions of other variability sources. The simulation results (see Fig. 20) clearly indicate that RDDs are still the dominant intrinsic source of statistical variability (around 71%), whereas the role of PGG, which is highly dependent on the Fermi-level pinning position and, consequently, on the structure of the polysilicon gate material and its deposition and annealing conditions, represents about 21%. Finally, LER contributes for less than 10% [48]. Although LER becomes critical for 32 and 22 nm, the RDDs are still the most important source of fluctuations [41], [66], [67].

As shown in Fig. 18, the mismatch in the 45-nm n-channel transistors is larger compared to their p-channel counterparts, which is in agreement with most of experimental results. Asenov *et al.* [68] have provided the following explanation for this "anomalous" behavior. In the n-channel MOSFETs, RDD, LER, and PGG have to be taken into account to obtain

good agreement between measured and simulated data. However, Asenov *et al.* showed that, in the p-channel MOSFETs, the RDD and LER contributions alone lead to a good match between the simulations and the experiment. They concluded that this asymmetry is due to the presence of acceptor-type GB states in the upper part of the bandgap, and the absence of symmetrical donor-type GB states in the low part of the bandgap is confirmed using the first-principles simulations [68].

V. Conclusion

A review of the results that we have obtained during the last ten years in the characterization and modeling of transistor mismatch in advanced CMOS technologies has been carried out. First, the theoretical background and modeling approaches that are generally employed for analyzing and interpreting the mismatch results have been presented. Then, the experimental methodologies used for characterizing the transistor matching have been discussed, with emphasis on a new A_{Vt} extraction procedure and test structure issues. Typical matching results that were obtained on several CMOS technologies from 500 nm to 32 nm have been analyzed. Specific features related to polysilicon gate structure, pocket implant, drain current variability versus gate and drain voltages, paired device interdistance, and correlation effects have been discussed. The beneficial matching improvement procured by undoped thin-film and metal-gate technologies has been underlined. Finally, the diagnosis of variability sources in bulk 45-nm CMOS devices due to atomistic simulations has been reminded, indicating that mismatch stems mostly from channel doping fluctuations.

Acknowledgment

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