DEVELOPMENT OF PIPELINE ADC FOR THE LUMINOSITY DETECTOR AT ILC

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KEYWORDS: ADC, Pipeline, Fully differential amplifier, Dynamic latch comparator

ABSTRACT: The design and measurement results of the prototype 1.5-bit stages developed for a 10 bit pipeline ADC for the luminosity detector (LumiCal) at International Linear Collider (ILC) are discussed. The motivation for the chosen architecture is presented and followed by the description of core analog blocks in a 1.5-bit stage pipeline ADC. The prototype stages were designed and fabricated in 0.35 μm CMOS technology. Wide spectrum of measurements of static (INL, DNL) and dynamic (SFDR, SNHR, SINAD, THD) parameters performed to understand and quantify the circuit performance is presented. Single 1.5-bit stage operation is studied in detail.

INTRODUCTION

The luminosity detector (LumiCal) [1] at the future International Linear Collider (ILC) will need a dedicated multichannel readout. The energy deposited in a sensor, detected and amplified in the front-end electronics, will need to be digitised and registered for further analysis. Simulations of LumiCal indicate that the reconstruction procedure needs about 10 bit precision on the measurement of deposited energy [2]. Considering the number of detector channels needed ($\sim$200,000) and the limitations on area and power, the optimum choice for the analog to digital conversion seems a dedicated multichannel ADC. Two analog to digital conversion schemes are presently under study: one relatively slow ADC per each front-end channel and one faster ADC per group of (about) 8 channels. First option would be the simplest solution from the designer point of view while the second one would allow to save area. The first option (ADC per channel) would require an ADC with sampling rate of about 3 Msample/s while the second would require a sampling rate of about 24 Msample/s. One of the most efficient architectures assuring a good compromise between the speed, area and power consumption is a pipeline ADC [4, 5, 6]. This architecture was chosen for the LumiCal data conversion. Since in the ILC experiment after each 1 ms of active beam time there will be 200 ms pause [3] the requirements on readout electronics power dissipation may be strongly relaxed if a power switching off is applied in the pause.
The paper is organised into three parts. In the first part the pipeline ADC architecture is briefly described. In the second part the design of main analog circuits of 1.5-bit stage pipeline ADC is presented. In the third part the measurements performed on the prototype ASICs are discussed together with the results. Then the conclusions follow.

ADC ARCHITECTURE

Pipeline ADC is built of several serially connected stages as shown in fig. 1. In the proposed solution a 1.5-bit stage architecture was chosen because of its simplicity and immunity to the offsets in the comparator and amplifier circuits. Since single stage generates only three different values coded on 2 bits it is called 1.5-bit stage. Each stage from fig. 1 generates 2 bits which are sent to digital correction block. In the correction block 18 output bits from 9 stages are combined together resulting in 10 bits of ADC output.

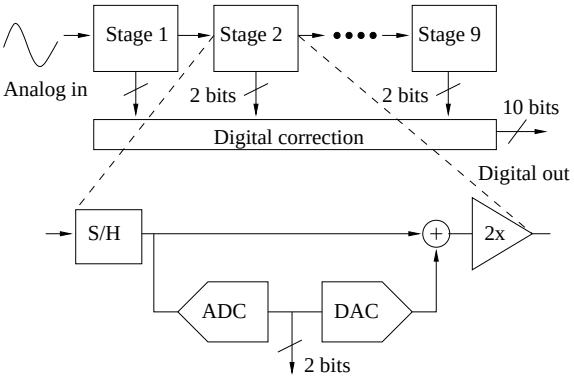

Fig. 1. Pipeline ADC architecture

The block diagram of a single stage is shown in fig. 2. Each 1.5-bit stage consist of two comparators, two pairs of capacitors C_s and C_f, an operational transconductance amplifier, several switches and small digital logic circuit. To improve the ADC immunity to digital crosstalks and other disturbances a fully differential architecture is used. The operation of the stage is performed in two phases. In phase φ_1 (see fig. 2) capacitors C_s and C_f connected to ground through S_1(in reality to common voltage, ground is used in description only for simplicity) are charged to voltages $V_{i\pm}$. In phase φ_2 the switches S_2 and S_3 change positions and S_1 is open. The C_f are now in the amplifier feedback while the C_s are connected to DAC reference voltages ($\pm V_{ref}$ or 0 depending on comparators decision). Such a connection results, if $C_f = C_s$ which is a common choice, in a gain of two in the 1.5-bit stage transfer function.

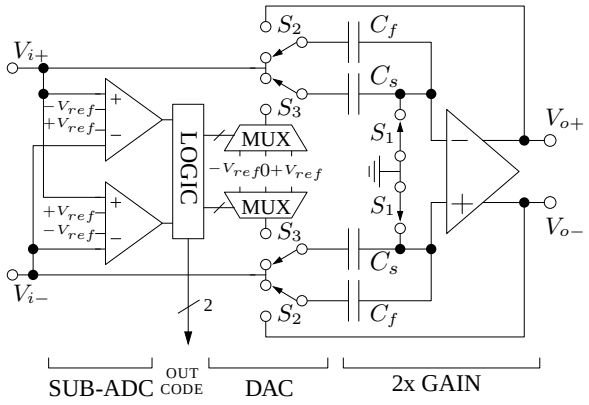

Fig. 2. Simplified schematic of a 1.5-bit stage. Switches set to φ_1 phase

ADC DESIGN

In the present design only the main core i.e. the eight 1.5-bit stages were implemented. In last 9th stage the amplifier multiplying by 2 (MDAC) and other components are not necessary but only sub-ADC consisting of comparators is needed. To simplify the layout design this sub-ADC was not yet implemented at present development stage. An important component of typical ADC, i.e. the input sample and hold (S/H) circuit, was also not implemented because it is planned to be the last stage of a front-end channel. For this prototype all reference voltages are assumed to be applied externally. The eight designed pipeline stages are almost identical with the only difference in the values of sampling C_s and feedback C_f capacitances and the current drawn by the amplifiers in the following stages. For this reason, regarding analog part, only the description of single stage components, i.e. of the amplifier and the comparator is presented in this work.

The digital logic block contains several gates to generate an output code and to control transistor switches in MUX block. These two blocks are not discussed here because of their simplicity.

Fully differential amplifier

A critical block of pipeline ADC is the fully differential amplifier. A telescopic cascode amplifier configuration is used here since compared to commonly used configurations i.e. folded cascode or two stage amplifier it represents the most efficient solution with respect to speed vs power. On the other hand, the considered technology with 3.3 V supply voltage leaves enough space for the signal dynamic range which would be the weak point of telescopic configuration at lower supply voltage. In order to obtain high enough gain in a single stage amplifier a gain-boosting scheme was implemented in both upper and lower cascode branches [7, 8].

The block diagram of the implemented fully differential amplifier is shown in fig. 3. In fact the simulated architecture achieves above 100 dB open loop gain, which leaves a large margin for the requested 10 bit resolution ADC. Both boosting amplifiers are fully differential single stage amplifiers. The lower branch

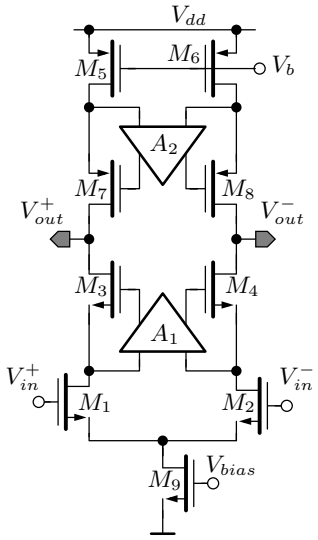

Fig. 3. Block diagram of fully differential amplifier with boosted gain

amplifier (A1) uses the telescopic cascode configuration similar to the main amplifier while the upper branch amplifier (A2) uses the folded cascode configuration with the NMOS input transistors. The main amplifier as well as both gain-boosting amplifiers use continuous common mode feedback (CMFB) scheme with MOS transistors working in the triode region connected between the ground and the source of transistor M9. The amplifier power consumption is scaled in the subsequent pairs of ADC stages decreasing the bias current by a factor of about 0.7.

Dynamic latch comparator

Since the 1.5-bit stage architecture leaves very relaxed requirements on the comparators ($\sim$100 mV threshold precision) a simple dynamic latch architecture can be used. For this work the circuit shown in fig. 4 was chosen [9].

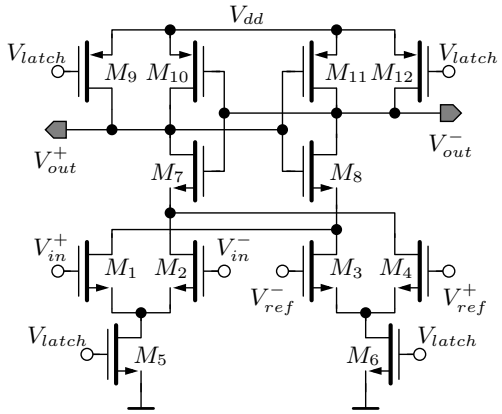

Fig. 4. Latched comparator scheme

The choice was motivated by a particularly good insensitivity to transistor mismatch and input signal common mode value. A small inconvenience is the fact that the threshold in this implementation is not given by a simple ratio of transistor dimensions but is given by

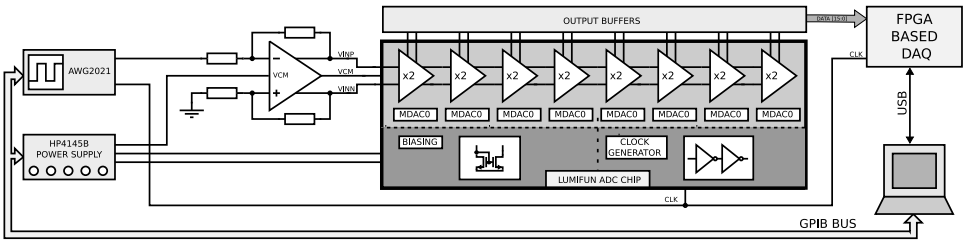

Fig. 5. Block diagram of complete test system

a second order equation. As shown by the authors [9], assuming $W_1 = W_2, W_3 = W_4$, bias currents $I_{D5} = xI_{D6}$ and requesting the threshold point $V_{in} = yV_{ref}$, the threshold condition is governed by the equation:

$$2xy^2 I_{D6}\frac{W_1}{L} - \mu C_{ox} y^4 V_{ref}^2 \left(\frac{W_1}{L}\right)^2 = 2I_{D6}\frac{W_3}{L} - \mu C_{ox} V_{ref}^2 \left(\frac{W_3}{L}\right)^2. \quad (1)$$

Using above equation one can get the transistors dimensions for the assumed x, y values.

PRELIMINARY MEASUREMENTS

Prototypes were fabricated in a 0.35μm, four-metal two-poly CMOS technology. The dimensions of the ASIC are 1.1×1.2 mm. The photograph of prototype glued and bonded on the PCB is shown fig. 6. Eight identical MDAC blocks are placed around the chip. Biasing and clocks generation blocks are located in the centre of the chip. The power consumption

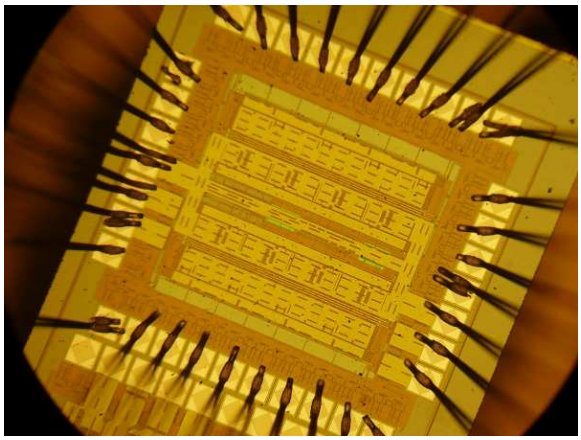

Fig. 6. Photograph of glued and bonded prototype

of the whole analog part was measured to 48 mW independently of sampling frequency. In first tests, the basic functionality was studied with DC input signal. Then the essential static (INL, DNL, missing codes) and dynamic (SFDR, SNHR, SINAD, THD) parameters were measured. Dedicated measurements were performed to get better insight into the operation of the key blocks of a single pipeline stage i.e. the MDAC and the sub-ADC.

Test Setup

Block diagram of the complete test system is shown in fig. 5. In order to perform the tests with single-ended input signals a dedicated circuit based on fast differential amplifier converting single ended signals to differential was added. As a source of input signal a 12 bit arbitrary waveform generator (Tektronix AWG 2021) was used. For measurements with static signals the AWG was used as a precise voltage source while for dynamic measurements it generated step signals as shown in fig. 7. The step signals were used because the S/H circuit was not implemented at the ADC input. The clock signal was also generated by the AWG. All reference voltages were applied with HP4145B precise power supply which was controlled through GPIB interface. Such configuration allowed us to determine the effect of biasing conditions on overall circuit performance.

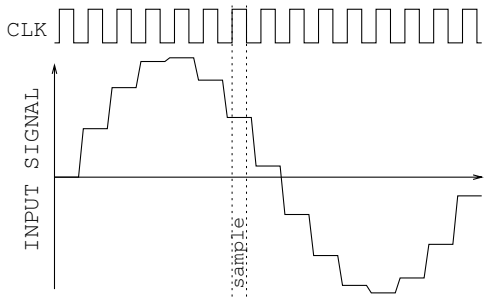

Fig. 7. Input signals generation and clocking

Because digital correction algorithm was not yet implemented in the ASIC all 16 bits had to be read out (instead of 9 in case if correction was implemented). Practically the readout was done by FPGA based data acquisition system connected to a PC via USB link. Digital correction was performed by software during data analysis.

INL and DNL measurements

The Integral Nonlinearity (INL) and the Differential Nonlinearity (DNL) results showed in fig. 8 were measured statically with the ADC sampling frequency of 10 MHz. These parameters were obtained with histogramming method. The integral nonlinearity was measured to be within ± 3 LSB. The Effective Number of Bits (ENOB) of 6.65 was calculated from the measured

INL curve.
Differential nonlinearity stays mostly within ± 0.5 LSB, but there are some codes with larger DNL. Six of the codes with DNL less than -0.9 were identified as missing codes [10]. These 6 missing codes (about 1% of the total) and quite high INL are the main issues to resolve in the present ADC version.

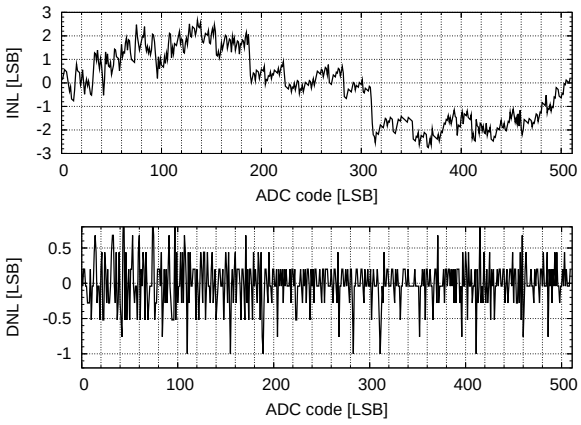

Fig. 8. INL and DNL measured statically

Dynamic FFT measurements

To estimate dynamic circuit performance measurements with pure sinusoidal wave input were performed [10]. Fast Fourier Transformation (FFT) was used to calculate output signal spectrum. Having in mind that ADC output signal is superposition of input signal, distortions and noise one can use few metrics to determine ADC performance. To estimate pure noise level in a circuit one has to compare the ratio of FFT signal amplitude at the input signal frequency f_0 to the integrated FFT spectrum excluding harmonic frequencies ($2f_0$, $3f_0$, $4f_0$, ...). Such metrics is called Signal to Non Harmonic Ratio (SNHR). The ratio of a signal amplitude to all harmonics is called the Total Harmonic Distortion (THD). The ratio of the FFT signal amplitude at the input frequency to the amplitude of the largest harmonic or spurious spectral component observed over the whole Nyquist band is called the Spurious Free Dynamic Range (SFDR). To determine the overall ADC performance the Signal to Noise and Distortion Ratio (SINAD) is used. Its value is calculated as a ratio of the signal at the input signal frequency to the integral over all frequencies (excluding input signal frequency).
Measured spectrum for 3.4 MHz full scale (0 dB) input signal sampled at 35 MHz is shown in fig. 9. The SINAD of 40.4 dB was obtained. It is dominated by the harmonic distortions (THD) which is equal to 40.9 dB. It is too low for 8 bit ADC (in the ideal 8 bit case it should be 49.9 dB). Detailed studies showed that such behaviour is due to MDAC gain mismatch (MDAC gain is lower than 2). It was verified with simulations that the gain mismatch is not caused by too low gain of the differential amplifier but is connected to not precise enough timing of MDAC switches. It will be improved in the next version. The SNHR of 49.1 dB was obtained and it's quite promising

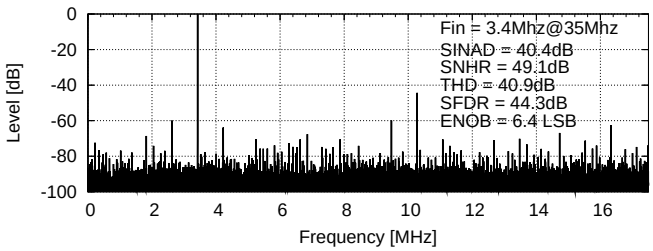

Fig. 9. Example FFT; 3.4 MHz @ 35 Mhz

because it shows that the pure noise level is equivalent to the ideal 8 bit ADC. The effective number of bits (ENOB) calculated from dynamic measurements equals 6.4 which is in good agreement with the results obtained from static measurements.
The dependence of all discussed above metrics on ADC sampling frequency was also investigated. The results of this measurements are shown in fig. 10. One may

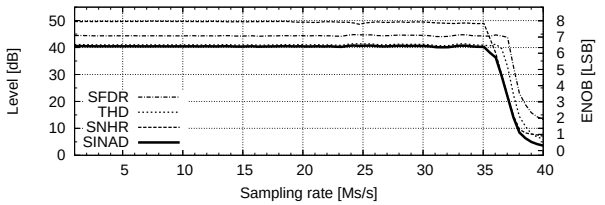

Fig. 10. ADC performance as a function of sampling rate

conclude that the ADC works well in a wide frequency range up to 36 Mhz. Above this frequency all the metrics fall due to bandwidth limit of MDAC amplifier. Also the effect of the input signal frequency was investigated and the measurements showed that it does not affect the ADC performance over the whole Nyquist band.

Stage transfer function transition points

Since it is possible to read the output of each stage comparators before correction the transition points of transfer function can be measured. Using these points it is possible to calculate the gain A and the thresholds (or rather threshold difference $\Delta th = th_{\text{high}} - th_{\text{low}}$) of consecutive stages and compare it to simulations.
For a single stage the transfer function is given by the formula:

$$V_o = AV_{in} - V_R, \quad V_R = \begin{cases} -V_{ref} & V_{in} < th_{\text{low}} \\ 0 & th_{\text{low}} < V_{in} < th_{\text{high}} \\ V_{ref} & V_{in} > th_{\text{high}} \end{cases}. \tag{2}$$

In the ideal case the gain A is equal 2 and the thresholds should be $th_{\text{low}} = -1/4V_{ref}$ and $th_{\text{high}} = 1/4V_{ref}$.
Since there is a single-ended to differential converter circuit at the ADC input (see fig. 5) the ADC V_{in} voltage can be written as:

$$V_{in} = av + b, \tag{3}$$

where a is the gain of input amplifier, b is offset of it and v is voltage at the input of the measured setup.

There are two transition points in the transfer function at the first stage output (equation 2). At the second stage output there are 6 such points and $2^{n+1}-2$ at the output of stage n. Let's denoted v'_1 and v'_2 as transition points of the first stage transfer function, $v''_1,\ldots,v''_6$ as transition points in the second stage transfer function and generally $v_1^{(n)},\ldots,v_{2^{n+1}-2}^{(n)}$ in stage n. Transition points for the first 6 stages are shown in fig. 11.

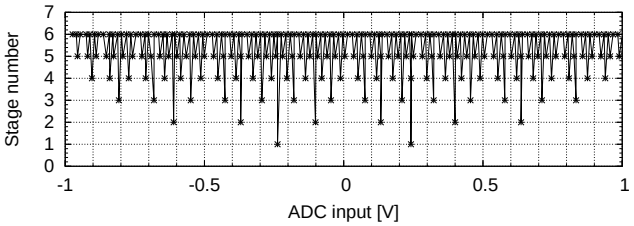

Fig. 11. Measured transition points of stage transfer functions. Lines are only to guide the eye.

Transition points v'_1 and v'_2 correspond to thresholds in first stage through the equation 3 so considering the input of the first stage one can write:

$$th'_{\text{low}} = av'_1 + b \tag{4}$$
$$th'_{\text{high}} = av'_2 + b \tag{5}$$

and the threshold difference is:

$$\Delta th' = th'_{\text{high}} - th'_{\text{low}} = a(v'_2 - v'_1). \tag{6}$$

If gain a is not known precisely the $\Delta th'$ cannot be calculated.
There are 6 transition points in the second stage which correspond to two thresholds of this stage (see fig. 11). It is also seen in fig. 11 that $v''_1, v''_2 < v'_1 < v''_3, v''_4 < v'_2 < v''_5, v''_6$. Considering the input of the second stage and using equation 2 it can be written:

$$th''_{\text{low}} = A_1(av''_1 + b) + V_{ref} \tag{7a}$$
$$th''_{\text{high}} = A_1(av''_2 + b) + V_{ref} \tag{7b}$$
$$th''_{\text{low}} = A_1(av''_3 + b) \tag{7c}$$
$$th''_{\text{high}} = A_1(av''_4 + b) \tag{7d}$$
$$th''_{\text{low}} = A_1(av''_5 + b) - V_{ref} \tag{7e}$$
$$th''_{\text{high}} = A_1(av''_6 + b) - V_{ref}. \tag{7f}$$

With the above system of equations the A_1 and $\Delta th''$ can be calculated in several ways. Here only two of them will be used as shown below:

$$aA_1 = \frac{V_{ref}}{v''_5 - v''_3} = \frac{V_{ref}}{v''_4 - v''_2} \tag{8}$$
$$\Delta th'' = \frac{v''_4 - v''_3}{v''_5 - v''_3}V_{ref} = \frac{v''_4 - v''_3}{v''_4 - v''_2}V_{ref}. \tag{9}$$

In this case the $\Delta th''$ can be easy obtained while to calculate A_1 the preamplifier gain a is necessary.
Considering the input of the third stage 14 equations can be written as:

$$th'''_{\text{low}} = A_2(A_1(av'''_1 + b) + V_{ref}) + V_{ref} \tag{10a}$$
$$th'''_{\text{high}} = A_2(A_1(av'''_2 + b) + V_{ref}) + V_{ref} \tag{10b}$$
$$th'''_{\text{low}} = A_2(A_1(av'''_3 + b) + V_{ref}) \tag{10c}$$
$$th'''_{\text{high}} = A_2(A_1(av'''_4 + b) + V_{ref}) \tag{10d}$$
$$th'''_{\text{low}} = A_2(A_1(av'''_5 + b) + V_{ref}) - V_{ref} \tag{10e}$$
$$th'''_{\text{high}} = A_2(A_1(av'''_6 + b)) + V_{ref} \tag{10f}$$
$$th'''_{\text{low}} = A_2(A_1(av'''_7 + b)) \tag{10g}$$
$$th'''_{\text{high}} = A_2(A_1(av'''_8 + b)) \tag{10h}$$
$$th'''_{\text{low}} = A_2(A_1(av'''_9 + b)) - V_{ref} \tag{10i}$$
$$th'''_{\text{high}} = A_2(A_1(av'''_{10} + b) - V_{ref}) + V_{ref} \tag{10j}$$
$$th'''_{\text{low}} = A_2(A_1(av'''_{11} + b) - V_{ref}) \tag{10k}$$
$$th'''_{\text{high}} = A_2(A_1(av'''_{12} + b) - V_{ref}) \tag{10l}$$
$$th'''_{\text{low}} = A_2(A_1(av'''_{13} + b) - V_{ref}) - V_{ref} \tag{10m}$$
$$th'''_{\text{high}} = A_2(A_1(av'''_{14} + b) - V_{ref}) - V_{ref}. \tag{10n}$$

It should be noticed that equations 7b–7e describing stage 2 input are very similar to equations 10f–10i from stage 3. Because of that only equations 10f–10i will be used to compute A_2 and $\Delta th'''$:

$$A_2 = \frac{V_{ref}}{aA_1(v'''_9 - v'''_7)} = \frac{V_{ref}}{aA_1(v'''_8 - v'''_6)} \tag{11}$$
$$\Delta th''' = \frac{v'''_8 - v'''_7}{v'''_9 - v'''_7}V_{ref} = \frac{v'''_8 - v'''_7}{v'''_8 - v'''_6}V_{ref}. \tag{12}$$

It is worth to notice that gain A_2 can be computed without exact value of a because the product aA_1 can be calculated from equation 8.
The same consideration can be repeated for 4th and consecutive stages and for each stage the formulae similar to 7b–7e and 10f–10i will appear. On this basis the general solution can be found. Generalising equations 11 and 12 one can obtain the following formulae (valid for $n > 1$):

$$A_{n-1} = \frac{V_{ref}}{(v_{2^n+1}^{(n)} - v_{2^n-1}^{(n)})a\prod_{i=1}^{n-2}A_i} = \frac{V_{ref}}{(v_{2^n}^{(n)} - v_{2^n-2}^{(n)})a\prod_{i=1}^{n-2}A_i}. \tag{13}$$

$$\Delta th^{(n)} = \frac{v_{2^n}^{(n)} - v_{2^n-1}^{(n)}}{v_{2^n+1}^{(n)} - v_{2^n-1}^{(n)}}V_{ref} = \frac{v_{2^n}^{(n)} - v_{2^n-1}^{(n)}}{v_{2^n}^{(n)} - v_{2^n-2}^{(n)}}V_{ref}. \tag{14}$$

Substituting $n+1$ with n in equation 13 and then substituting equation 13 for A_{n-1} in the denominator product the final formula for the stage gain is obtained for $n > 2$:

$$A_n = \frac{v_{2^n+1}^{(n)} - v_{2^n-1}^{(n)}}{v_{2^{n+1}+1}^{(n+1)} - v_{2^{n+1}-1}^{(n+1)}} = \frac{v_{2^n}^{(n)} - v_{2^n-2}^{(n)}}{v_{2^{n+1}}^{(n+1)} - v_{2^{n+1}-2}^{(n+1)}}. \tag{15}$$

To obtain relatively simple formulae 14 and 15 only 4 equations were used which correspond to the middle region of the input signal dynamic range. This is not the

only possibility. There are many more equations allowing the calculation of gain and threshold. Other two simple equations sets ("brunches" in fig. 11) giving simple analytical formulae could be obtained choosing for each stage either 4 equations for the smallest amplitude of input signal or the ones for the highest amplitude.
Table 1 shows results of calculations with use of formulae 15 and 14. Regarding the MDAC gain it is seen that

TABLE 1. Gain and Δth of ADC stages computed from transition points of stage transfer functions

Stage	Gain ($\pm$ std)	Δth ($\pm$ std) [V]
1	1.99$\pm$0.010	0.479$\pm$0.0011
2	1.97$\pm$0.013	0.468$\pm$0.0029
3	1.96$\pm$0.021	0.480$\pm$0.0047
4	1.96$\pm$0.034	0.48$\pm$0.011
5	1.94$\pm$0.065	0.48$\pm$0.017
6	—	0.50$\pm$0.032

the results of each stage are systematically smaller than 2 (the ideal case). This lower gain is the reason of observed nonlinearities discussed already together with FFT measurements. The second column of table 1 shows the differences between high and low threshold value which should be equal to 0.5 V in the ideal case (for $V_{ref} = 1\ V$). The measurements results are different only by about 20 mV which is a very good result a for single stage latch comparator.

SUMMARY

The critical analog blocks of a pipeline ADC including MDAC with a fully differential amplifier and sub-ADC with a dynamic latch comparator were designed and incorporated into a 1.5 bit ADC stage. The prototype ASIC comprising eight pipeline stages was completed and fabricated in 0.35 μm CMOS technology. Full functionality of this ADC core was verified and key static (INL, DNL) and dynamic (SFDR, SNHR, THD, SINAD) ADC parameters were measured. Both analog blocks i.e. fully differential amplifier and dynamic latch comparator operate properly. The operation of the comparator was verified by the measurements of transition points. The proper ADC functionality for sampling frequency up to 36 MHz was verified. The measured noise represented by the SNHR shows expected 50 dB performance for 8 stages. Work is still needed to improve the linearity (THD, INL, DNL).

ACKNOWLEDGEMENTS

This work was partially supported by the Commission of the European Communities under the 6^{th} Framework Programme "Structuring the European Research Area", contract number RII3-026126. It was also supported in part by the Polish Ministry of Science and Higher Education under SPUB nr 112/E-356/SPB/DESY/P-03/DZ376/2003-2005 and under contract nr 372/6.PRUE/2007/7. We are grateful to the members of the FCAL Collaboration for fruitful cooperation. We acknowledge useful discussions with prof. Wladyslaw Dabrowski and continuous encouragement from prof. Leszek Suszycki.

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