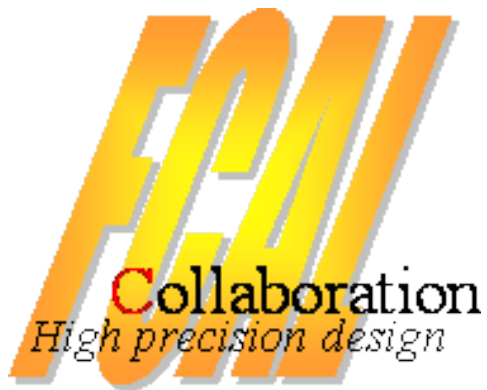


Development of readout electronics for ILC Forward Calorimetry

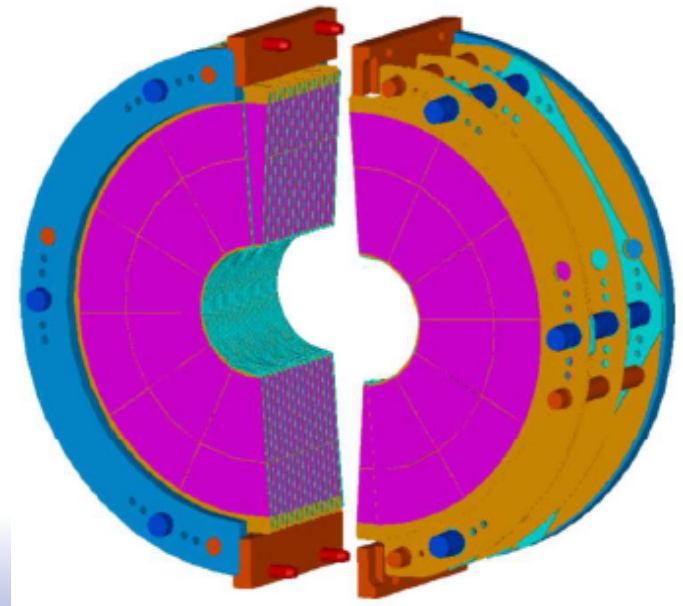


Marek Idzik, Krzysztof Świentek, Szymon Kulis,
Jan Gajewski, Dominik Przyborowski

AGH-UST Kraków

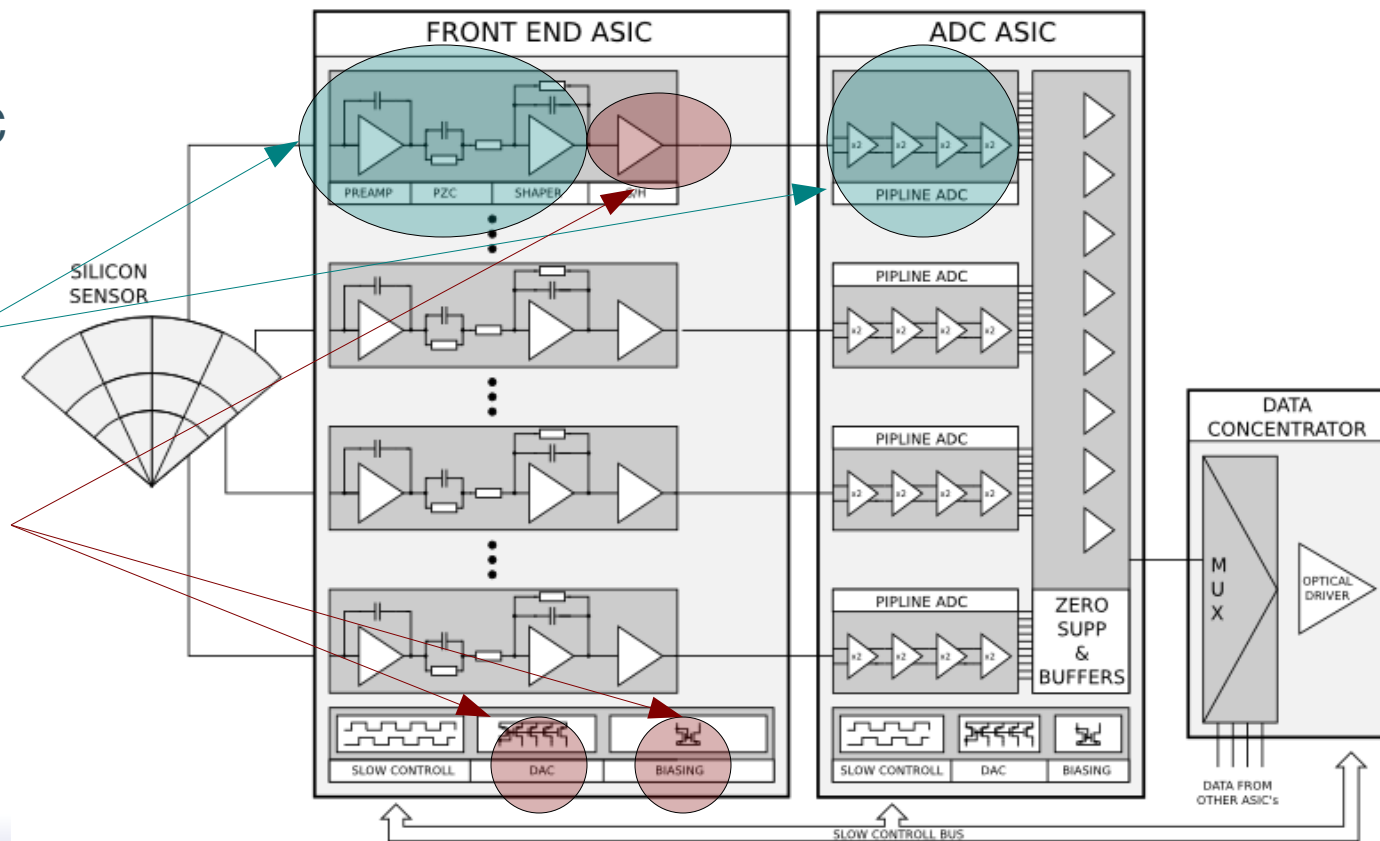
Outline

- ❑ LumiCal readout architecture & design
- ❑ Measurements of Front-end prototypes
- ❑ Measurements of ADC prototypes
- ❑ Summary & plans



LumiCal Readout architecture

- ❑ Front-end (~32 channels) and ADC (? channels) ASIC
- ❑ First prototypes in AMS 0.35 μm
- ❑ Design in progress (S/H, DAC, Bias)



Challenges of LumiCal front-end

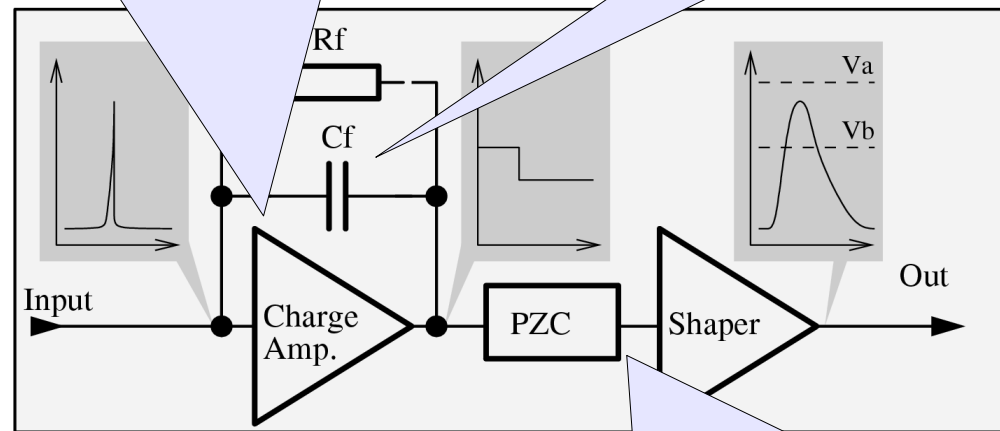
Large C_{det} range 10-100 pF

Calibration mode S/N~10 for MIP

Charge sensitive amplifier

$Q_{\text{max}} \sim 10 \text{ pC}$

$C_f \sim 10 \text{ pF}$



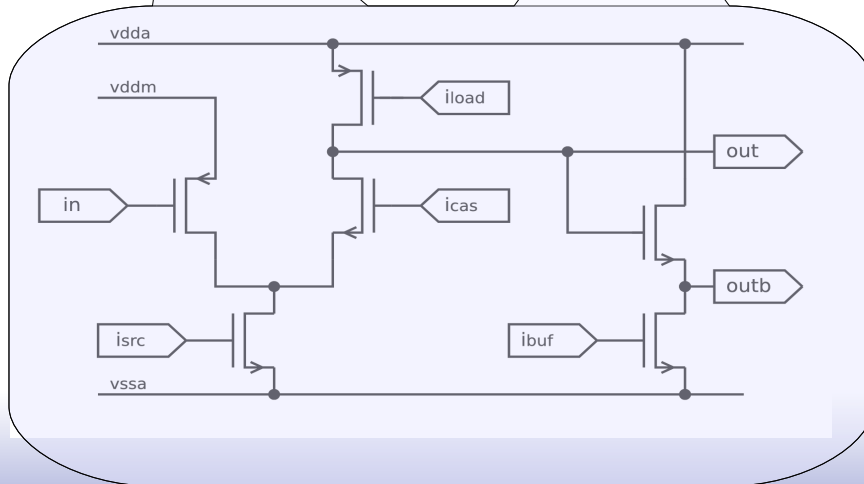
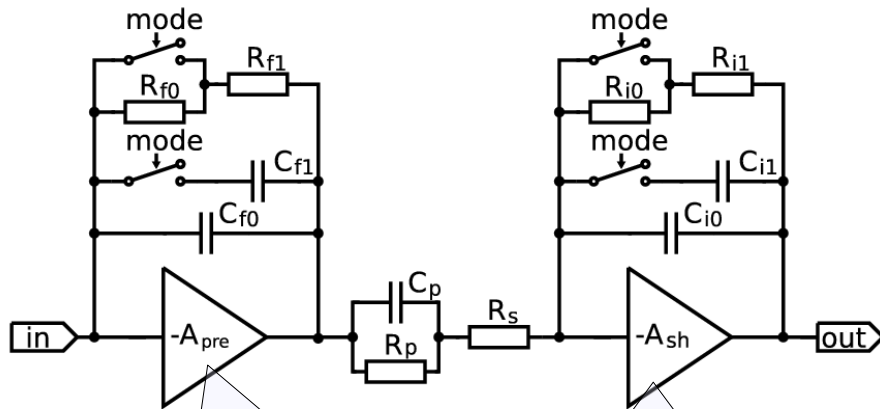
Calibration & Physics mode

Variable gain

$\Delta t \approx 300 \text{ ns}$, high occupancy

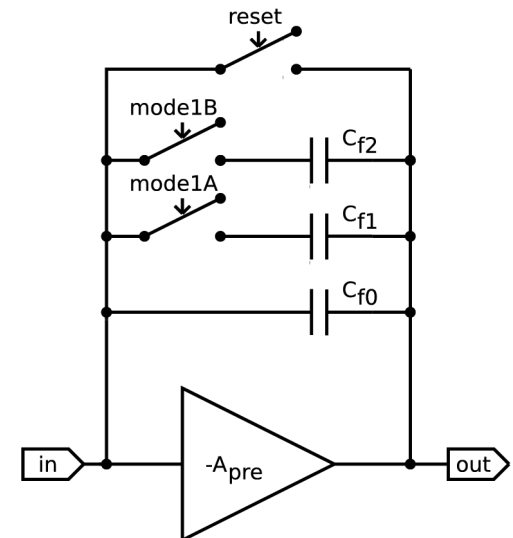
PZC + Shaper $T_{\text{peak}} \sim 60 \text{ ns}$

Front-end architecture

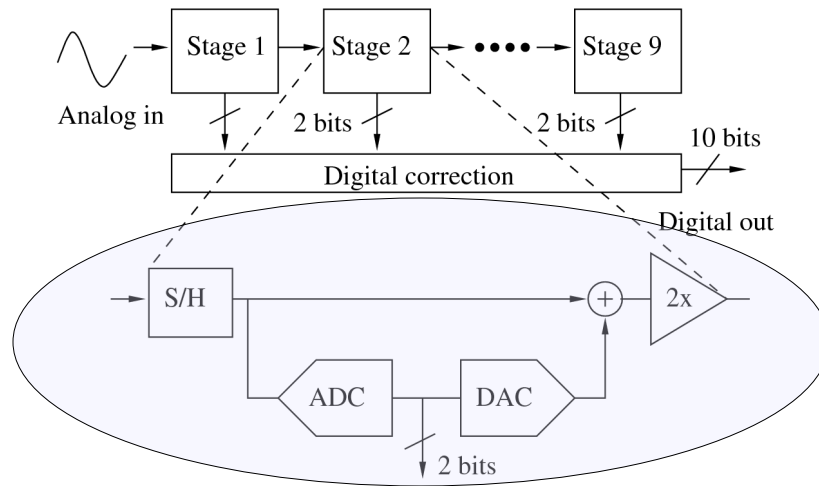


- Preamp. feedback: passive R_f or MOS
- Preamp: $I_{pre} \sim 2.5\text{mA}$, PMOS input, $C_f \sim 10\text{pF}$ (physics), $C_f \sim 0.5\text{pF}$ (calibration)
- Shaper: 1st order, $T_{peak} \sim 60\text{ns}$

Alternative configuration Gated-Reset



ADC architecture

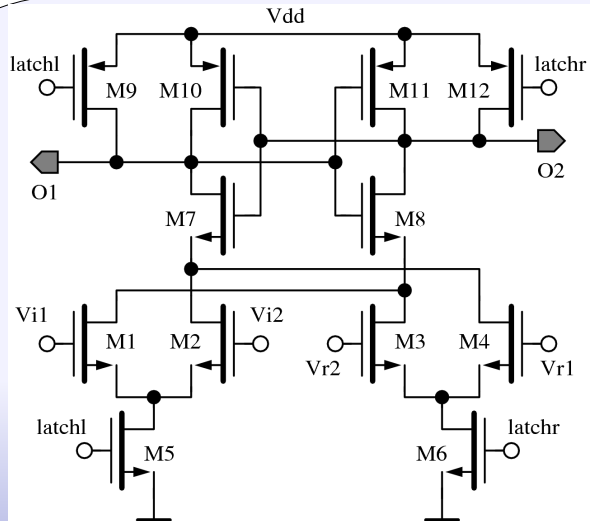
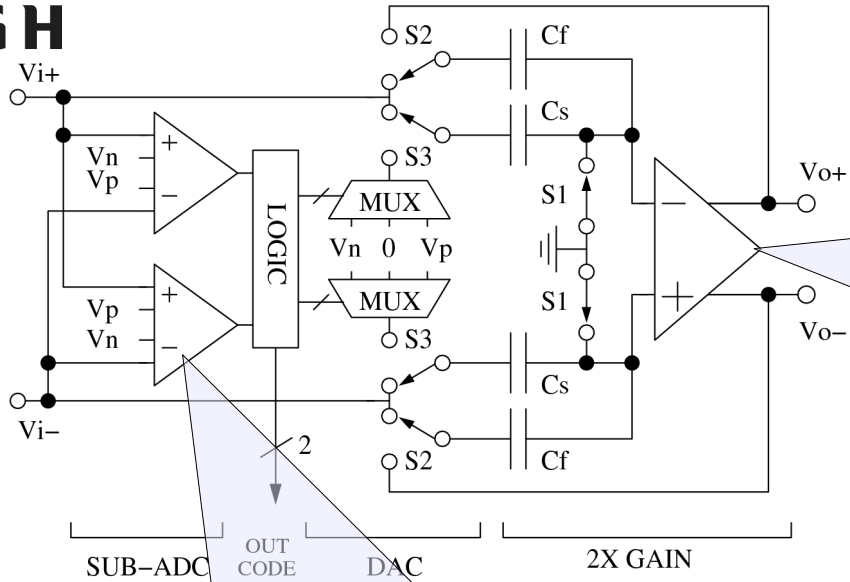


- ❑ Pipeline architecture
- ❑ 1.5 bit per stage
- ❑ Fully differential

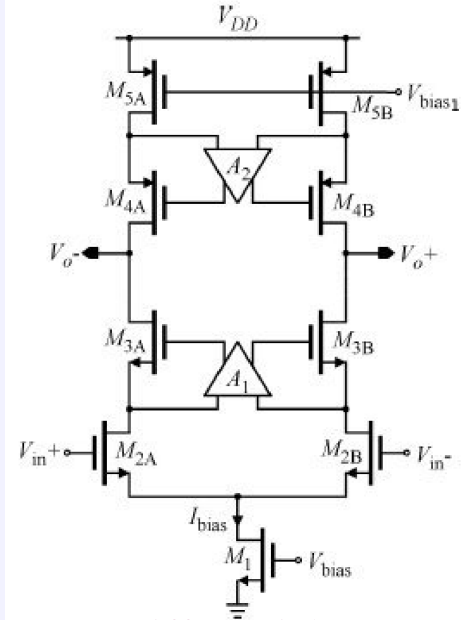
- 10 bits resolution
- Input dynamic range 2V
- Maximum sampling frequency 35 MHz
- Low power consumption



1.5 bit stage architecture



Dynamic latch comparators



Differential amplifier with boosted gain



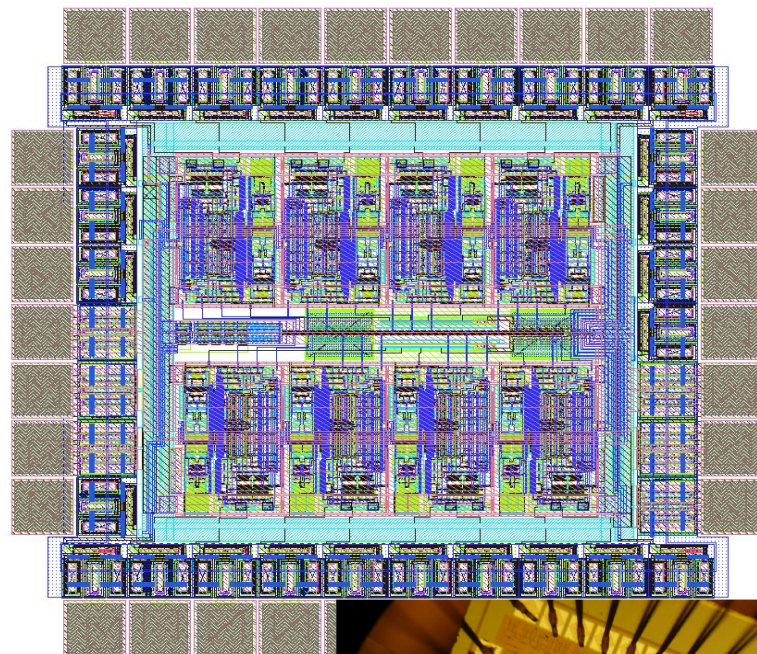
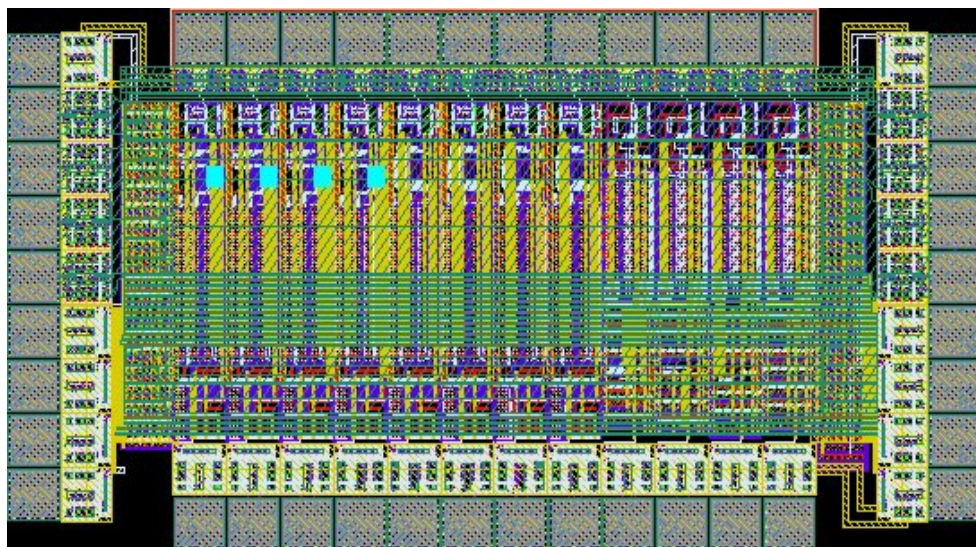
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First prototypes

12 channels front-end ASIC

8 stages of pipeline ADC

submitted in June 2007

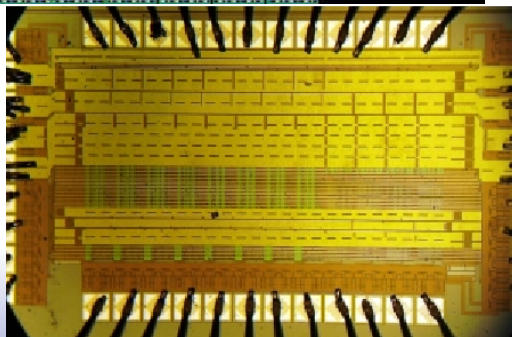


8 chan. - continuous shaping

4 passive Rf feedback

4 triode MOS feedback

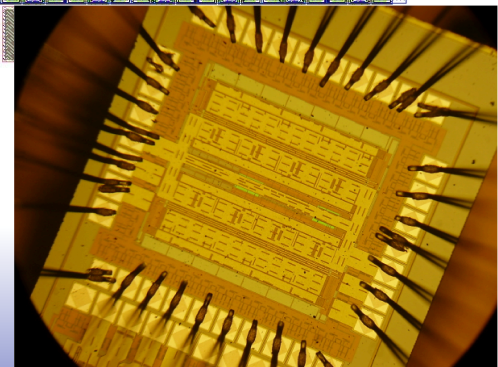
4 chan. - Gated-Reset



No reference
voltages.

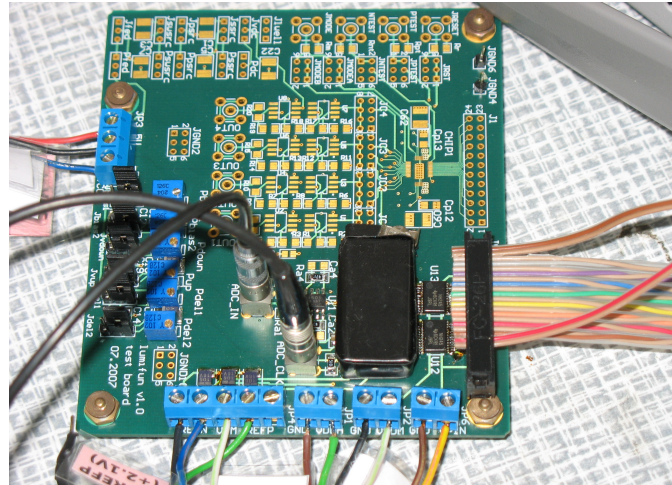
No digital
correction.

No ...

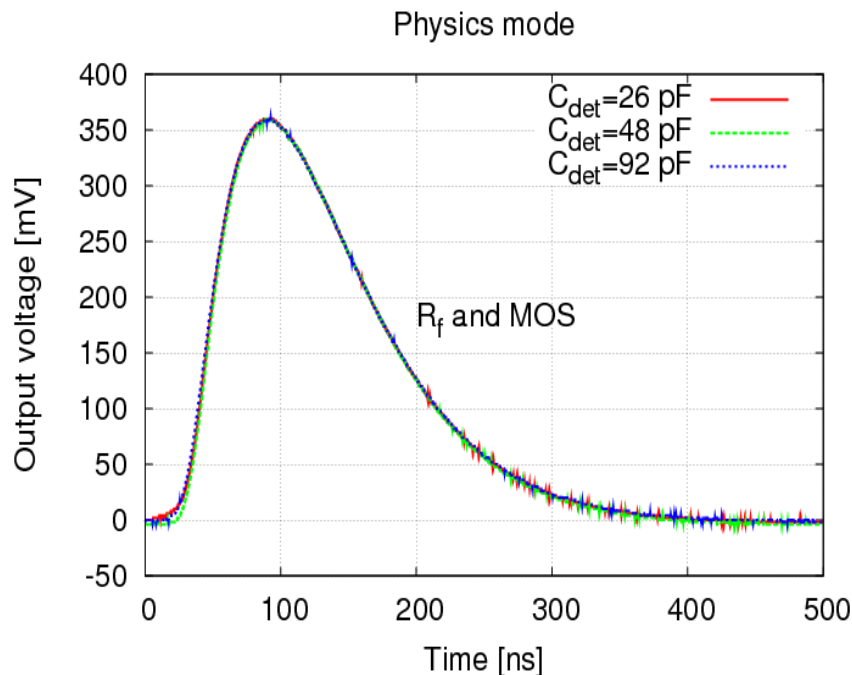


Front-end measurements

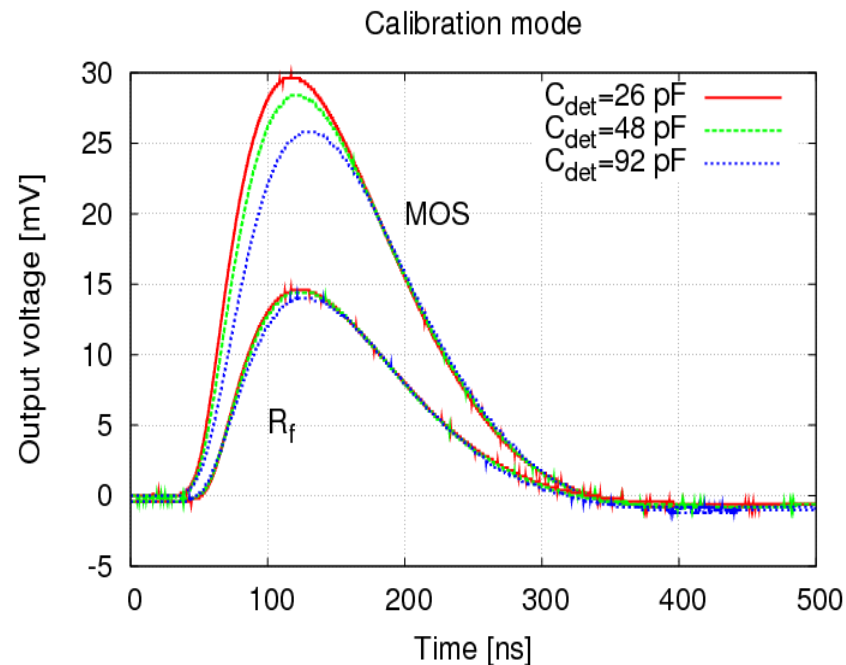
- ❑ 40 ASICs received
- ❑ PCB designed & produced
- ❑ Test Setup established
- ❑ Tests with generator and external capacitance. Tests with sensors just started at DESY
 - Pulse shape
 - Gain
 - Noise
 - Pulse rate
 - Crosstalk, Power consumption



Pulse shape



Very good charge sensitivity in physics mode (same for MOS and passive R_f feedback)

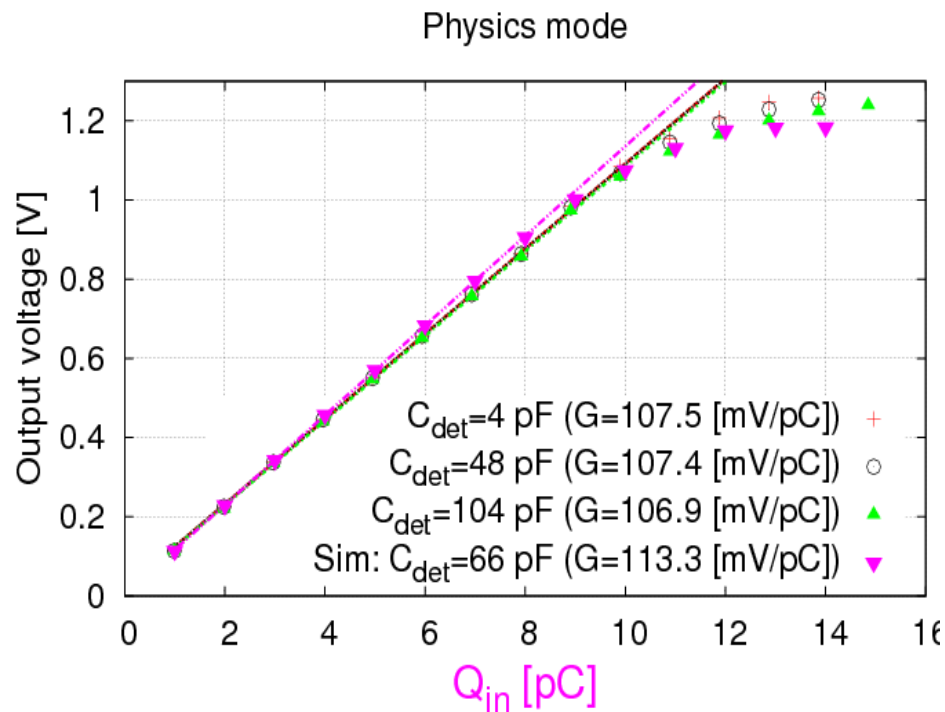


Slight sensor capacitance dependence in calibration mode (gain for MOS and R_f feedback different by design)

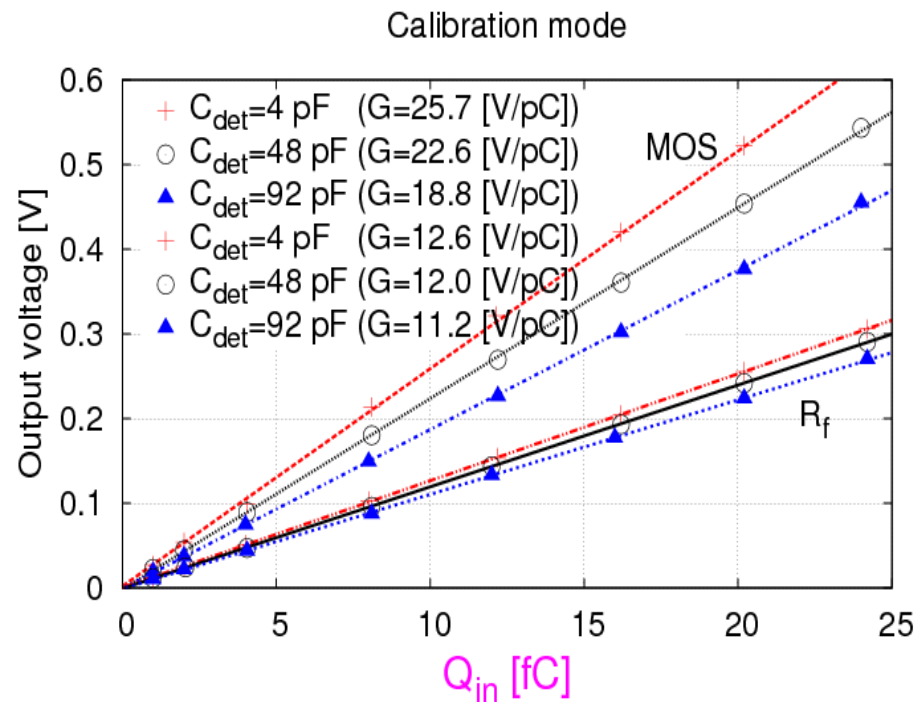


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Gain



Constant gain in physics mode

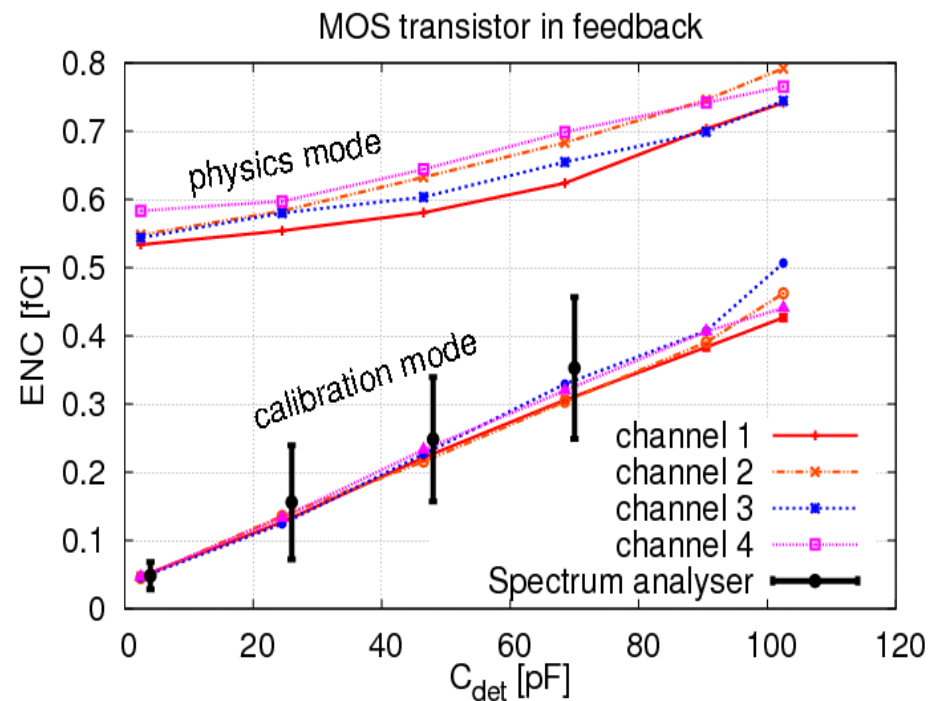
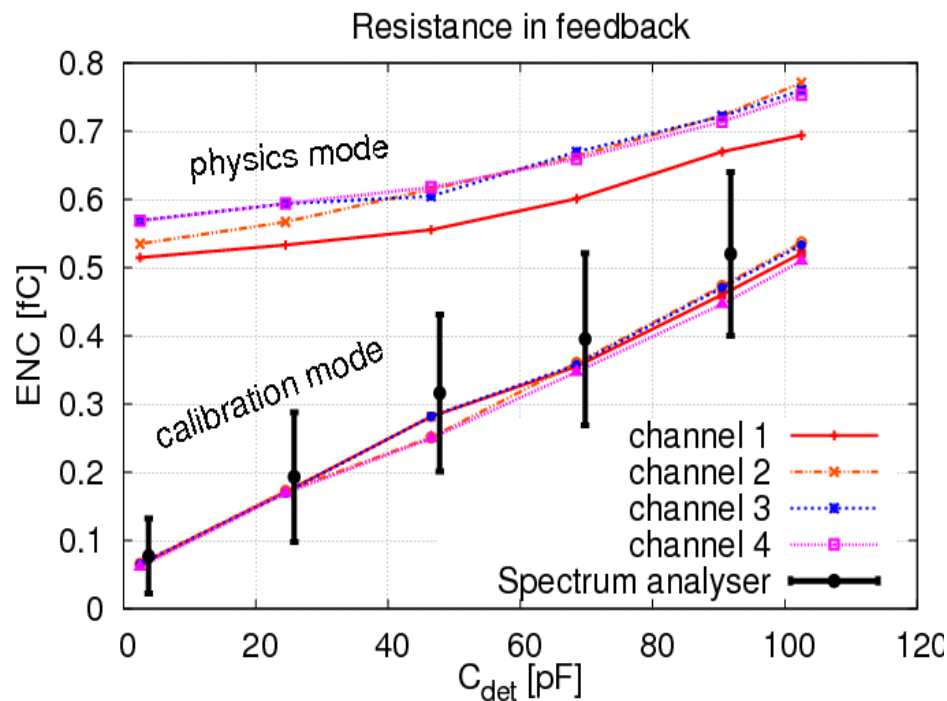


Slight gain decrease with growing sensor capacitance in calibration mode



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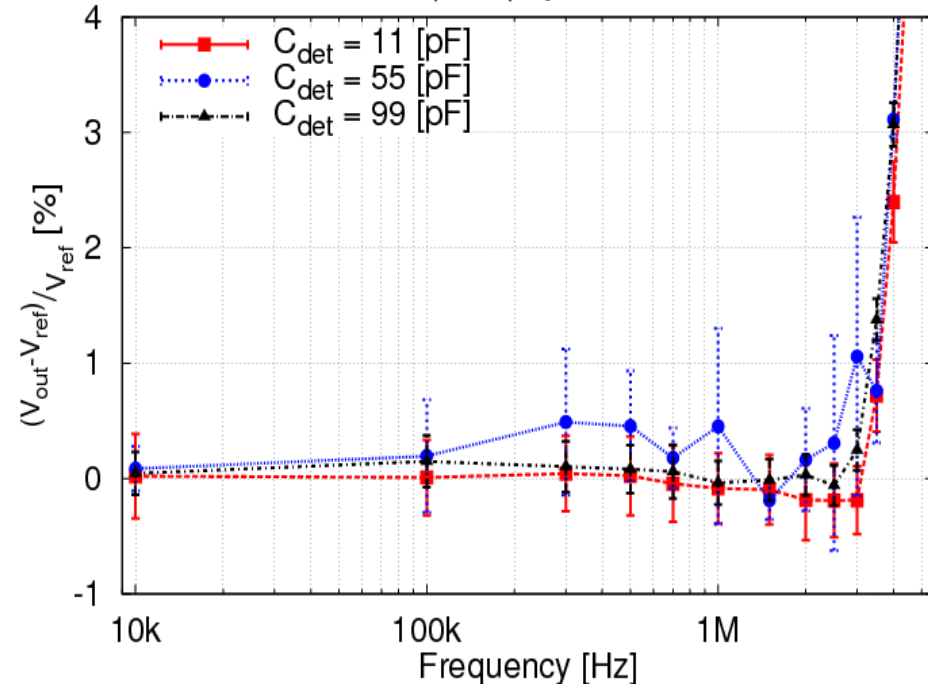
Noise



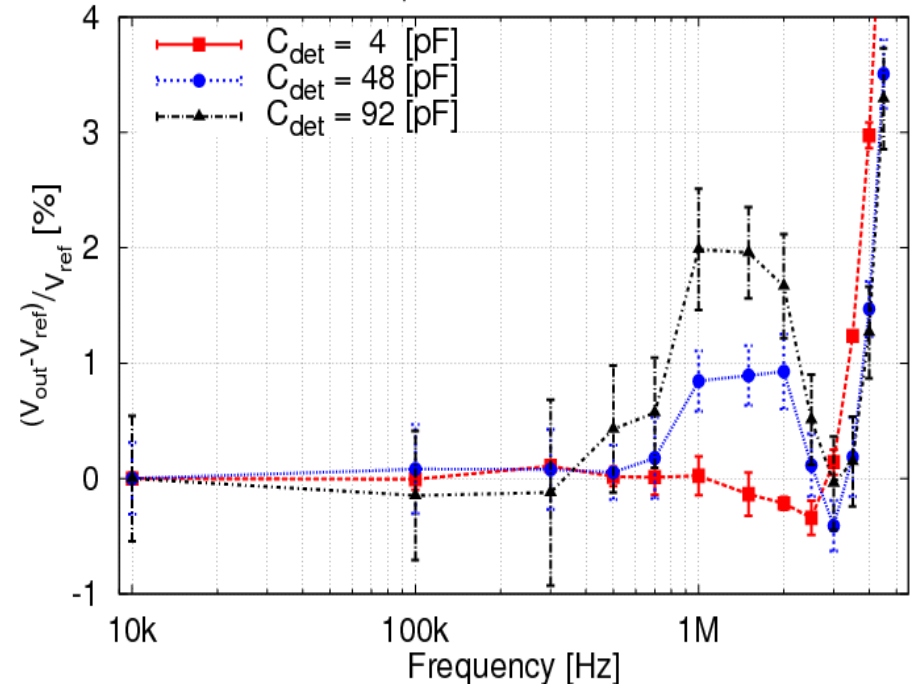
- *Measurements done with external capacitance and generator. Need to be confirmed with sensor and particles*
- *In calibration mode noise below 0.4 fC - good MIP sensitivity (SNR > 10)*
- *Noise for MOS feedback similar to R_f Feedback*
- *Results with true RMS meter consistent with spectrum analyser*

Pulse rate

Pile-up for physics mode



Pile-up for calibration mode



Front-end works well up to ~3 MHz continuous input rate. In calibration mode slight dependence on sensor capacitance – as expected from simulations

Crosstalk, Power

Crosstalk measurements done with PIN photodiode and impinging laser light

Crosstalk		
Feedback:	MOS	R_f
Calibration	0.08 %	0.25 %
Physics	0.95 %	1.5 %

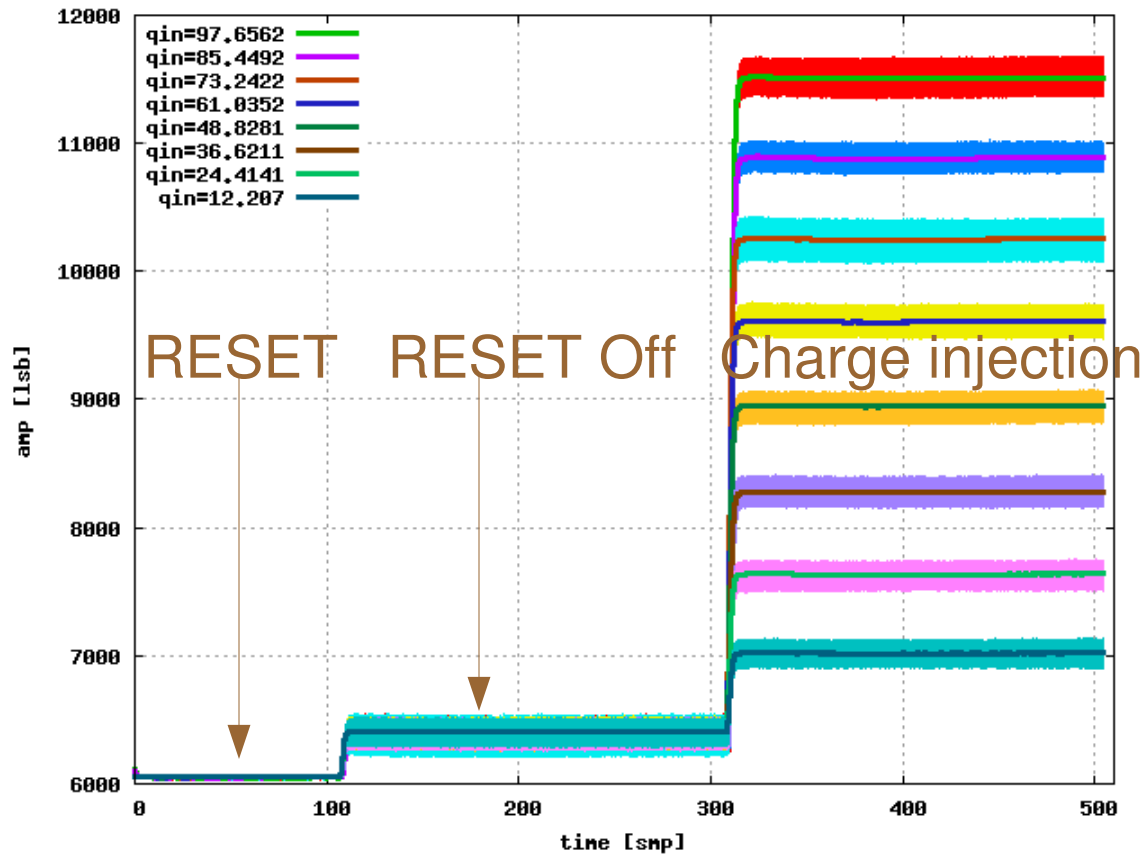
R_f area larger than MOS

Feedback capacitance area in physics mode larger than in calibration

Work on Layout needed

Power consumption about 8.9 mW/channel consistent with simulations.

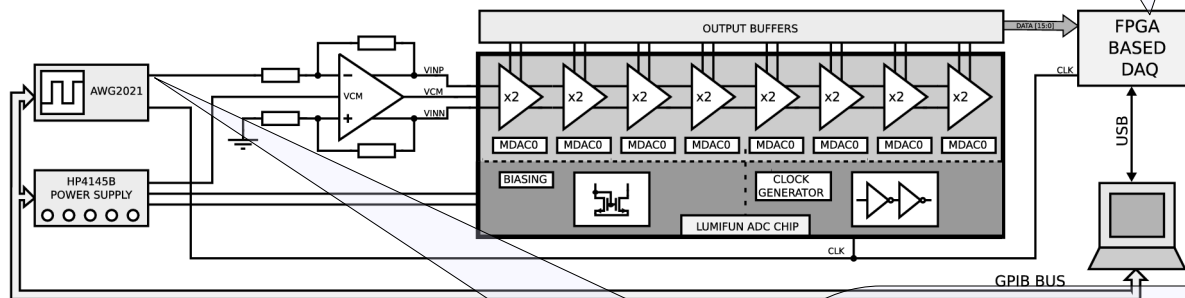
Gated-Reset prototype



- ❑ Gated-Reset charge amplifier fully functional
- ❑ Measurements in progress...

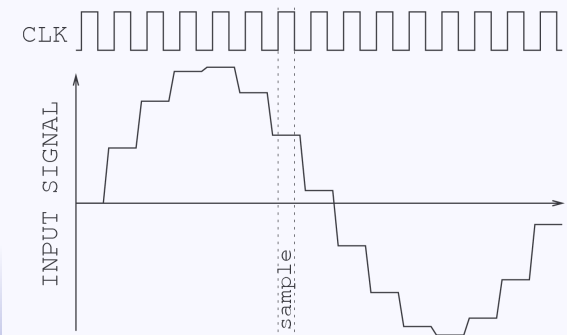
ADC measurements

- ❑ 40 ASICs received
- ❑ PCB designed & produced
- ❑ FPGA based setup allowing full ADC characterization

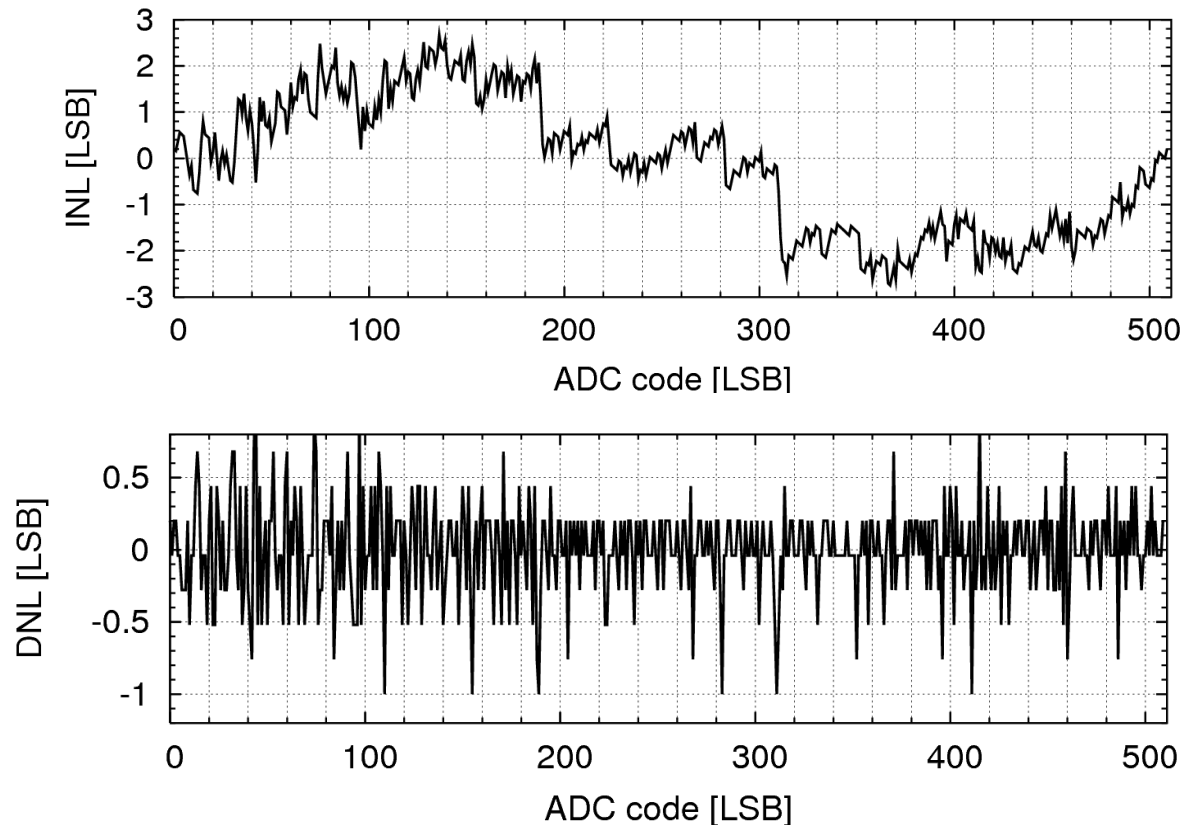


DAQ working up to
~120MHz sampling
frequency

- ❑ Static measurements
 - INL, DNL, ENOB
- ❑ Dynamic FFT measurements
 - SNHR, THD, SFDR, SINAD, ENOB



Static ADC tests



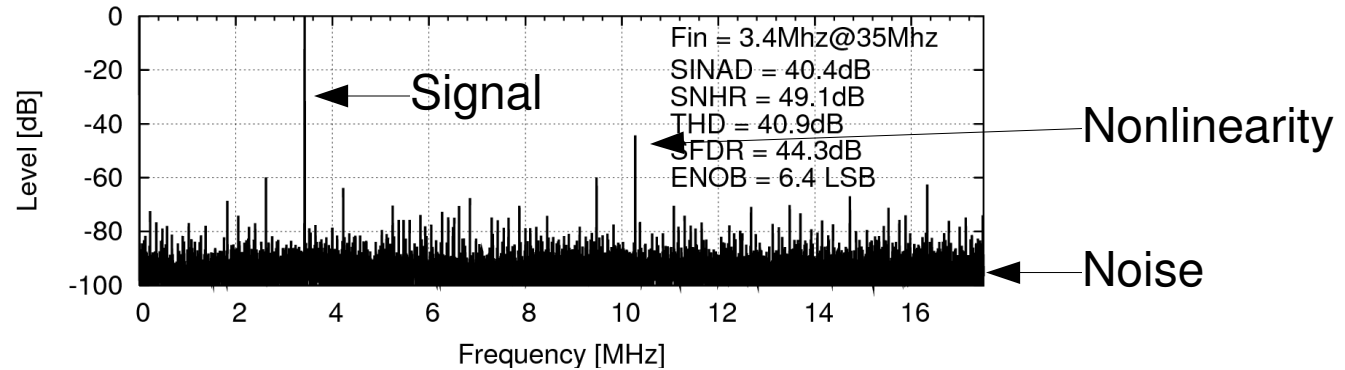
- ❑ Maximum Integral Nonlinearity found $\pm 2.5\text{LSB}$, could be improved
- ❑ Differential Nonlinearity generally OK, but few missing codes found (DNL=-1) needs to be corrected



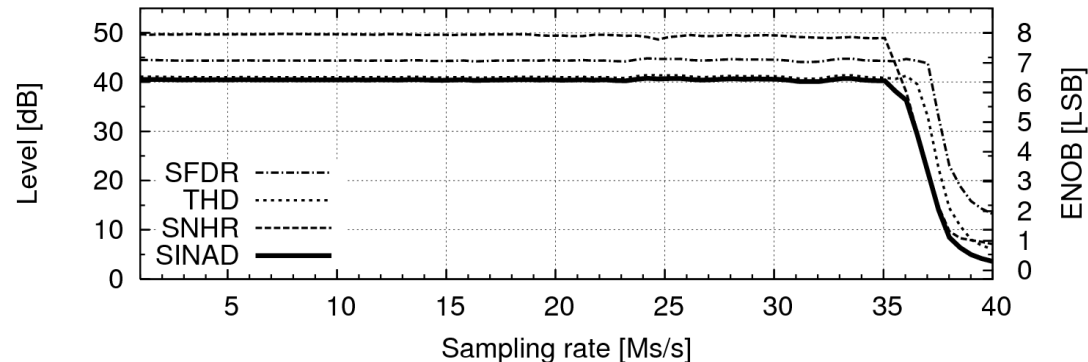
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Example of
FFT spectra

Dynamic FFT ADC tests



Results



- ❑ Stable functionality up to 35 MHz in agreement with simulations
- ❑ Nonlinearity errors (THD) limit the resolution, in agreements with static measurements, to be improved

Measurements status

- ❑ First prototypes of front-end channels and pipeline ADC stages designed, produced and found fully functional
- ❑ Front-end parameters measurements completed, in good agreement with simulations. Measurements with sensors and fanout still needed.
- ❑ Final front-end architecture not yet decided (continuous, gated...?)
- ❑ Setup for ADC measurements established
- ❑ Pipeline ADC stages measurements completed. Small nonlinearity errors found, their sources identified

Summary & milestones

- ❑ First front-end and ADC prototypes successfully tested
- ❑ Few months of delay according to initial schedule (partially because the sensors has not been produced yet)
- ❑ Improved ADC version being prepared for submission - design finished, layout in progress
- ❑ Track&Hold - design completed, layout started
- ❑ DACs - design almost completed
- ❑ Bandgap references - design almost completed
- ❑ Next submission – september 2008