Development of General Purpose Low–power Small–area 10 bit CMOS DAC

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Outline

1. Design of 10b Low–Power Small–Area Current–Steering DAC.
   - Specifications
   - Circuit Design.
   - Layout
2. Measurements of 1^{st} Prototype
   - Static Measurements
   - Power Measurements
   - Transient Measurements
   - Comparison with other low–power 10 bit DACs
3. Summary

Outline

Design of 10b Low–Power Small–Area Current–Steering DAC. Specification

Requirements:

- 10 bit resolution.
- High swing voltage output.
- Low power consumption – below 1 mW.
- Small area.

Considered architectures:

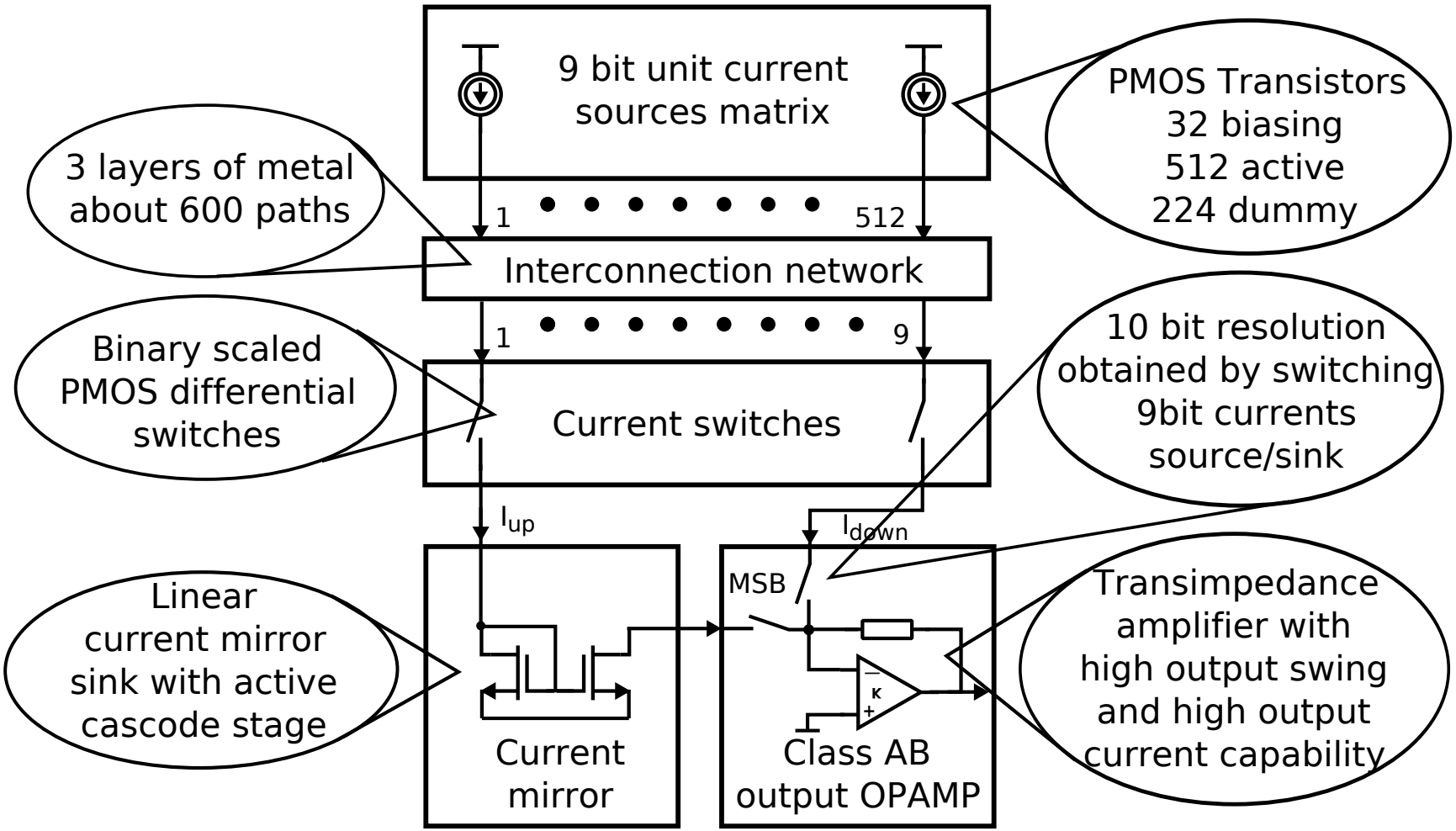
- Current steering.
- Resistors ladder.

Chosen architecture:

- Current steering – matching of MOS better than resistors for given technology.

Outline

Design of 10b Low–Power Small–Area Current–Steering DAC. Circuit Design.



Block diagram of proposed DAC.

Design of 10b Low–Power Small–Area Current–Steering DAC. 9 bit Current Sources Array.

Matching formulas

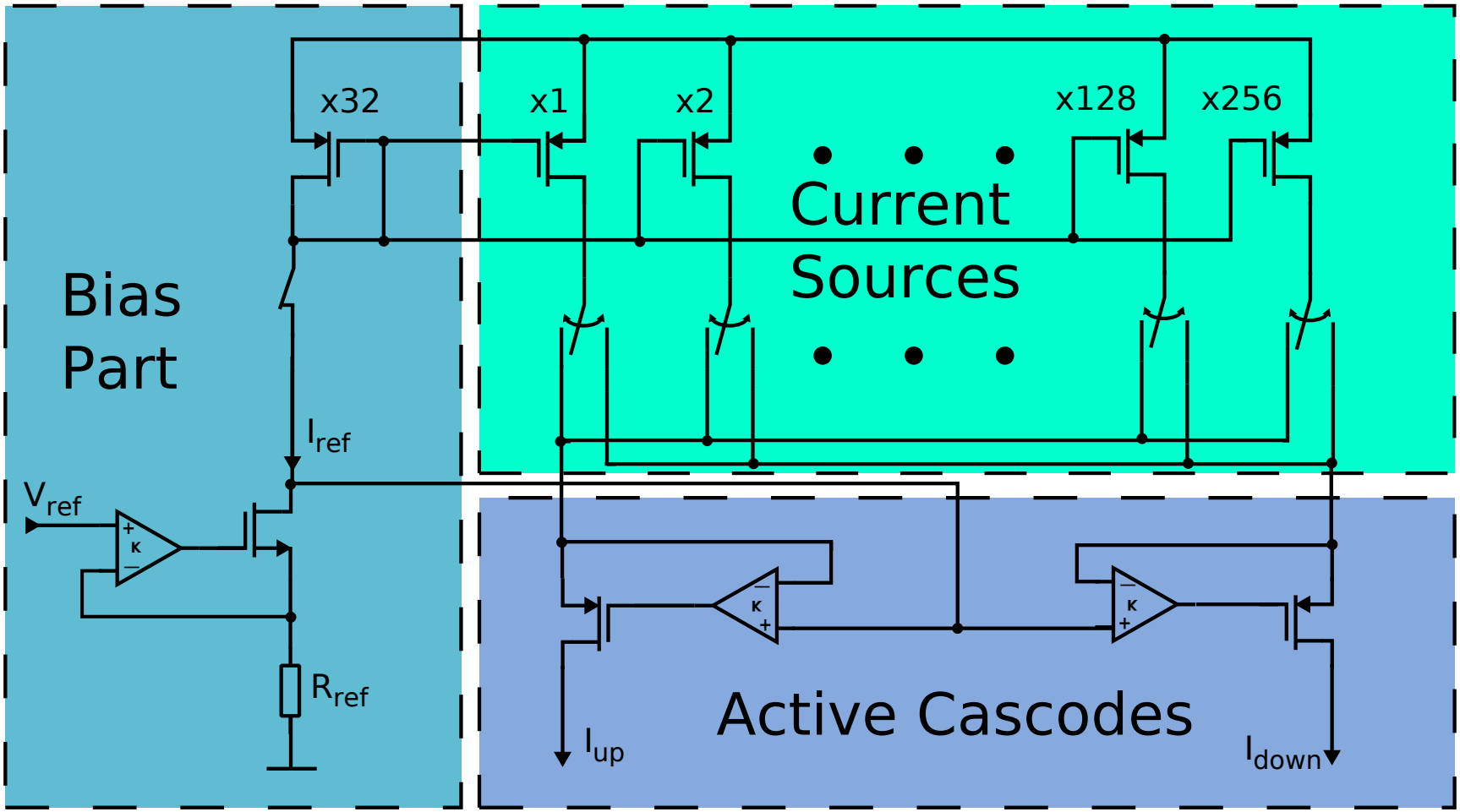
$$\delta I_{MSB} \leq \frac{1}{3} \cdot 2^{-9} \cdot 100\% = 0.065\%$$

$$W \cdot L \geq \frac{1}{\sigma^2(I_D)} \cdot \left[A_\beta^2 + \left(\frac{2 \cdot A_{V_{th}}}{V_{ov}} \cdot 100\% \right)^2 \right]$$

Choice of transistors size:

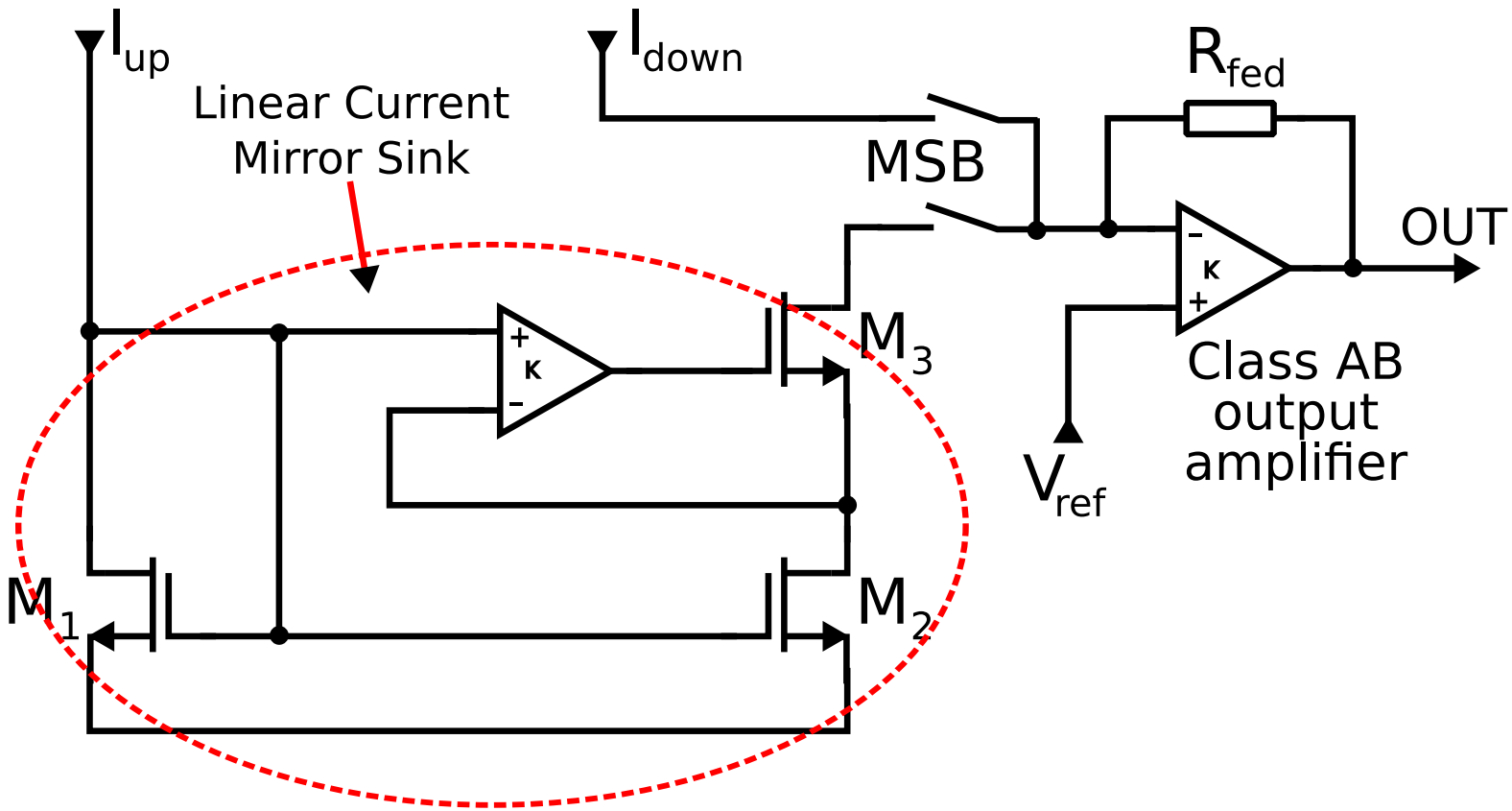
- Assumed LSB current $= 100[nA]$
- Assumed current source overdrive voltage $\geq 500[mV]$
- Chosen transistor type – PMOS
- Chosen W/L unit transistor ratio – 1/80 ($V_{ov} = 637[mV]$)
- Calculated unit current source dimensions – $W/L = 0.5\mu/40\mu$

Design of 10b Low–Power Small–Area Current–Steering DAC. Current Source Array with Active Cascodes Stage.



9 bit current output DAC

Design of 10b Low–Power Small–Area Current–Steering DAC.
High Swing Output Stage Including Current Mirror Sink.



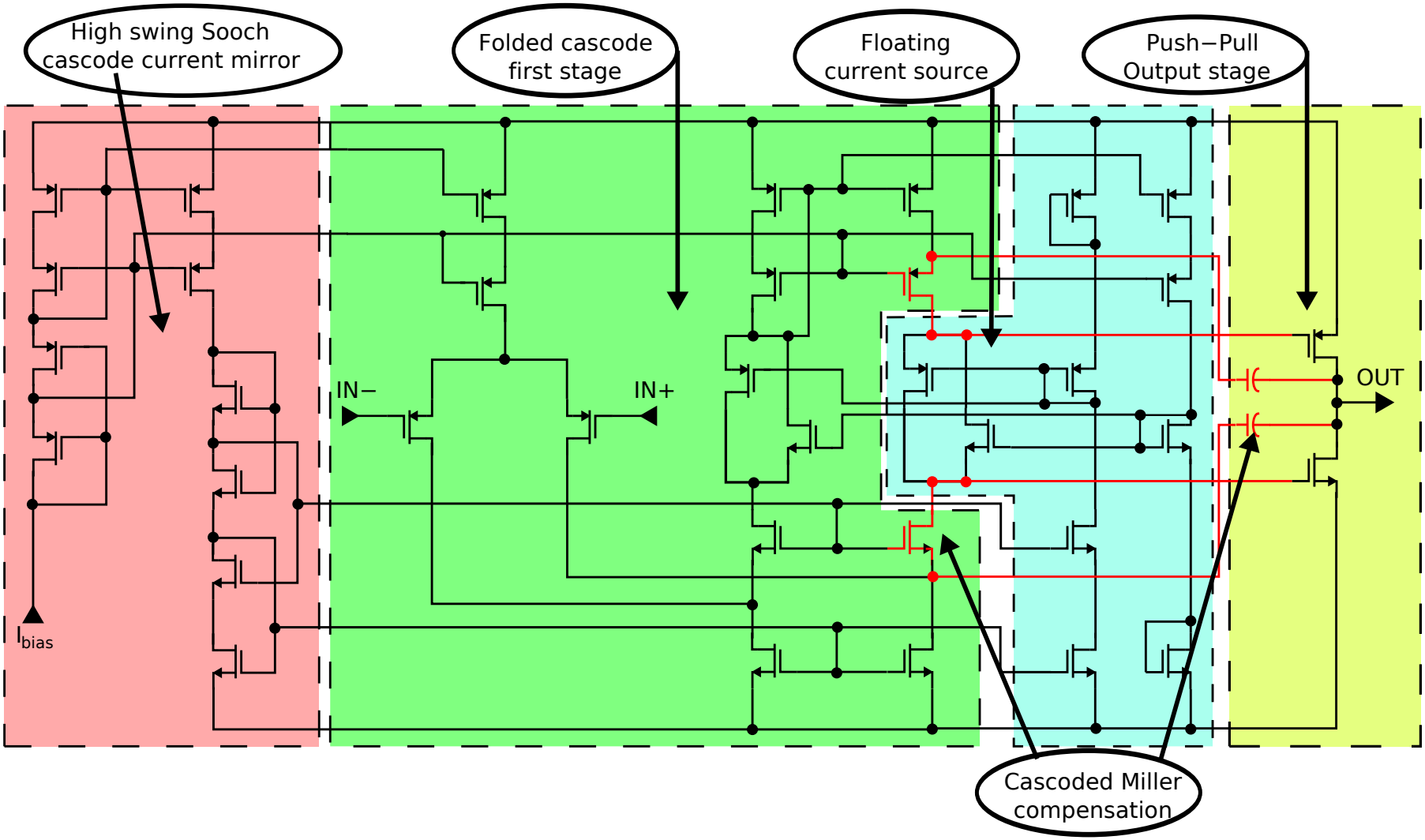
$$\frac{W_1}{L_1} = \frac{W_2}{L_2} = 16 \cdot \frac{3.2\mu}{52.5\mu}$$

Design of 10b Low–Power Small–Area Current–Steering DAC.
Amplifiers used in DAC

Two types of amplifiers were used:

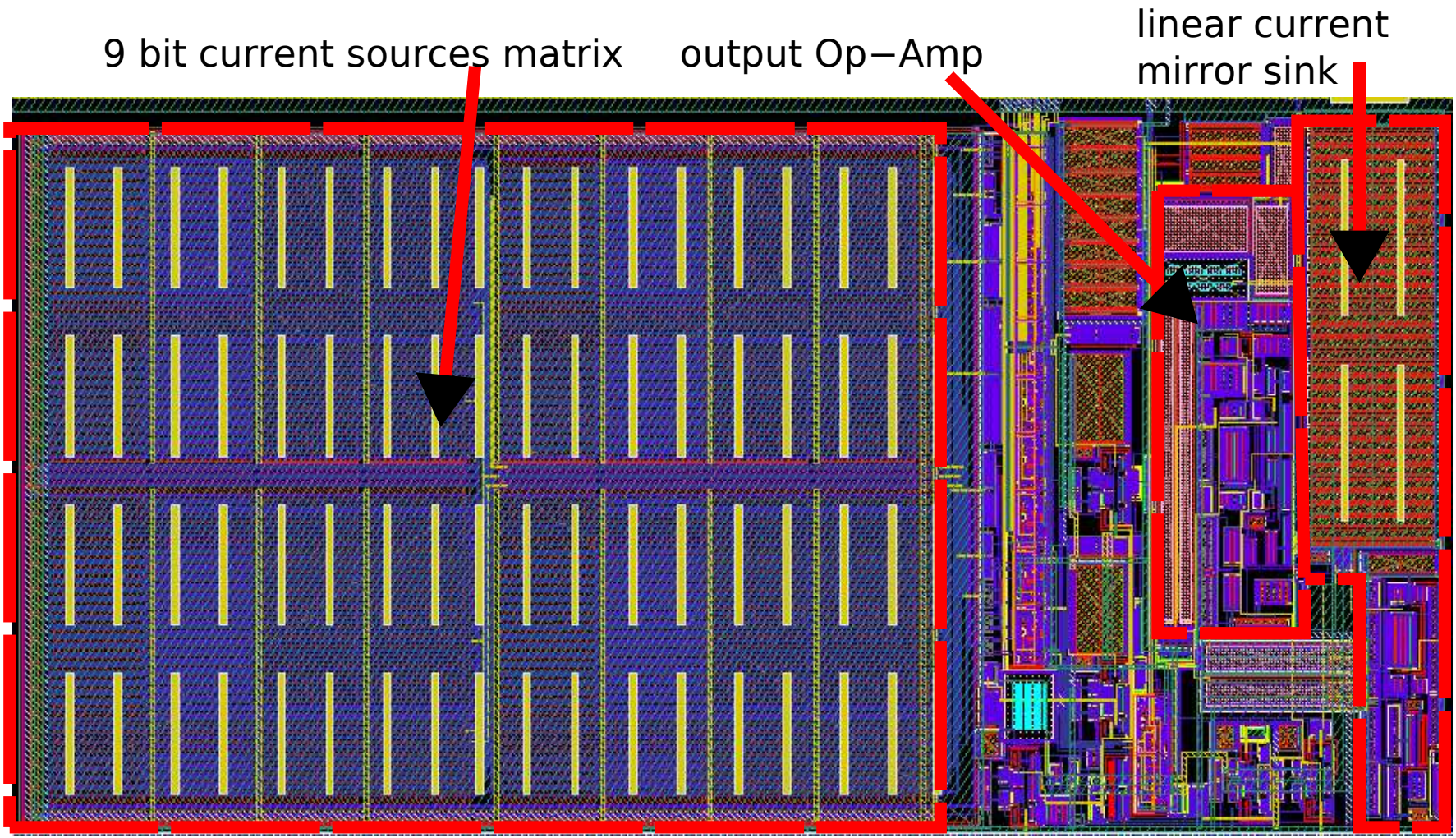
- 6 single stage OTAs in active cascode stages and biasing.
  - Architecture – folded cascode.
  - Power consumption 3.5 – 25 μW.
  - Open loop Gain 60 – 88 dB.
  - Gain x Bandwidth (GBW) 1 – 7 MHz.
  - Phase Margin $>$ 70°.
- One two stage class AB operational amplifier for output current–to–voltage converter.
  - Power consumption – 60 μW (quiscent power).
  - Open loop gain – 115 dB (quiscent load current)
  - GBW – 2 MHz
  - Phase Margin $>$ 75°.

Design of 10b Low–Power Small–Area Current–Steering DAC.
Class AB Operational Amplifier



Outline

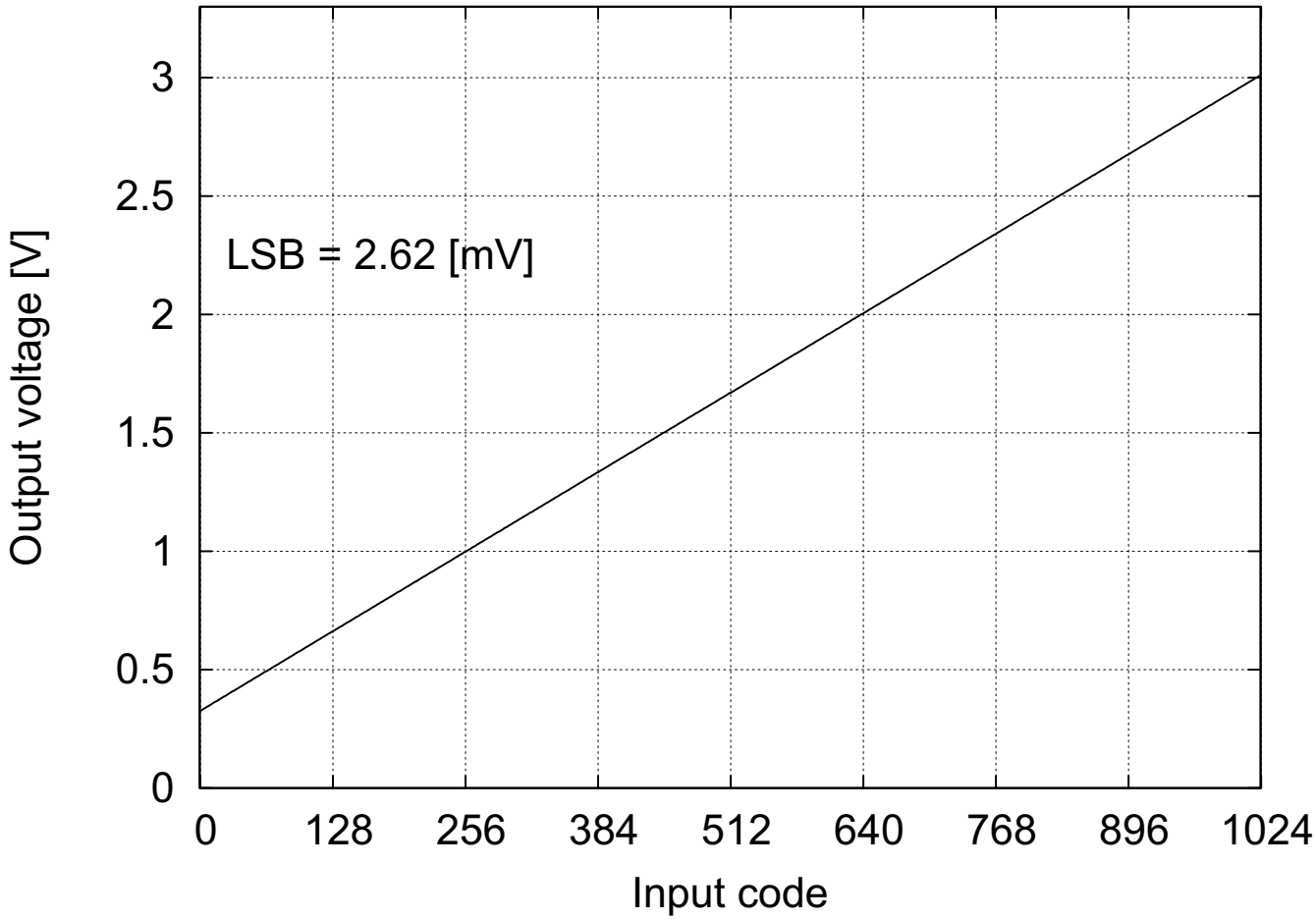
Layout of 1^{st} prototype.



DAC core dimensions – 295x595μm.

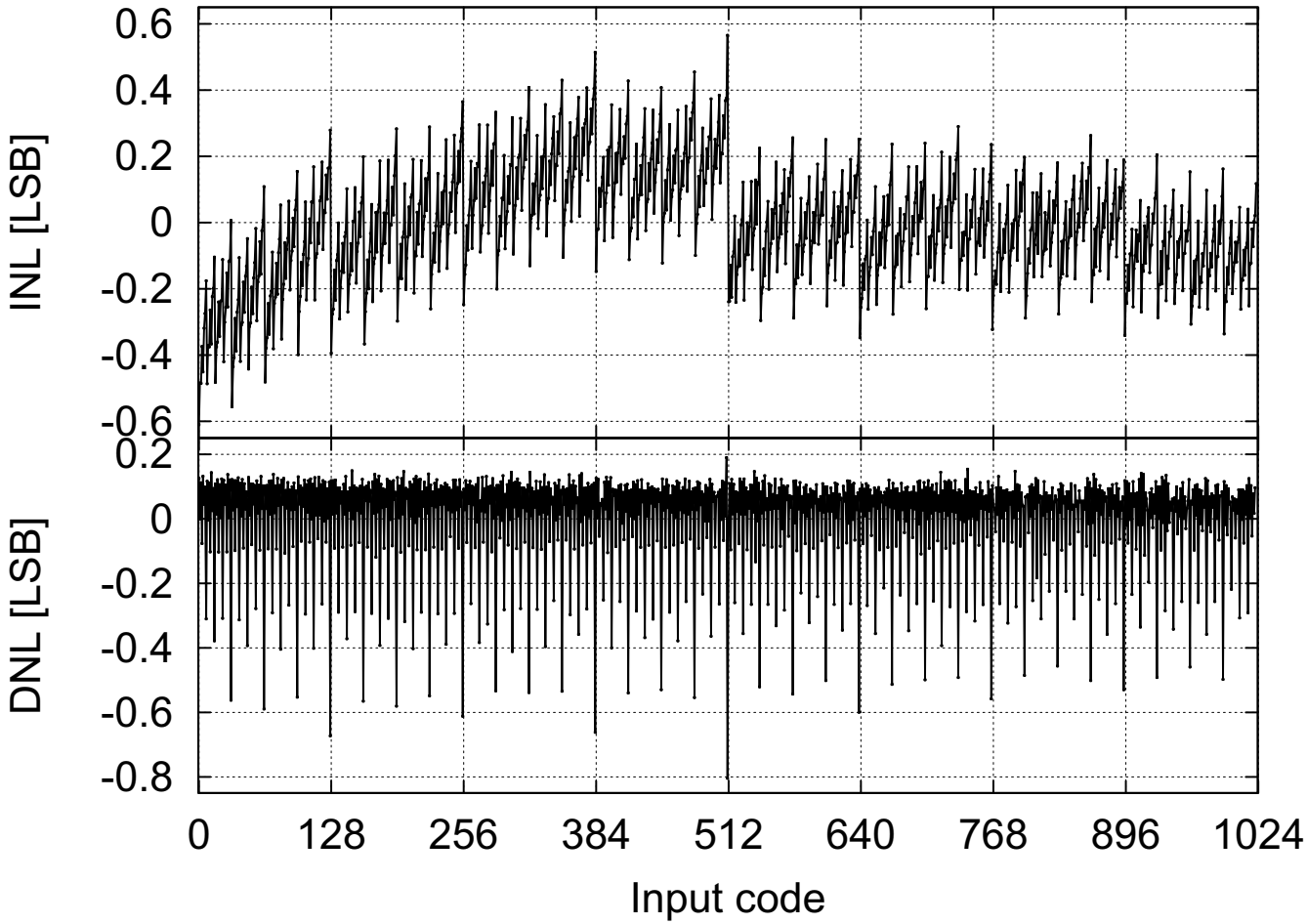
Outline

Measurements of 1st Prototype
Transfer Curve.



Fully functional; Full Scale Range – 2.68 V

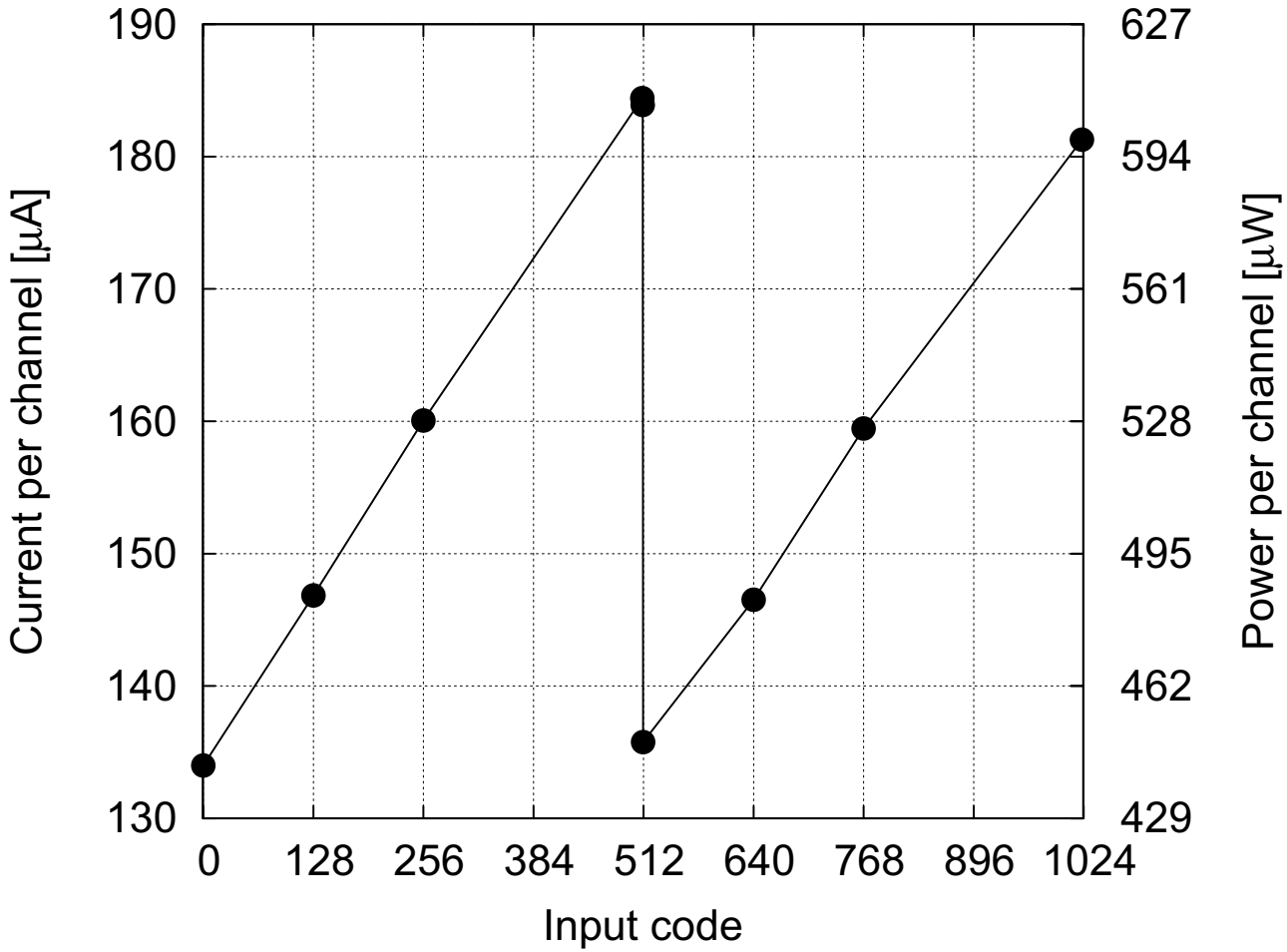
Measurements of 1^{st} Prototype
Integral (INL) and differential (DNL) nonlinearities.



$$|INL_{max}| = 0.6LSB \quad |DNL_{max}| = 0.8LSB$$

Outline

Measurements of 1st Prototype
Power Measurements

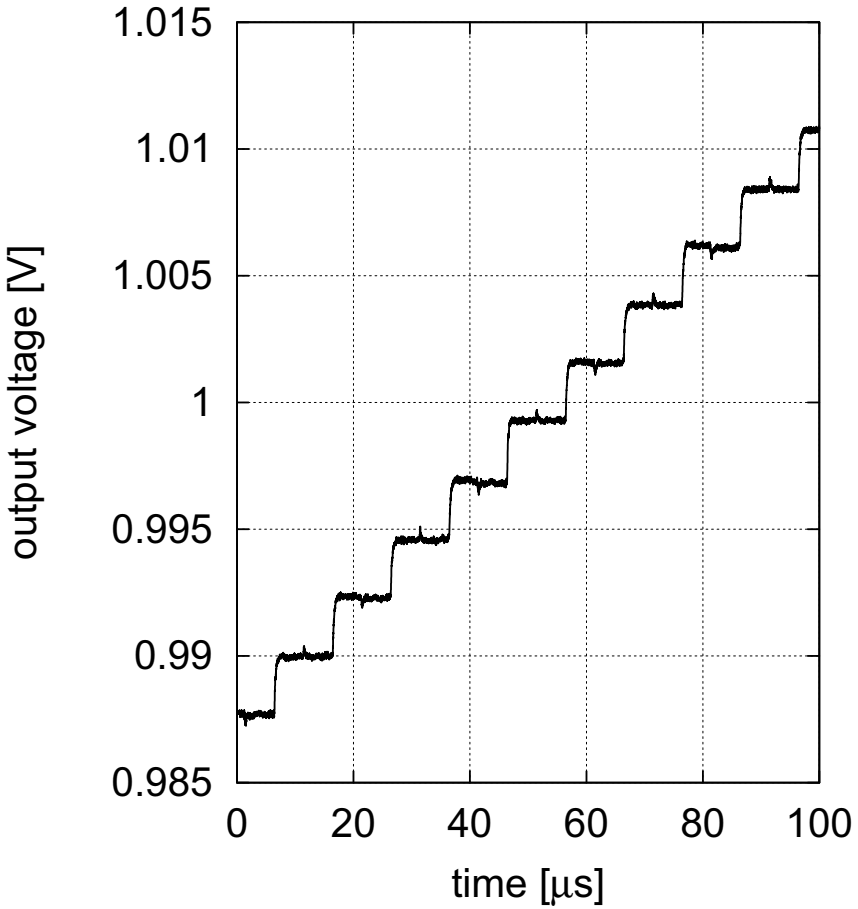


Power consumption vs input code

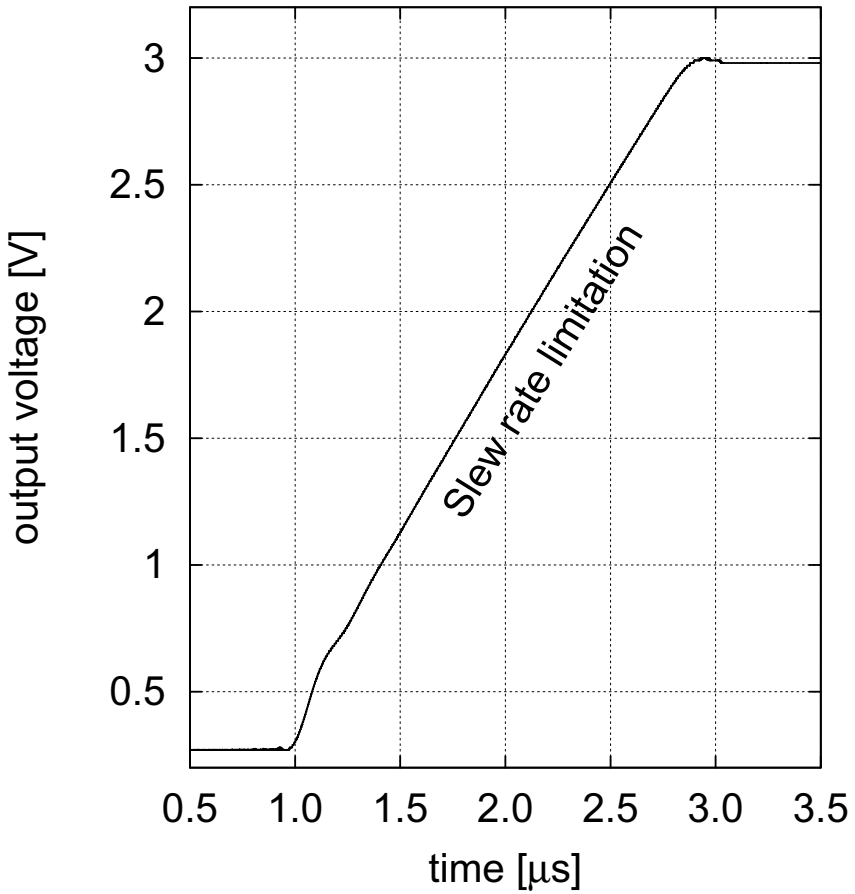
$P_{tot} \in (0.45; 0.6)[mW]$

Outline

Measurements of 1st Prototype
Transient Measurements.



Waveform showing 1 LSB steps.
$t_{set} \approx 0.5\mu s$



Worst case settling time (0 – 1023).
$t_{set} \approx 2\mu s$

Outline

Comparison with other low–power 10 bit DACs

	1	2	3	4	This work
archit.	current steering	R–2R ladder	resistor ladder	resistor string	current steering
tech.	0.35 μm CMOS	0.18 μm CMOS	0.35 μm CMOS	0.13 μm CMOS	0.35 μm CMOS
power [mW]	$\leq$ 7.8	4	0.07 (analog part)	0.5	$\leq$ 0.6
area [mm^2]	0.23	0.01	0.022	0.18	0.18
max INL [LSB]	0.2	0.75	0.7	2.0	0.6
max DNL [LSB]	0.2	0.7	0.35	0.5	0.8
speed	upd. rate 30 MS/s	low freq.	set. time 3 $\mu s/10pF$	upd. rate 2MS/s	set. time $0.5 - 2[\mu s]$
output type	current $\leq$2.5mA	current $<$2.2mA	voltage no buffer	voltage high–swing	voltage high–swing

1 M. Borremans, A. Van den Bosch, M. Steyeart, W. Sansen, *A low power 10–bit CMOS D/A converter for high speed applications*, IEEE 2001 custom integrated circuits conference.

2 B. Greenlay, R. Veith, Dong–Young Chang, Un–Ku Moon, *A low–voltage 10–bit CMOS DAC in 0.01–mm^2 die area*, IEEE Transactions on Circuits and Systems, vol. 52, no 5, 2005.

3 Y. Perelman, R. Ginosar, *A low–power inverted ladder D/A converter*, IEEE Transactions on Circuits and Systems, vol. 53, no 6, 2006.

4 F. Ge, M. Trivedi, B. Thomas, W. Jiang, H. Song, *1.5V 0.5mW 2MSPS 10B DAC with rail–to–rail output in 0.13μm CMOS technology*, SOC Conference, 2008 IEEE International.

Summary

- 1^{st} prototype of 10 bit DAC is fully functional.
- Measurements results are generally in good agreement with simulations:
  - Low power consumption $< 0.6mW$.
  - Small area – 0.295 x 0.595 mm^2 = 0.176 mm^2
  - Integral Non–Linearity ($|INL_{max}|$) $\simeq$ 0.6 [LSB].
  - Differential Non–Linearity ($|DNL_{max}|$) $\simeq$ 0.8 [LSB] – higher than expected, attributed to current source matrix layout.
  - Settling time = 0.5 – 2 μs.
- Improved design is completed and ready for submission.