Development of a General Purpose Low–power Small–area 10 bit Current Steering CMOS DAC

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***Abstract*—The design and measurements of the prototype general purpose digital to analog converter for readout systems in high energy physics experiments are presented. The main goals for the proposed DAC are low power consumptions, small die area and high output swing. The 10 bit DAC design is based on current steering architecture comprising high swing class AB output amplifier. The prototype ASIC is fabricated in the 2P–4M 0.35-μm technology. The measurements of maximum differential (DNL) and integral (INL) nonlinearity show 0.8 and 0.6 LSB respectively. The total power consumption is below 0.6 mW while the area is 0.18 mm^2.**

***Index Terms*—DAC, current steering, high swing, low power, class AB amplifier.**

I. Introduction

Digital to analog converters (DAC) are commonly used in multichannel readout electronics systems designed for high energy physics experiments like ILC (International Linear Collider). Often a large number of precise DACs is required to be used in a single ASIC to control various parameters. For this reason a general purpose moderate resolution low power small area DAC is one of the required components in such systems. The goal of this paper is to design a 10 bit resolution, high-swing, low power, small area DAC.

Among the most popular are the DACs based on current steering architecture. Current steering DACs are very well suited for implementation in standard CMOS process and they provide a good compromise between the occupied area, power consumption and speed. Other commonly applied architecture with similar advantages uses resistor strings.

In this work the current steering architecture is chosen, which is motivated mainly by the comparison of the resistor and transistor matching for the given technology. In section II the design of the proposed DAC is described. The measurements performed on few prototypes are presented in section III. In section IV the comparison of this work with the state of the art DACs is shown and possible improvements for the next prototype are discussed.

II. Circuit design

The block diagram of the proposed DAC is shown in figure 1. The core component is a binary weighted 9 bit current source matrix. A 10 bit resolution is achieved by mirroring the current from the 9 bit current matrix and switching (MSB switch) between the current source or sink at the input of the current to voltage converter. To obtain high output swing and high current drive capability a class AB rail-to-rail output transimpedance amplifier is used in the current to voltage converter. The reference potential of the output amplifier is set externally (by default at half of power supply voltage). To guarantee a constant drain–source voltages in the current sources matrix and in the current mirror and to increase the output resistance an active cascode stage is used in both these blocks.

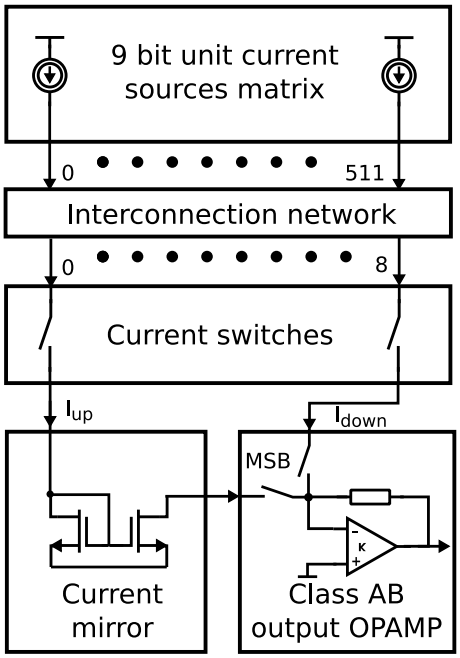

Fig. 1. Block diagram of proposed circuit.

A. Current sources matrix

The current source matrix consists of 511 unit current PMOS sources mirroring the currents from the reference source I_{ref} (see figure 2). In general the requirement of N bit DAC resolution implies achieving an error of less than 0.5 LSB. For a current steering DAC it translates to a maximum error on the MSB current given by the expression [1]:

$$\frac{\Delta I_{MSB}}{I_{MSB}} \leq \frac{100\%}{2^N} \tag{1}$$

For a 9 bit accuracy the error on MSB current should be less than 0.19 %. To satisfy this requirement at 99% confidence level ($\sim 3\sigma$ of Gaussian distribution), the standard deviation of MSB current should be 3 times lower. In this design the size of the unit current source is chosen to guarantee the INL of $\pm$ 0.5 LSB (3σ level) and is calculated using the Pelgrom model [2]. The Width–to–Length (W/L) transistor ratio is determined by the overdrive voltage, while the area of the unit transistor is determined by the deviation of drain current. Knowing that the W/L ratio is given by expression:

$$\frac{W}{L} = \frac{2 \cdot I_D}{\beta \cdot V_{ov}^2} \tag{2}$$

the area of the unit current source is given by:

$$W \cdot L \geq \frac{1}{\sigma^2(I_D)} \cdot \left[A_\beta^2 + \left(\frac{2 \cdot A_{V_{th}}}{V_{ov}} \cdot 100\% \right)^2 \right], \tag{3}$$

where $\beta = \mu_0 \cdot C_{ox}$ is current gain factor, $V_{ov} = V_{gs} - V_{th}$ is transistor overdrive voltage, A_β and $A_{V_{th}}$ are process dependent matching parameters for current gain factor and threshold voltage respectively.
To fulfil low power consumption requirement a very low LSB current value of about 100 nA is chosen. As can be seen from equations (2) and (3) the current deviation is inversely proportional to the overdrive voltage, which is proportional to the square root of the drain current. These limitations force the designer to use very small W/L ratio. In the 9 bit current source matrix of the proposed DAC the W/L ratio of the unit current source is set to $0.5\mu/40\mu$.

B. Current switches

For best matching a unit current source and its correspondent switches should constitute a single cell in a matrix. Unfortunately the drawback of such solution is an increased ASIC area. To minimize the area a binary scaled current switches are used. For the LSB switch a minimum transistor dimensions ($0.4\mu/0.35\mu$) are chosen. In spite of its small dimensions the resistance of the switches is negligible compared to the current sources resistance. In addition, smaller switches result in smaller capacitance and lower feedthrough charge injections. This allows to achieve smaller glitches and so the better dynamic performance of the DAC.

C. Active cascodes stage.

In order to make the drain current independent of the error associated with the channel modulation factor, the active cascode stages shown in figure 2 are used.
The reference potential of the active cascode amplifiers is set to guarantee the equal drain potentials on both sides of the current mirrors. In addition, the active cascode circuit strongly increases the output resistance of current sources, which is given by expression:

$$r_{out} \simeq K_0 \cdot g_m \cdot r_{ds} \cdot r_{CS}, \tag{4}$$

where K_0 is the open loop amplifier gain, g_m and r_{ds} are the transconductance and drain–source small signal resistance

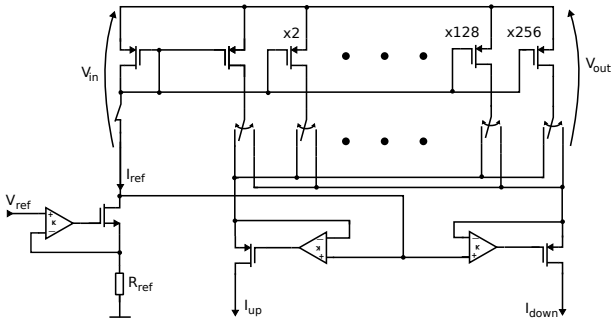

Fig. 2. Block diagram of active cascode stage.

of cascode transistor and r_{CS} is a small signal resistance of current source.
Another advantage of adding active cascode is filtering of the glitches caused by charge injection from switching.
Very important issue of an active cascode stage is its stability. The dominant pole of this stage is the first pole of cascode amplifier while the nondominant one is related to the transconductance of a cascode transistor and is given by:

$$p_{nd} \approx \frac{g_m}{C_{cs}}, \tag{5}$$

If the DAC is set to a state providing zero current on active cascode transistor, then the nondominant pole of this stage moves to zero and the circuit becomes unstable. To alleviate this problem a dummy source (not shown in figure 2) guaranteeing minimum current in the cascode transistor (and so minimum g_m) is added.

D. High swing output amplifier

In order to obtain a rail–to–rail output swing the DAC current may be source (sink) into (from) the output transimpedance amplifier. The block diagram of the designed current mirror sink and the class AB rail-to-rail output amplifier is shown in figure 3.

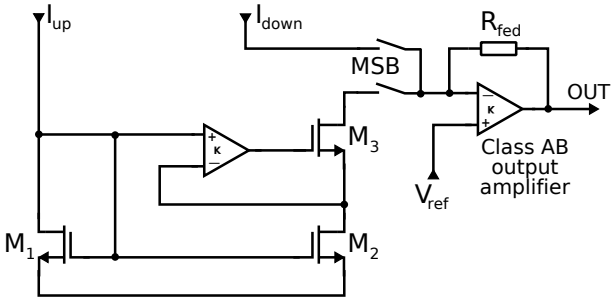

Fig. 3. Block diagram of high swing output circuit.

Depending on the MSB switch configuration the 9 bit current matrix may either source the current I_{down} into the output amplifier or sink the mirrored current I_{up} from the output amplifier. The value of voltage drop corresponding to the DAC LSB is set by the feedback resistance R_{fed}. In this work R_{fed} was selected to have the LSB of about 2.5mV. Because of this

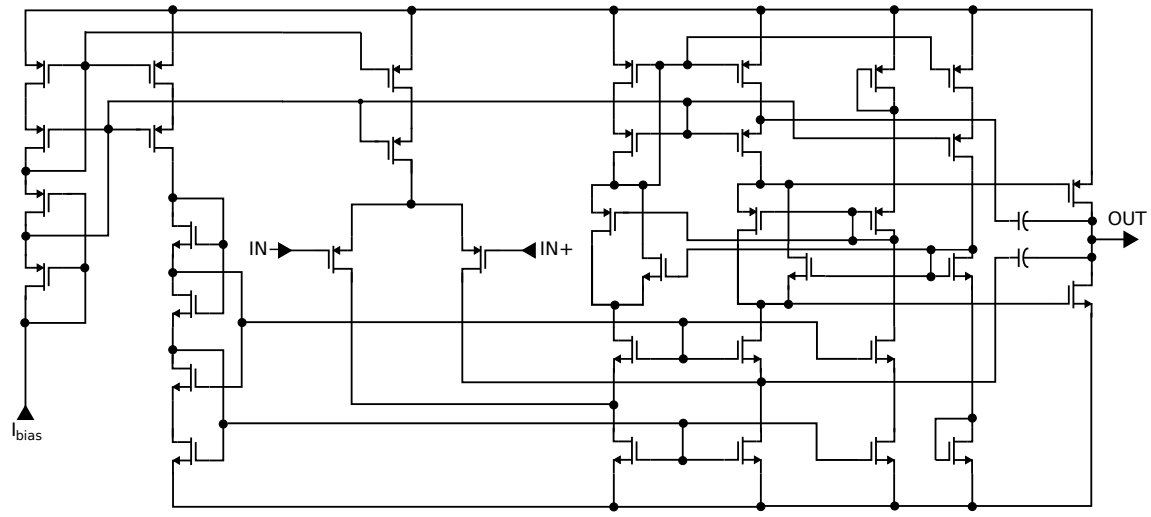

Fig. 4. Schematic diagram of class AB output amplifier.

choice, even if the output amplifier allows a rail-to-rail swing, the actually implemented swing is few hundred milivolts less. If needed, the LSB and the output swing amplitude may be adjusted by changing the R_{fed} value. The relation between the two complementary currents I_{up} and I_{down} is given by the expression:

$$I_{down} = 511 \cdot I_{LSB} - B_{dec} \cdot I_{up}, \tag{6}$$

where B_{dec} is the decimal code representing DAC state (without MSB bit). If the MSB bit is set to 0, then the I_{down} switch is closed and the output voltage is set in the range from $V_{ref} - B_{dec} \cdot I_{LSB} \cdot R_{fed}$ up to V_{ref}. If the MSB bit is set to 1 the I_{up} current is mirrored by the current mirror and the output voltage sets in the range from V_{ref} up to $V_{ref} + B_{dec} \cdot I_{LSB} \cdot R_{fed}$.

The equality of currents in the mirror is guaranteed by setting equal drain–source voltages of transistors M_1 and M_2, which is done by an active cascode amplifier. The size of transistors M_1 and M_2 is chosen to match their currents better than half of the LSB current (on 3σ deviation level). The layout of the current mirror M_1, M_2 is drawn in a common–centroid matrix of 32 NMOS transistors. The size of unit transistor is set to $W/L = 3.2\mu/52.5\mu$. Such sizing guarantees the matching error below 0.5 LSB but results in a large time constant (low transconductance and high capacitance of the mirror) increasing about 3 times the rise time of output signal. To improve the settling time, a smaller transistors with trimming will be used in the next prototype.

E. Amplifiers design

In the proposed DAC, two types of amplifiers are used. Most of the amplifiers (except from the output amplifier) do not require high swing and high current drive capability. For this reason in all these cases a single stage operational transconductance amplifier (OTA) is used. On the other hand the output amplifier requires both high output swing and high output current capability. For this reason it is designed as a two stage operational amplifier with rail–to–rail class AB output stage.

1) Single stage OTAs: Each OTA is built using a folded cascode amplifier configuration. Depending on the desired input voltage value the OTA amplifiers use either NMOS or PMOS input differential pair. The power consumption of these amplifiers is below 15 μW per OTA.

2) Class AB operational amplifier: To fulfil the requirement of high output swing and wide output current range a rail–to–rail output class AB amplifier is chosen. A schematic diagram of the designed amplifier is shown in figure 4. The first amplifier stage is built as a folded cascode amplifier, while the second stage uses class AB (Push–Pull) configuration. The Push–Pull stage is biased by a floating current source [3]. To ensure stability the cascoded Miller compensation technique is used. This compensation provides better PSRR ratio and requires about 2 to 3 times smaller compensation capacitance compared to a classical Miller compensation technique [4]. The simulated gain and unity gain bandwidth are respectively 115 dB and 2 MHz. The power consumption is below 60 μW.

III. Measurements results

The first prototype of the designed DAC is fabricated in the two–poly four–metal n–well 0.35 μm CMOS technology. The dimensions of the DAC core are 295 μm x 595 μm. In figure 5 the photograph of the prototype ASIC glued and bonded to the PCB is shown. The results of the performed static, dynamic and power consumption measurements are presented below.

A. Static measurements

Static parameters measurements are done using the Agilent B1500 Semiconductor Devices Analyser. In order to check the DAC functionality the measurement of transfer function (output voltage vs DAC input code) is performed first. The observed curve is shown in figure 6. The results are in very

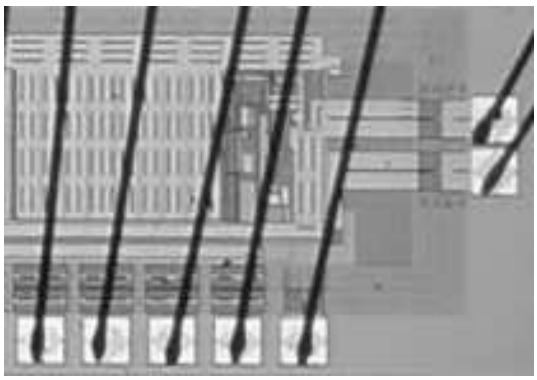

Fig. 5. Photograph of glued and bonded prototype.

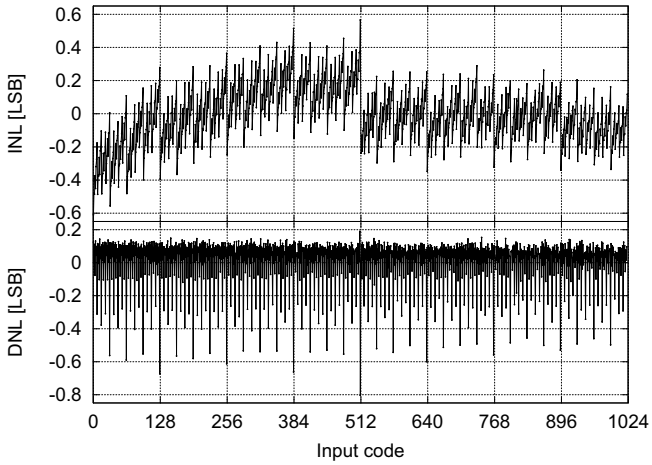

Fig. 7. Measured INL and DNL nonlinearities.

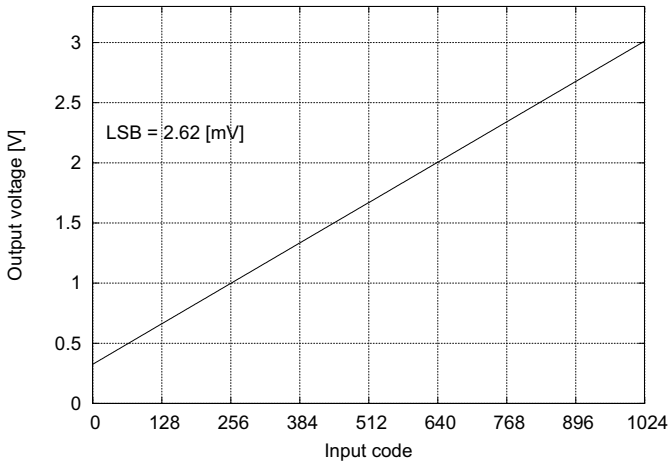

Fig. 6. Output voltage vs DAC input code.

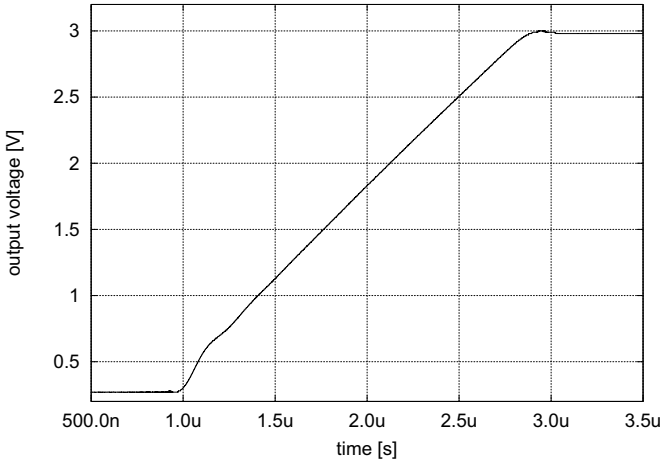

Fig. 8. Waveform showing settling between 0 and 1023 input code

good agreement with the simulations. Although the DAC output stage allows the rail–to–rail swing the design parameters are chosen to set the output voltage values within a slightly smaller range. For precise characterization of static behaviour the nonlinearity measurements are done. The integral (INL) and differential (DNL) nonlinearity are shown in figure 7. The maximum INL and DNL values are 0.6 LSB and 0.8 LSB respectively. While the INL is quite satisfactory, the maximum DNL is slightly above the expectations. Even if most of the states show the DNL value below ± 0.5 LSB, there are some states exceeding this range. In order to improve the DNL the layout of the current source matrix will be redesigned for the next submission.

B. Transient measurements

Although dynamic behaviour is not a main issue in this design, few transient measurements are done for the better ASIC characterization. The measurements are performed sending the digital code into the DAC inputs at a given clock frequency and observing the analog output waveform with the TDS3034 scope. A worst case settling time is measured changing the input code between the values of 0 and 1023. The transient response in such case is shown in figure 8 where the settling time of about 2 μs is found. It is seen that long settling time comes from the slew rate limitation. If needed it could be improved by allowing more power into the output amplifier. Figure 9 shows an output waveform obtained changing the input code by one LSB with 100 kHz clock frequency. In this case the observed rise time is always below 500 ns. One can see that converter practically does not show glitches. The glitches from switching are suppressed by using active cascode stages in the current mirrors and by additional filtering (capacitance parallel to R_{fed}) in the feedback of the output amplifier.

TABLE I
COMPARISON WITH OTHER DACS

	[5]	[6]	[7]	[8]	[9]	This work
architecture	current steering	current steering	R–2R ladder	resistor ladder	resistor string	current steering
resolution [bits]	10	10	10	10	10	10
technology	0.35 μm CMOS	0.18 μm CMOS	0.18 μm CMOS	0.35 μm CMOS	0.13 μm CMOS	0.35 μm CMOS
power cons. [mW]	$\leq$ 7.8	$\leq$ 22	4	0.07 (analog part)	0.5	$\leq$ 0.6
area [mm^2]	0.23	0.35	0.01	0.022	0.18	0.18
max INL [LSB]	0.2	0.1	0.75	0.7	2.0	0.6
max DNL [LSB]	0.2	0.1	0.7	0.35	0.5	0.8
speed	upd. rate 30 MS/s	upd. rate 250MS/s	low frequency	set. time 3 $\mu s/10pF$	upd. rate 2MS/s	worst set. time 2 μs 1 LSB rise time $<$ 500 ns
output type	current $\leq$2.5mA	current $\leq$10mA	current $<$2.2mA	voltage without buffer	voltage high swing	voltage high-swing

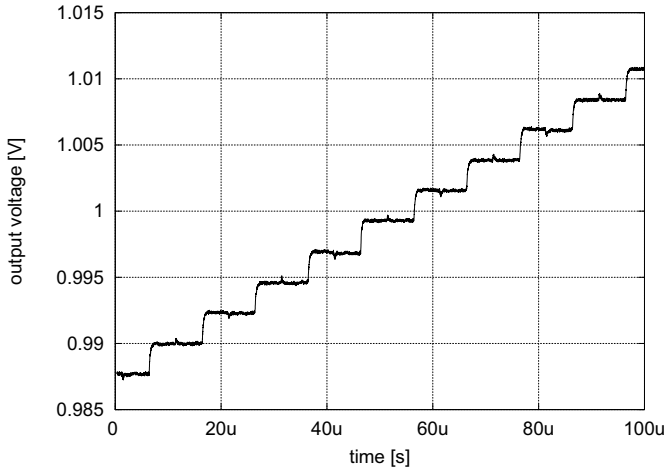

Fig. 9. Waveform showing 1 LSB steps transient

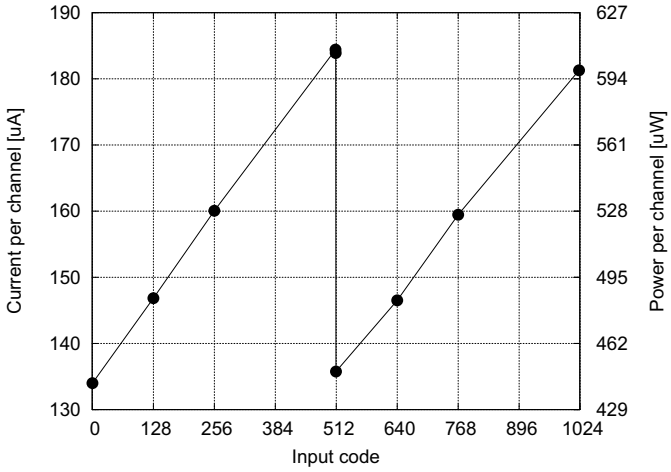

Fig. 10. Power consumptions vs DAC input code.

C. Power consumption

The power consumption from 0.45 mW (B_{dec} low) up to 0.6 mW (B_{dec} high) is measured and its dependence on input code is shown in figure 10. A nonmonotonic relation between DAC input code and power consumption results from the MSB switching between the current matrix sources and the current mirror. The measurement results are in good agreement with simulations.

IV. COMPARISON WITH OTHER DACS

In this section the present work is compared with the published state of the art 10 bit DAC designs. For clarity all designs with relevant parameters are presented in table I.
The designs [5] and [6] are presented here only for a general overview and because of the same current steering architecture. Both designs are aimed mainly at higher update rates (what is reflected by the power consumption) and so a current as the output signal is used in these works.
Also the design described in [7] uses current as the output but the main goal in [7] is to have general purpose static DAC, what is closer related to the presented work. The main advantage of that work is extremely small area of 0.01 mm^2 (mainly due to R-2R ladder architecture) but comparing to the design presented here one should remember about its lack of current to voltage converter and the smaller technology size. On the other hand the power consumption in [7] is significantly higher while the conversion rate is not given quantitatively compared to the presented design.
A very interesting 10 bit resistor ladder DAC is presented in [8]. It is a static converter with very low power consumption (70 μW analog part) and very small area (0.022 mm^2). Converter presented in [8] provides a voltage output but because of the lack of output buffer its high output resistance (40 $k\Omega$) limits the driving capabilities.

The last among compared works [9] uses the resistor string architecture. The DAC presented in [9] has the closest functionality to the presented design since it has a voltage output with rail-to-rail class AB output amplifier. Also the die area and the power consumption in [9] are very similar to the presented design. The performance of that design is also quite similar to the results presented here but it should be kept in mind that the DAC in [9] is fabricated in much smaller size technology (0.13 μm CMOS).

V. Conclusions

In this paper the design and measurements of a low power small area 10 bit DAC with high output swing are presented. The prototype DAC is fully functional and the performed measurements are in good agreement with the simulations. In particular the low power consumption (0.6 mW) and the good integral nonlinearity (0.6 LSB) are measured. The maximum differential nonlinearity measured is slightly above the expectations (0.8 LSB). In order to improve the DNL the layout redesign will be addressed in the next submission.

Acknowledgment

This work was partially supported by the Commission of the European Communities under the 6^{th} Framework Programme "Structuring the European Research Area", contract number RII3-026126. It was also supported in part by the Polish Ministry of Science and Higher Education under SPUB nr 112/E-356/SPB/DESY/P-03/DZ376/2003-2005 and under contract nr 372/6.PRUE/2007/7.

The authors would like to thank Piotr Wiacek and Szymon Kulis for technical help and Tomasz Fiutowski and Krzysztof Swientek for fruitful discussions.

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