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Praca dyplomowa

Development of a 10-bit ultra-low power SAR ADC in 130 nm CMOS technology

Rozwój 10-bitowego ADC typu SAR, o ultra-niskim poborze mocy, w technologii CMOS 130 nm

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Introduction

Physics aims to understand the fundamental principles, that govern the behavior of matter, energy and interactions. As experimental techniques advance, increasingly precise measurements are required to validate theoretical models and search for new phenomena. One of the most demanding fields is High Energy Physics (HEP), where subatomic particles are accelerated to extreme energies and collided to study the resulting interactions.

In modern scientific experiments, particularly in particle physics, it is important to accurately measure and process signals from detection systems. At the Large Hadron Collider (LHC), particle collisions are studied using large detectors, which rely on dedicated readout electronics to convert sensor signals into data that can be analyzed in order to understand the laws of physics. These systems have played a significant role in confirming predictions of the Standard Model, including the historic discovery of the Higgs boson in 2012. As particle physics experiments become more complex, the need for precise measurements of signal amplitude, time and position becomes even greater. At the same time, reducing power consumption is now a top priority, particularly in large-scale setups, where millions of readout channels operate.

The goal of this work was to redesign the existing Successive Approximation Register (SAR) Analog-to-Digital Converter (ADC) to reduce power consumption by adding a programmable threshold for the input signal, which stops the conversion process if the signal level is below threshold. By skipping unnecessary conversions, this approach minimizes energy usage while maintaining critical functionality.

This thesis is split into four parts. The first chapter is short introduction to high-energy physics and the experiments in this field at LHC or at Deutsches Elektronen-Synchrotron (DESY). It explains how detection systems work and why precise signal processing matters in these experiments. Particular focus is given to front-end ASICs and their role in extracting physical observables from detector data. The chapter also discusses how the increasing complexity of modern experiments affects the design of readout systems.

The second chapter focuses on ADCs, explaining their key characteristics and important parameters, which are essential for understanding the challenges of designing low-power, high-precision readout systems. Several ADC architectures are compared in terms of power, resolution and speed. The metrics used to evaluate ADC performance are described in detail.

In the third chapter, the entire design process of the ADC in CMOS 130 nm circuit is described. It starts with the basic idea of how the ADC works, then moves to the electronic schematic design, and finally explains how the physical layout is created. Throughout the design process, the main goal is to reduce power consumption without compromising overall performance.

The final chapter provides a detailed analysis of simulation results, including Monte Carlo and worst-case scenarios. These simulations were performed to verify the circuit's performance under extreme operating conditions, ensuring the ADC meets the strict requirements of high-energy physics experiments. The effects of parasitics, mismatch and process variation are studied. Comparison with other designs confirms the efficiency of the proposed approach.

This work advances the development of energy-efficient readout systems, supporting future experiments to operate sustainably with minimal power consumption. The proposed solution demonstrates that significant power savings can be achieved without moving to more advanced CMOS process nodes. It offers a scalable solution for multi-channel integration in modern detectors. The results provide a solid foundation for further development and future ASIC prototyping.

1 Short Introduction to High Energy Physics

High Energy Physics explores the fundamental building blocks of the universe and the forces that govern their interactions. Decades of research have revealed that all visible matter is composed of a small set of elementary particles. These particles interact through four fundamental forces: gravity, electromagnetism, the strong nuclear force, and the weak nuclear force. To explain these particles and interactions between them, physicists developed the Standard Model of particle physics.

1.1 Standard Model

The Standard Model is one of the most successful theories in physics, describing how elementary particles and three fundamental forces (strong, electromagnetic, and weak) interact [3]. It classifies particles into two main categories: quarks and leptons with properties shown in Table 1.1. Quarks combine to form mesons and baryons, while leptons include well known particles like electrons and neutrinos. These particles acquire mass through interactions with the Higgs field, discovered in 2012 at the LHC.

Table 1.1: Elementary fermions in the Standard Model [4]

Fermion	Family			Charge
quark	up (u)	charm (c)	top (t)	$2/3$
	down (d)	strange (s)	bottom (b)	$-1/3$
lepton	e	μ	τ	-1
	ν_e	ν_μ	ν_τ	0

The interactions between these particles are mediated by force carriers, as shown in Table 1.2. These carriers act as messengers of the forces:

- The photon (γ) transmits electromagnetic interactions (e.g., light, electric fields).
- The W^+, W^-, and Z bosons mediate the weak force, responsible for processes like nuclear beta decay.
- Gluons bind quarks together via the strong force, forming mesons and baryons.

Table 1.2: Fundamental Force Particles (excluding Gravity)

Force	**Particles**	**Force Carrier**	**Range**
Weak Force	Quarks, Leptons	W^+, W^-, Z	Short range
Electromagnetism	Electrically charged	Photon (γ)	Infinity
Strong Force	Quarks	Gluons	Short range

Gravity is not part of the Standard Model. At the subatomic scale, its effects are too weak to matter, and no quantum theory of gravity has been proven experimentally.

While the Standard Model was confirmed by discoveries like the top quark in 1994 and Higgs boson in 2012, it still remains incomplete. Some phenomena, like neutrino oscillations, dark matter, and the Higgs mass hierarchy, cannot be explained by the Standard Model, suggesting the need for new theory. Understanding and solving these gaps is the main mission of particle physics experiments, such as those at the LHC and future colliders, which aim to uncover physics beyond the Standard Model.

1.2 Experiments in HEP

The biggest and most known particle accelerator in the world is Large Hadron Collider at CERN. It consists of a 27-kilometer circular tunnel located 100 meters underground, spanning the border between Switzerland and France. The LHC accelerates protons and heavy ions to nearly the speed of light, colliding them to recreate conditions similar to those just after the Big Bang, allowing scientists to study fundamental particles and forces.

The CERN accelerator complex presented in Figure 1.1 works like a particle factory, where protons are prepared and boosted in stages before entering the LHC [5]:

- **Stage 1 - Proton Source:** Hydrogen atoms are stripped of electrons, creating protons that get their first speed boost in a linear accelerator.
- **Stage 2 - Pre-acceleration:** Protons enter smaller circular accelerators that increase their energy step-by-step.
- **Stage 3 - Final Boost:** The Super Proton Synchrotron accelerates protons to around 99.9% light speed before injecting them into the LHC.
- **Stage 4 - LHC Operations:** In the 27-km LHC ring, protons reach 13.6 TeV energy, colliding with each other to create new particles.

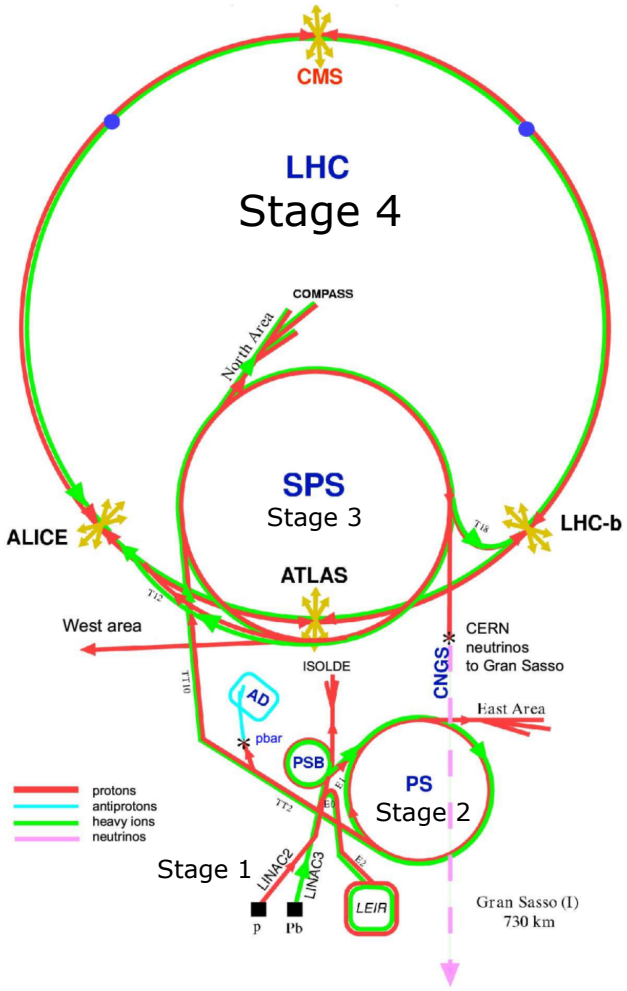

Figure 1.1: The accelerator complex of CERN with the Large Hadron Collider [5]

The LHC tunnel was originally constructed for the Large Electron-Positron Collider (LEP), a circular electron-positron collider that operated from 1989 to 2000 and was dedicated, among other goals, to the search for the Higgs boson. Although LEP reached a maximum center of mass energy of 209 GeV, it fell just short of making a discovery. With the physics potential limited by energy, CERN engineers upgraded the infrastructure to build the LHC, capable of proton-proton collisions at energies nearly 100 times higher. This upgrade proved essential for the successful discovery of the Higgs boson in 2012.

Another large particle accelerator, other than the LHC, is located at DESY in Hamburg. This research center, located in Hamburg, Germany, operates a 2.3 kilometer synchrotron called PETRA III, which generates extremely bright X-ray beams. These beams enable high-resolution studies of matter at the atomic and molecular scale. Between 1992 and 2007, DESY also hosted the Hadron-Electron Ring Accelerator (HERA), a 6.3-kilometer collider that uniquely collided electrons (or positrons) with protons. The entire research campus is shown in Figure 1.2. Today, DESY focuses primarily on photon science and synchrotron radiation applications, while electron-proton collisions are now being explored at the Facility for Antiproton and Ion Research (FAIR) at GSI in Darmstadt. FAIR aims to study the properties of dense nuclear matter through high-energy collisions involving protons, antiprotons and heavy ions.

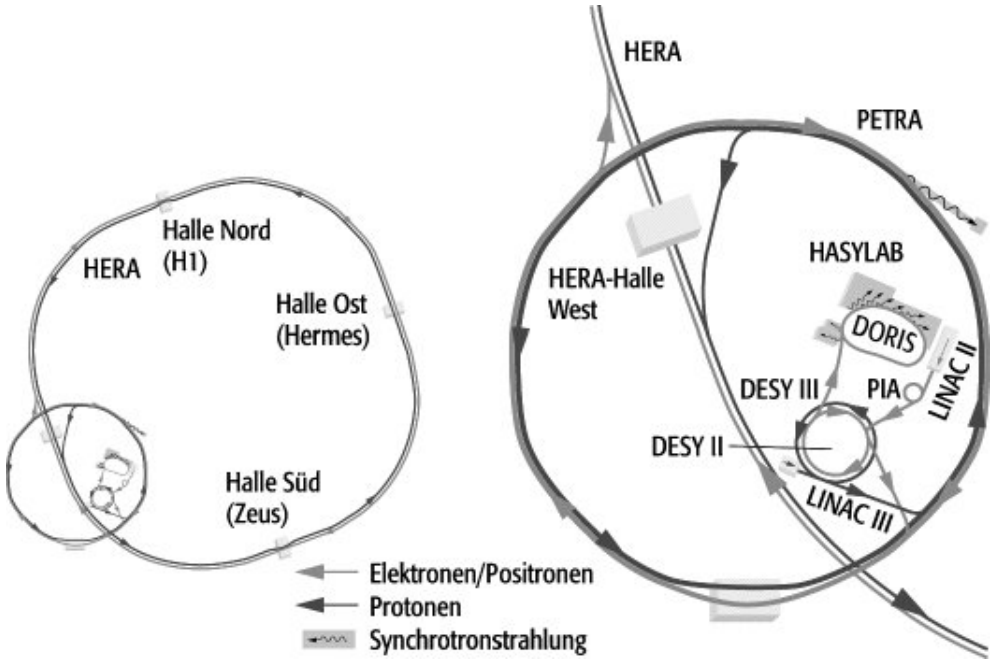

Figure 1.2: Schematic view of DESY accelerators and the experimental stations [6]

Large accelerator facilities are also located outside Europe, playing a key role in global particle physics research. Selected examples include:

- **Fermilab (USA):** Previously operated the Tevatron, a proton–antiproton collider that was the world's most powerful accelerator from 1983 to 2011. Fermilab now leads the Deep Underground Neutrino Experiment (DUNE), which investigates neutrino oscillations by sending an intense beam of muon neutrinos over 1300 km from Illinois to South Dakota. The experiment aims to determine the neutrino mass ordering and explore CP violation in the lepton sector.
- **SLAC National Accelerator Laboratory (USA):** Operates the Linac Coherent Light Source (LCLS), a free-electron X-ray laser used to study ultrafast processes in materials, chemistry and biology. While its primary focus is photon science, SLAC is also involved in particle physics, contributing to dark matter detection projects and LHC experiments. SLAC originally housed the Stanford Linear Collider, an e^+e^- machine active in the 1980s and 1990s.
- **KEK (Japan):** Hosts the SuperKEKB accelerator, where the Belle II experiment studies matter–antimatter asymmetries through e^+e^- collisions. KEK is also developing the International International Linear Collider (ILC), a proposed linear collider that would produce clean e^+e^- interactions for precision measurements of the Higgs boson and potential new physics.

The **ILC** is one of several proposed next-generation accelerator projects. Other major initiatives include the **FCC** (Future Circular Collider), a 100-kilometer tunnel planned at CERN to support both pp and e^+e^- modes, and the **CEPC** (Circular Electron Positron Collider), a Chinese collider dedicated to Higgs boson and electroweak studies. CERN is also working on the **CLIC** (Compact Linear Collider), a high-gradient e^+e^- machine designed for staged operation up to multi-TeV energies. In the United States, the **CCC** (Cool Copper Collider) is another linear e^+e^- concept focused on efficient Higgs production using advanced cooling techniques. Additional concepts include the **EIC** (Electron-Ion Collider) at Brookhaven National Laboratory, which will study the structure of protons and nuclei with polarized electron-ion collisions. Another proposal is the **Muon Collider**, which could enable high-energy collisions with minimal synchrotron radiation losses, offering a compact alternative to traditional circular machines. At CERN, the **LHCee** is being considered as a possible reuse of the LHC tunnel for future e^+e^- collisions after the high-luminosity LHC program ends. Most of these projects are still awaiting formal approval, but a possible timeline for their construction and operation phases is presented in Figure 1.3.

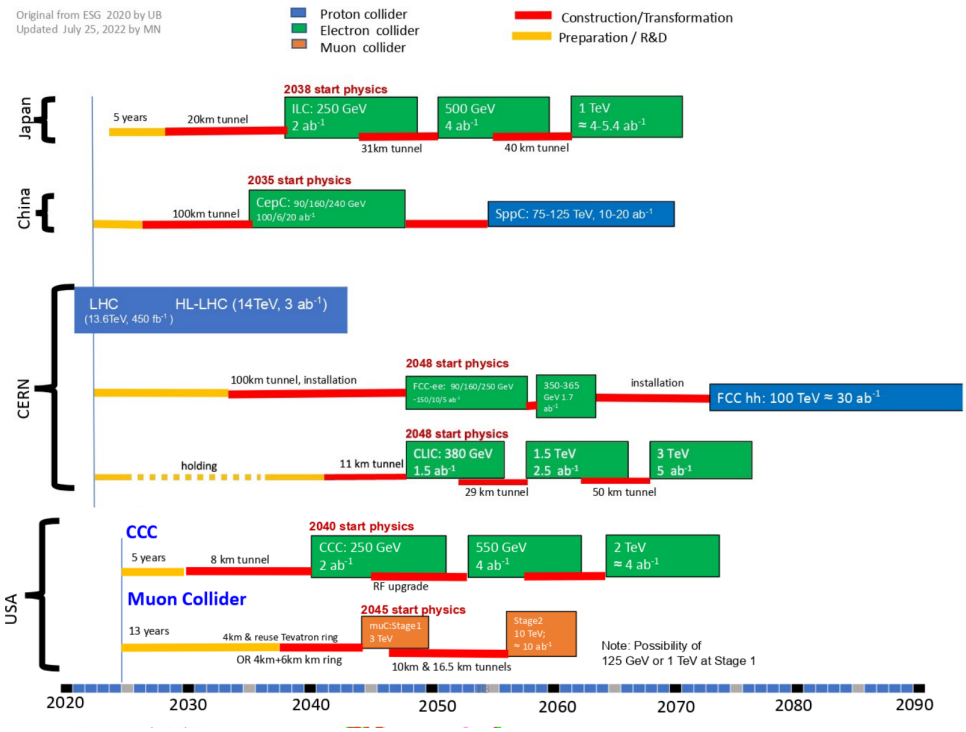

Figure 1.3: Timelines of various future collider projects [7]

1.3 Readout electronics for HEP

In high-energy physics experiments, detectors are designed to measure two key properties of particles: momentum and energy. Specialized tracking detectors, called trackers, reconstruct the trajectories of charged particles. Meanwhile, calorimeters measure energy by absorbing particles and analyzing the depth of their interactions. To precisely handle the extreme data rates generated by thousands of collisions per second, experiments rely on advanced readout electronics. Among these systems, Application-Specific Integrated Circuit (ASIC) is specially designed to meet the strict requirements of particle physics experiments, such as high-speed data processing, low power consumption, and radiation hardness.

A typical readout system in particle physics experiments consists of four main blocks. Firstly, the sensor converts energy depositions into electrical signals. Sensors can be gas-based detectors, semiconductor pixel or strips systems or scintillators. Next, the front-end electronics processes these signals, amplifying and digitizing them using components like charge-sensitive amplifiers, shapers ADC and Time-to-Digital Converter (TDC). Then, the back-end electronics, usually relying on Field Programmable Gate Array (FPGA), selects and processes data before sending it to the Data Acquisition system (DAQ), where it is stored for further analysis.

The precision of data and ability to reflect the true state of particle interactions depend heavily on the performance of the front-end electronics. This stage is responsible for capturing and processing raw signals from the sensors. The front-end electronics system consists of several critical components, as shown in Figure 1.4:

- **Amplifier:** Boosts weak input signals from the sensor to levels suitable for further processing. It is designed to maximize the signal-to-noise ratio (S/N), using low-noise techniques such as charge-sensitive preamplifiers to preserve signal integrity.
- **Shaping Circuit:** Modifies the shape of the amplified signal to optimize it for digitization. It reduces noise bandwidth, suppresses pile-up, and helps match the signal shape to the dynamic range of the ADC. Common implementations use CR-RC filters or more advanced architectures depending on the detector type.
- **Analog-to-Digital Converter (ADC):** Converts the amplitude of analog signal into a digital value. For decades, simple discriminators — 1-bit ADC — have been commonly used, while higher resolution ADCs were typically placed in the back-end due to high power consumption. The choice of ADC architecture as SAR, pipeline or sigma-delta, depends on the trade-off between speed, resolution and power consumption.
- **Digital Signal Processing (DSP) Block:** Handles the digital output from the ADC. It may include baseline correction, common-mode subtraction, zero suppression and formatting of data for transmission to the back-end system.

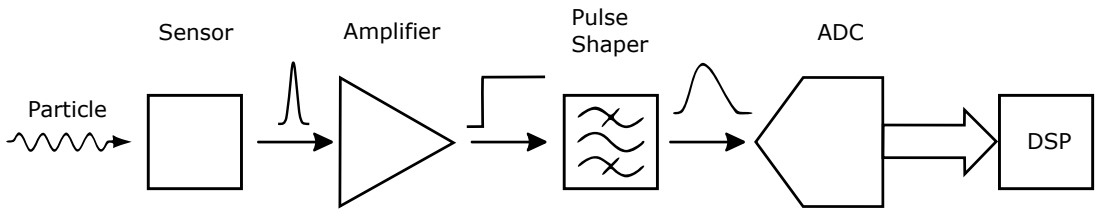

Figure 1.4: Diagram block of a front-end electronics

In high-luminosity environments such as the upgraded LHC, precise time measurement is indispensable to differentiate between particle events. Therefore, in addition to the ADC, a TDC can be integrated into the front-end to measure the time of arrival of the signal below nanosecond or much better precision. A TDC typically operates by converting the time interval between a reference clock and the input pulse into a digital signal. Combining both amplitude and time information allows improved event reconstruction and better separation of closely spaced collisions.

2 Analog-to-Digital Converters

An analog-to-digital converter (ADC) transforms continuous analog signals, such as voltage pulses from particle detectors, into digital values that can be stored and analyzed. This conversion happens in three stages: sampling, quantization, and encoding. Initially, the analog signal is sampled and stored on a capacitor and after the ADC measures the analog signal, the value is rounded to the nearest discrete level based on the ADC's resolution. Finally, it is encoded into a binary number, enabling digital processing. The general schematic diagram of the ADC is illustrated in Figure 2.1.

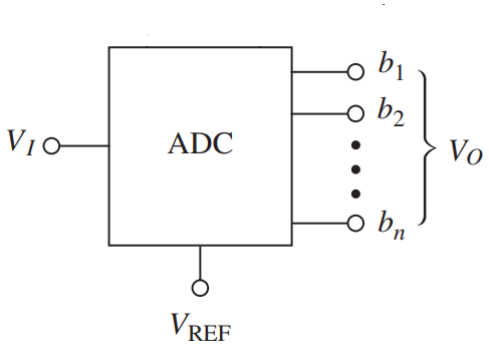

Figure 2.1: Schematic of ADC operation [8]

The ADC's maximum accuracy is determined by the reference voltage (V_{REF}) and the number of bits (N). This accuracy, defined as the Least Significant Bit V_{LSB}, is expressed by the formula:

$$V_{\mathrm{LSB}} = \frac{V_{\mathrm{REF}}}{2^N}. \tag{2.1}$$

Using Equation 2.1, the output signal amplitude can be defined as:

$$V_{\mathrm{O}} = \sum_{i=0}^{N-1} b_i \cdot 2^i \cdot V_{\mathrm{LSB}}, \tag{2.2}$$

where b_i is the binary value of the i-th bit (0 or 1). For example, a 3-bit ADC with $V_{\mathrm{REF}} = 1\,\mathrm{V}$ produces an ideal transfer characteristic with $\pm\frac{1}{2}V_{\mathrm{LSB}}$ errors called quantization noise (e_q), as shown in Figure 2.2.

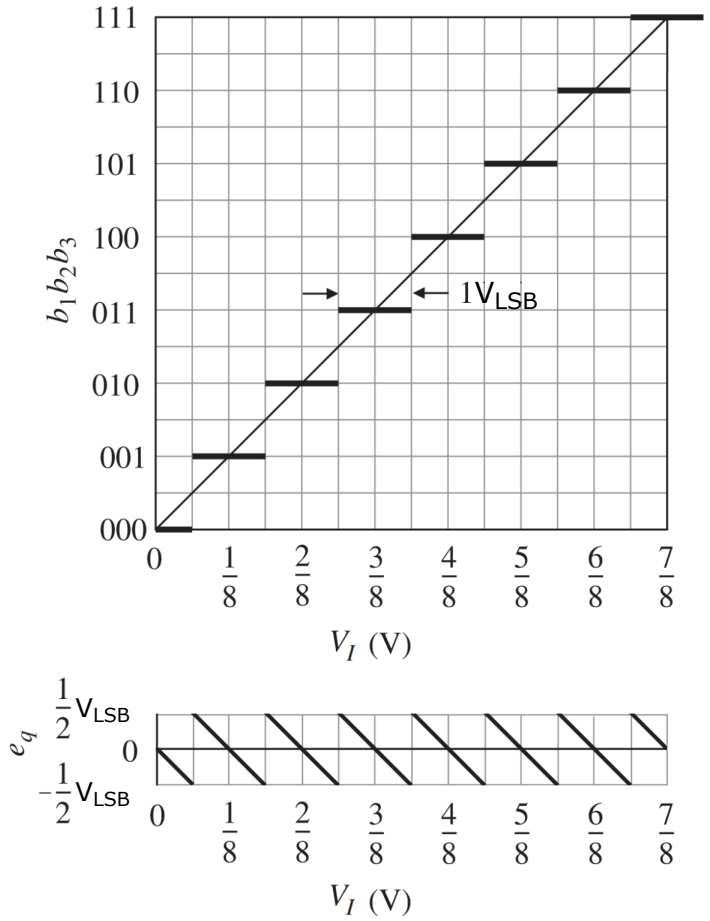

Figure 2.2: ADC's ideal transfer characteristic and quantization noise [8]

2.1 Low power ADC architectures

In low power applications, common ADC architectures include sigma-delta, flash, pipeline, and SAR. Each type differently balances speed, resolution and energy efficiency.

To compare these ADCs designed using different architectures, the Figure of Merit (FOM) is used [9]:

$$\text{FOM} = \frac{\text{Power}}{2^{\text{ENOB}} \cdot f_{\text{sample}}}, \tag{2.3}$$

where Effective Number of Bits (ENOB) describes the ADC's real-world resolution, including noise and distortion. A plot comparing the FOM of existing ADC designs is shown in Figure 2.3.

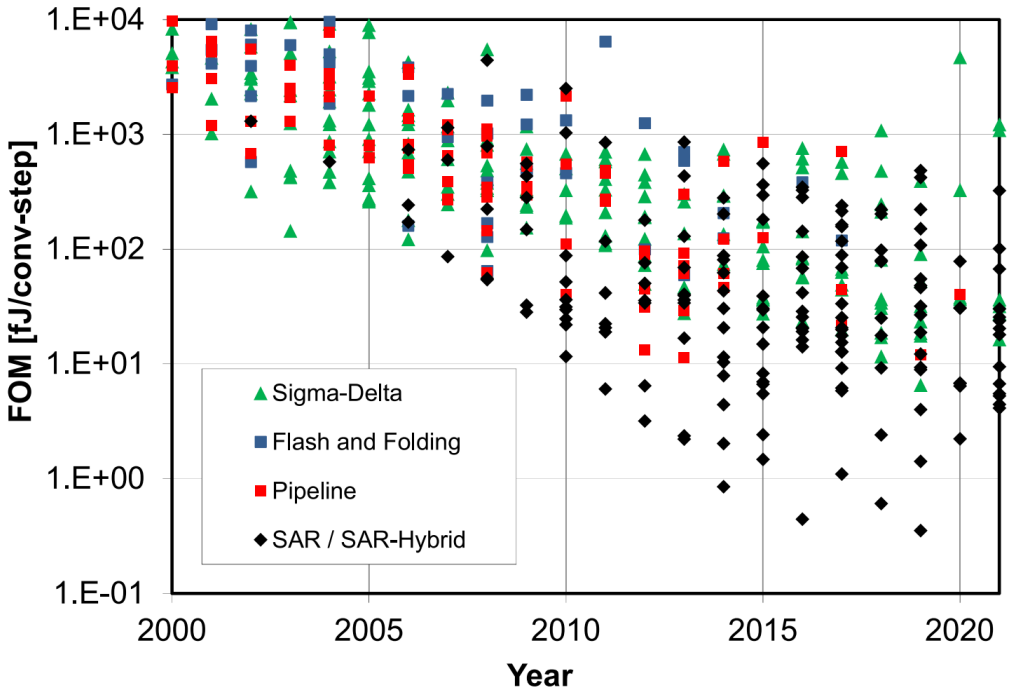

Figure 2.3: ADC energy efficiency over the years [9]

In recent years, ADCs based on SAR architecture have consistently achieved the best FOM values. This trend confirms the dominance of SAR converters in applications requiring extremely low power consumption.

2.1.1 Sigma-Delta

The sigma-delta (Σ-Δ) ADC is a key architecture for high-resolution, low-speed applications like modern voiceband, audio or precision industrial measurement systems. It relies on oversampling and noise shaping to achieve accuracy with simple analog components and digital filtering [10]. A first-order Σ-Δ ADC consists of an integrator, a 1-bit comparator, and a 1-bit Digital-to-Analog Converter (DAC) in a feedback loop. The integrator accumulates the difference between the analog input and the DAC output. The comparator digitizes this result into a bitstream. The DSP block then filters and decimates the bitstream to produce a high-resolution output. The basic structure is shown in Figure 2.4.

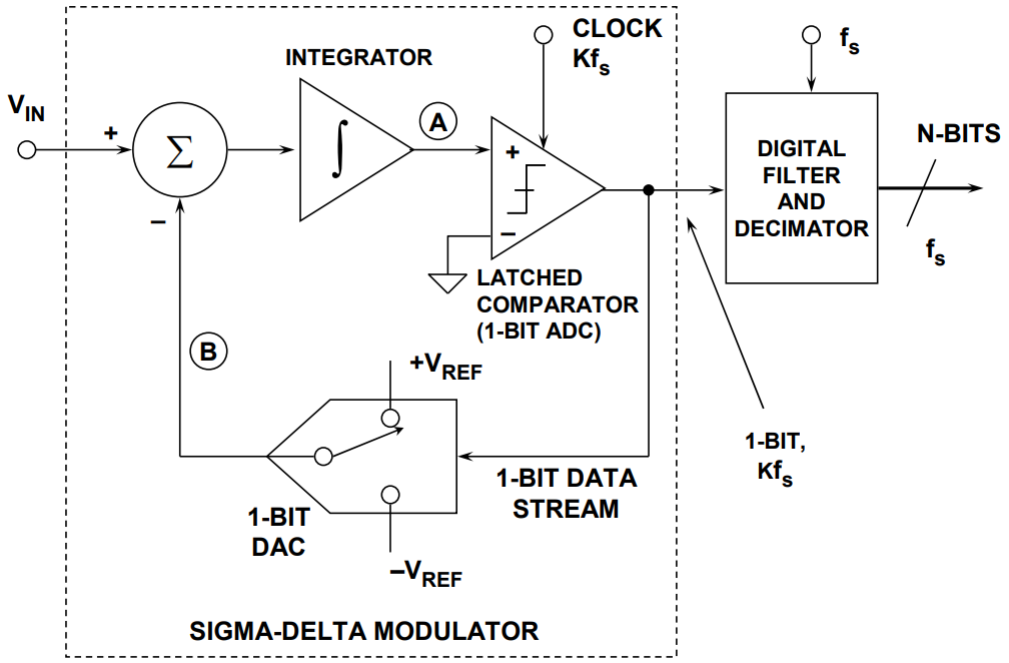

Figure 2.4: Architecture of first order $\Sigma - \Delta$ ADC [10]

The ADC oversamples the input at rates much higher than the Nyquist frequency, pushing most of the quantization noise to higher frequencies. A digital low-pass filter removes this out-of-band noise. Resolution improves with a higher oversampling ratio or by increasing the order of the modulator, which adds more integrator stages and enhances noise shaping. The main limitation is low input bandwidth, which makes this architecture unsuitable for high-speed systems like those used at the LHC.

2.1.2 Flash

A flash ADC is the fastest type of analog-to-digital converter, ideal for high-speed applications like radar or digital communication systems. It uses $2^N - 1$ comparators for N-bit resolution. For example, a 5-bit flash ADC requires 31 comparators. The input signal is compared to reference voltages from a resistor ladder, creating a thermometer code. A decoder converts this code into binary output, as shown in Figure 2.5.

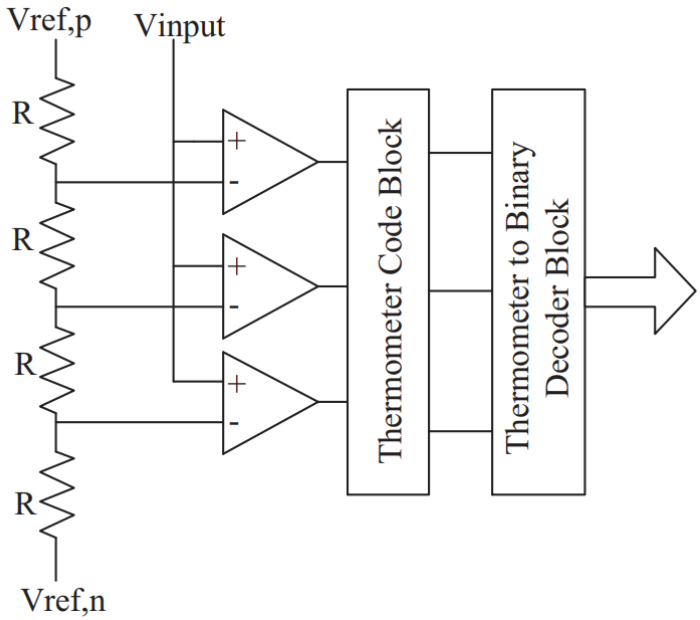

Figure 2.5: General flash ADC architecture [11]

Despite speed, the flash ADC has major drawbacks. Power consumption and circuit area grow exponentially with resolution, making it impractical for large-scale systems like at the LHC, where millions of channels are required. This inefficiency drives the need for other low-power alternatives.

2.1.3 Pipeline

A pipelined ADC splits the conversion into subsequent serial stages. Each stage processes part of the signal while passing the remainder to the next stage. This allows multiple stages working at the same time. Block diagram of this architecture is presented at Figure 2.6.

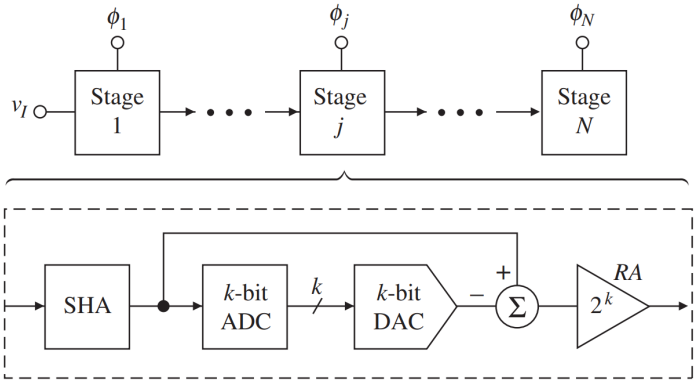

Figure 2.6: Pipelined ADC architecture [8]

Each stage has a sample-and-hold (SHA) to store the input, a ADC to convert a k bits, a DAC to turn those bits back to analog, a subtractor to remove the converted part, and an amplifier to boost the remaining signal. For example, a 10-bit ADC might use five stages, each handling 2 bits. The biggest problem is complexity, each stage requires advanced circuits, which consume significant power. However, in many applications with very high sampling frequencies, they offer the best FOM.

2.1.4 SAR

The SAR ADC is a widely used architecture for medium-to-high-resolution applications, combining simplicity with low power consumption. It operates based on a binary search algorithm, where each bit of the output is determined sequentially, starting from the Most Significant Bit (MSB) and progressing to the Least Significant Bit (LSB), to approximate the input voltage as closely as possible. As shown in Figure 2.7, the main components include a capacitive DAC, a comparator, and a control logic block.

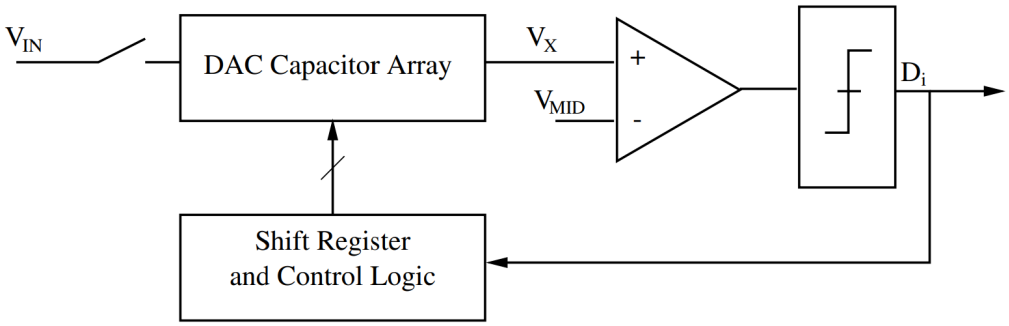

Figure 2.7: SAR ADC architecture [12]

The DAC generates approximation by switching a binary-weighted capacitor array. Starting with the MSB, if the trial voltage exceeds the input, the bit is set to "0"; otherwise, it remains "1". This algorithm is presented in Figure 2.8.

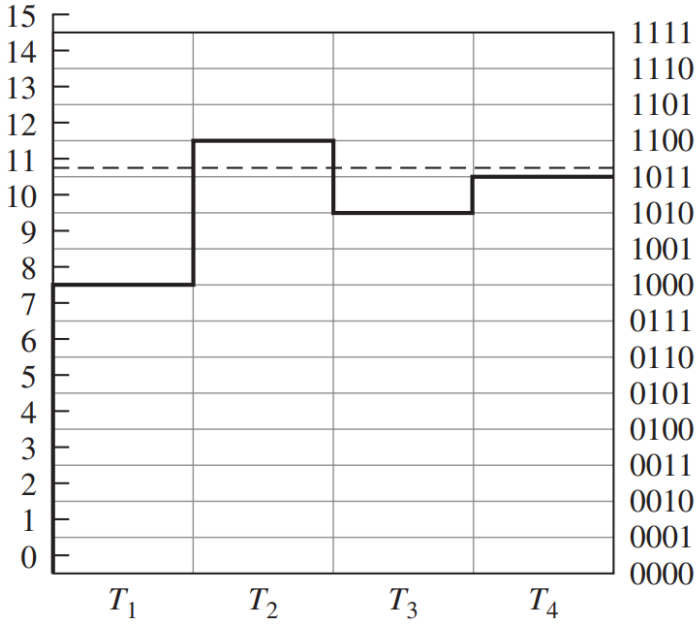

Figure 2.8: Algorithm of a 3-bit SAR ADC [8]

The primary power consumers in a SAR ADC are the comparator, the capacitor array switching and digital logic. Recent advancements, such as splitting the largest capacitor into subarrays or using monotonic switching algorithms, significantly reduce switching energy. For example, the Merged Capacitor Switching (MCS) technique decreases the switching power consumption by up to 87.5% by adding the common-mode voltage in differential designs. The SAR ADC maintains an excellent balance between power consumption and resolution, achieving sufficient speeds for readout systems in particle physics experiments. However, this efficiency is typically achievable only in modern CMOS processes $\leq$130 nm.

2.2 ADC parameters

The performance of a produced ADC is different from ideal behavior due to inherent imperfections in design and manufacturing. Static parameters describe accuracy limitations when converting constant input signals. While certain stiatic errors, such as offset error or gain error, have limited impact on basic functionality, the most critical limitations arise from nonlinearity errors. Dynamic parameters describe the ADC's performance for nonconstant signal, focusing on ability to accurately process input signals changing over time. To fully understand the ADC's suitability for high-energy physics readout systems, it is important to understand both static and dynamic parameters.

2.2.1 Static parameters

Static parameters are measured under constant or very low frequency (DC) input signal conditions to isolate accuracy limitations. The offset error defines a voltage shift across all digital codes in the ADC transfer characteristic. This error, presented in Figure 2.9, originates from mismatches in critical components such as comparator input pairs or reference voltage network. In SAR ADCs, discrepancies in the capacitive DAC directly contribute to this error.

While the offset error shifts the entire transfer characteristic uniformly, the gain error reflects a mismatch in the slope of the ADC transfer function compared to ideal linear approximation. Unlike the offset error, this deviation accumulates across the input range, becoming most significant at the final code transition, as shown in Figure 2.9. This error is caused by mismatches in components such as transistors and capacitors.

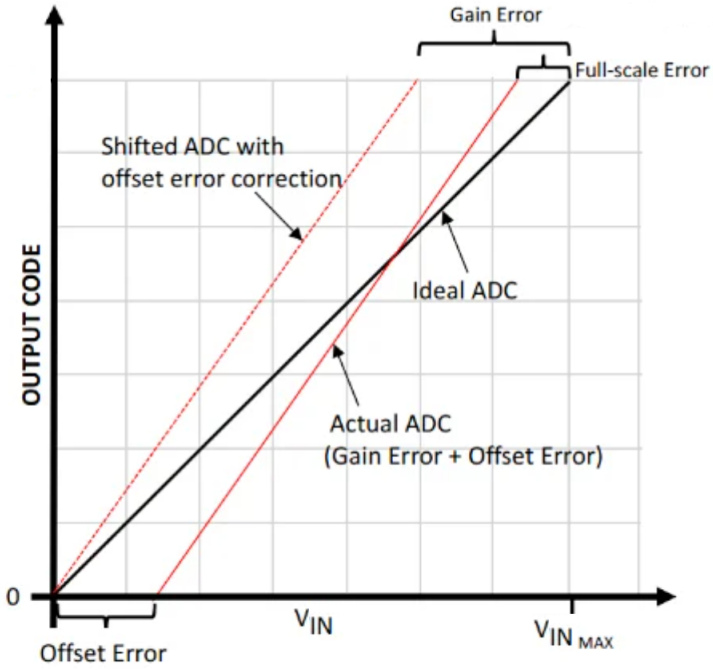

Figure 2.9: Offset and gain error in ADC [15]

Both offset and gain errors can be calibrated out in a foreground or background correction stage, improving DC accuracy before linearity measurements.

The Integral Non-Linearity (INL) is the deviation of the ADC transfer characteristic from an ideal straight line after correcting offset and gain errors. This line is defined by connecting the midpoints of the transfer response. INL measured in LSB units accumulates errors across the input range. In high-energy physics systems, large INL values distort signal amplitudes, leading to inaccuracies in data analysis.

Complementing INL, the Differential Non-Linearity (DNL) measures the deviation of individual code transition widths from the ideal LSB step. This error originates from mismatches in components such as capacitors within the DAC array. Both INL and DNL, presented in Figure 2.10, are static parameters, measured under low-frequency conditions to isolate DC accuracy limitations.

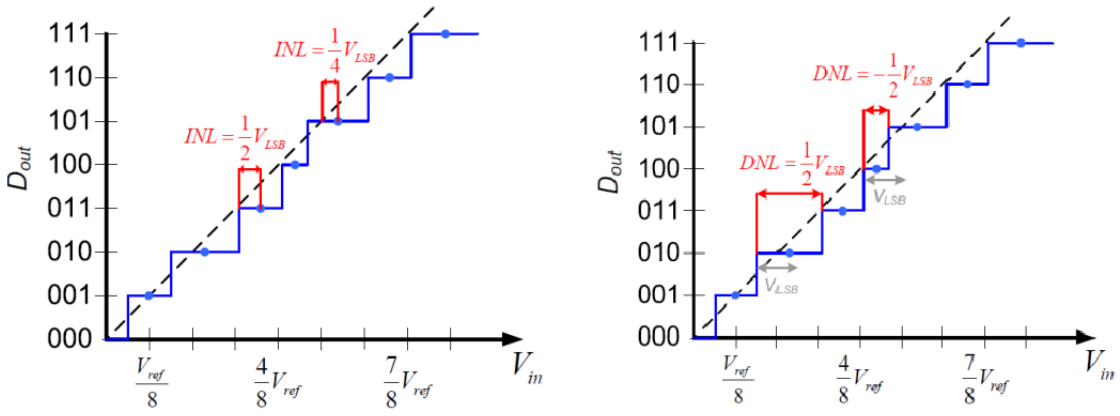

Figure 2.10: INL and DNL errors in ADC [14]

The DNL and INL can be formally described using mathematical expressions. The DNL for code k is defined as:

$$\mathrm{DNL}(k) = \frac{\Delta V(k) - V_{\mathrm{LSB}}}{V_{\mathrm{LSB}}} \tag{2.4}$$

where $\Delta V(k)$ is the actual voltage step between two adjacent code transitions, and V_{LSB} is the ideal step size defined in equation 2.1 or average step from measurements.

The corresponding INL represents the accumulated deviation of the actual transition voltage $V(k)_{\mathrm{actual}}$ from the ideal value $V(k)_{\mathrm{ideal}}$:

$$\mathrm{INL}(k) = \frac{V(k)_{\mathrm{actual}} - V(k)_{\mathrm{ideal}}}{V_{\mathrm{LSB}}} \tag{2.5}$$

Alternatively, the INL can be calculated as the cumulative sum of individual DNL values:

$$\mathrm{INL}(k) = \sum_{i=1}^{k} \mathrm{DNL}(i) \tag{2.6}$$

2.2.2 Dynamic parameters

Dynamic parameters describe the ADC performance under time-varying input conditions. Unlike static metrics, which are measured with DC or slow ramp inputs, dynamic parameters evaluate how accurately the converter processes signals in the frequency domain. To measure dynamic performance, a sinusoidal input signal close to full scale is applied at a frequency within the ADC bandwidth. The resulting output code sequence is analyzed using a Fast Fourier Transform (FFT) [16].

Among dynamic parameters, one of them is the Signal-to-Noise Ratio (SNR) defined as the ratio of signal power to noise power:

$$SNR = 10 \log_{10} \left(\frac{P_{\text{signal}}}{P_{\text{noise}}} \right) \text{ dB}, \tag{2.7}$$

where P_{signal} and P_{noise} are the root-mean-square (RMS) power of the signal and noise. Practical noise sources include thermal noise, clock jitter, and component mismatches. Low SNR limits the detection of weak signals, such as low-energy particle interactions in calorimeters, where noise levels approaching 1/2 LSB can invalidate measurement accuracy.

The Total Harmonic Distortion (THD) quantifies the distortion introduced by the ADC when processing sinusoidal signals. It is defined as the ratio of the total power of harmonic frequencies—integer multiples of the input signal frequency—to the power of the fundamental (original) signal. For example, a 10 kHz input signal may generate harmonics at 20 kHz, 30 kHz, and higher frequencies due to nonlinearities in the ADC circuitry. The THD is calculated as:

$$THD = 10 \log_{10} \left(\frac{\sum P_{\text{distortion}}}{P_{\text{signal}}} \right) \text{ dB}, \tag{2.8}$$

where $\sum P_{\text{distortion}}$ is the combined power of all harmonic components.

To present noise and distortion effects, the Signal-to-Noise-and-Distortion Ratio (SNDR) combines both into a single metric:

$$SNDR = 10 \log_{10} \left(\frac{P_{\text{signal}}}{P_{\text{noise}} + P_{\text{distortion}}} \right) \text{ dB}. \tag{2.9}$$

The Spurious-Free Dynamic Range (SFDR) defines the ratio of the fundamental signal amplitude to the largest spurious component in the frequency domain:

$$SFDR = 10 \log_{10} \left(\frac{P_{\text{signal}}}{P_{\text{spur}}} \right) \text{ dB}. \tag{2.10}$$

Spurious tones, caused by clock feedthrough or substrate coupling, obscure valid data in multi-channel readout systems. Figure 2.11 shows the amplitude spectrum of an ADC output for a single-tone sinusoidal input. Each vertical line represents the amplitude of a frequency component in the output spectrum. The signal of interest corresponds to the fundamental frequency, while smaller spurious components appear at other frequencies due to nonlinearities and interference. The SFDR is defined as the amplitude ratio of the main signal to the largest spur in the frequency spectrum.

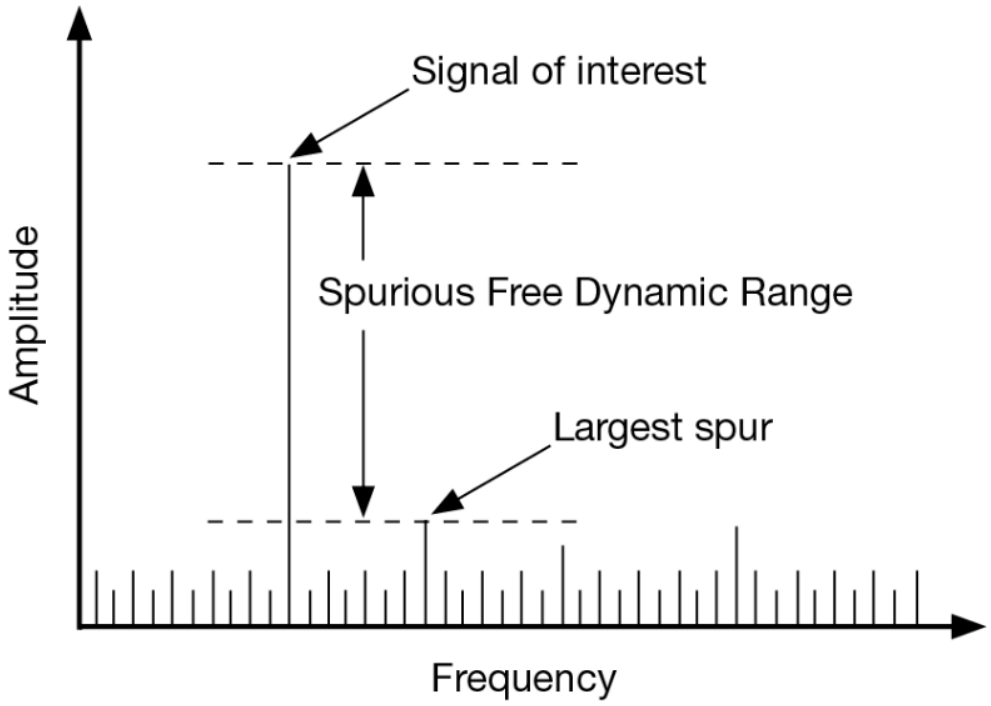

Figure 2.11: Illustration of SFDR [18]

2.2.3 Effective Number of Bits

The ENOB describes the actual resolution of an ADC under real operating conditions, as noise, distortion, and nonlinearities. It is derived from the SNDR and reflects how many bits an ideal ADC would need to match the measured performance. The relationship originates from the theoretical SNR of an ideal N-bit ADC: $SNR_{\text{ideal}} = 6.02N + 1.76$. By replacing SNR_{ideal} with the measured SNDR, the ENOB is calculated as [16]:

$$ENOB = \frac{SNDR - 1.76}{6.02}. \tag{2.11}$$

For example, in a SAR ADC capacitor mismatch in the DAC array or comparator metastability can degrade the SNDR, directly reducing the ENOB. This degradation limits the system's ability to resolve small signal variations.

An alternative method to determine ENOB is to fit a sine wave to the measured output data and comparing it to the input waveform. The root-mean-square error E_{rms} of this fit measures the deviation caused by ADC nonlinearity. The ENOB can be express as [16]:

$$ENOB = N - \log_2\left(\frac{E_{\text{rms}}}{LSB/\sqrt{12}}\right). \tag{2.12}$$

This method focuses on errors specific to the converter, such as nonlinearities or timing jitter, by ensuring the input and output frequencies match while optimizing amplitude, offset, and phase.

3 Design of 10-bit SAR ADC

In this chapter, the design of an ultra-low power, fast 10-bit SAR ADC in CMOS 130 nm technology is presented. This ADC is an extension of an experimentally verified 10-bit SAR ADC (INL, DNL < 0.5 LSB, ENOB > 9.5), working up to 50 MSps and consuming 680 μW at 40 MSps [2]. The goal of the present work was to add a programmable threshold for the processed input signal, to stop the conversion and thus greatly reduce power consumption in case the signal is below the threshold.

3.1 ADC Architecture

To achieve low power consumption, the SAR architecture was selected for this design. The ADC is implemented as a fully differential structure and includes bootstrapped input switches [25], a differential capacitive DAC with the MCS switching scheme [27], a dynamic comparator [28] and asynchronous dynamic control logic. Since all these components are active only during the conversion phase, static power dissipation is fully avoided. To further reduce input capacitance and dynamic power, a split-capacitor DAC configuration was adopted, as shown in Figure 3.1. The segmentation follows a 6-1C-3 structure, with a 6-bit sub-DAC for the most significant bits, a unit split capacitor, and a 3-bit sub-DAC for the least significant bits. This arrangement enables the lowest achievable total capacitance within the limits of the selected CMOS technology. Compared to the earlier ADC design [2], the only modification lies in the SAR control logic, where a programmable threshold was introduced, as illustrated in Figure 3.1. The total layout area remains unchanged at 560μm $\times$ 80μm.

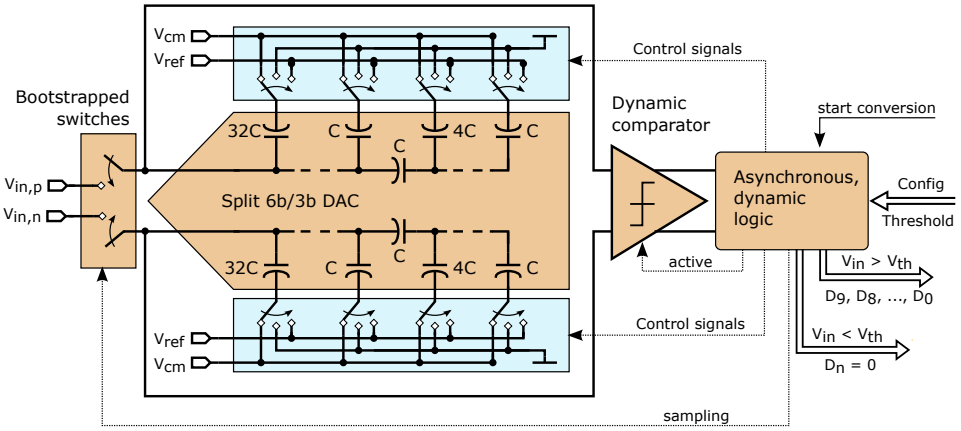

Figure 3.1: Block diagram of 10-bit SAR ADC [1]

The bootstrapped switches sample the input voltage with minimal distortion. This is achieved by constant switch overdrive voltage, which is critical to maintaining linearity throughout the input range. Then, the comparator evaluates comparing the voltage between the sampled input and the approximation DAC, triggering the digital control logic to update the DAC. This iterative process continues until the resolution of LSB is reached.

3.2 Switching Algorithm

Among various capacitive switching schemes developed to reduce power consumption, the MCS algorithm was selected for this design. The MCS technique minimizes the energy required to charge and discharge the DAC capacitor array by reducing unnecessary voltage transitions. Compared to the conventional SAR switching scheme, where energy consumption is highly asymmetric between opposite transitions, the MCS algorithm balances the switching path and eliminates redundant steps. As demonstrated in Figure 3.2, this technique reduces average power consumption by 93.4% [19] compared to traditional approaches, making it particularly suitable for low-power applications in high-energy physics experiments.

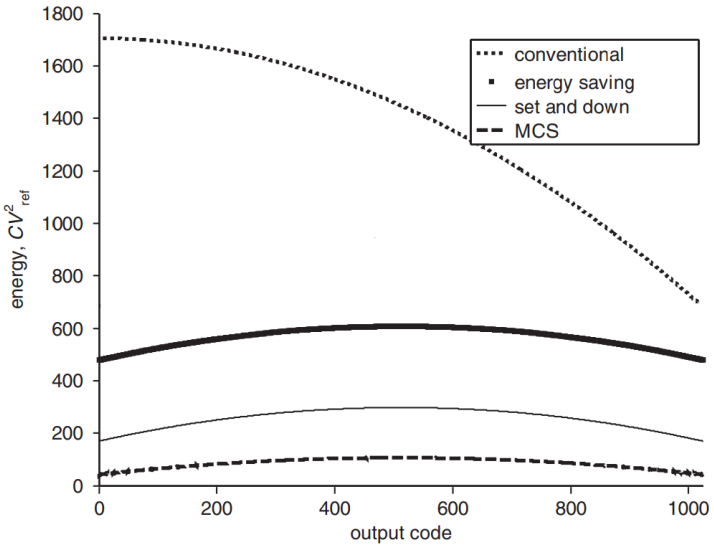

Figure 3.2: Switching energy comparison [19]

In the MCS scheme, only an $(N-1)$ bit DAC is required for an N bit SAR ADC, since the most significant bit (MSB) is resolved without any switching activity. The DAC array is initially pre-charged to the common-mode voltage $V_{CM} = V_{DD}/2$, and the differential input signal is sampled onto the top plates of the capacitors. The detailed switching sequence for a 3-bit SAR ADC using MCS is shown in Figure 3.3.

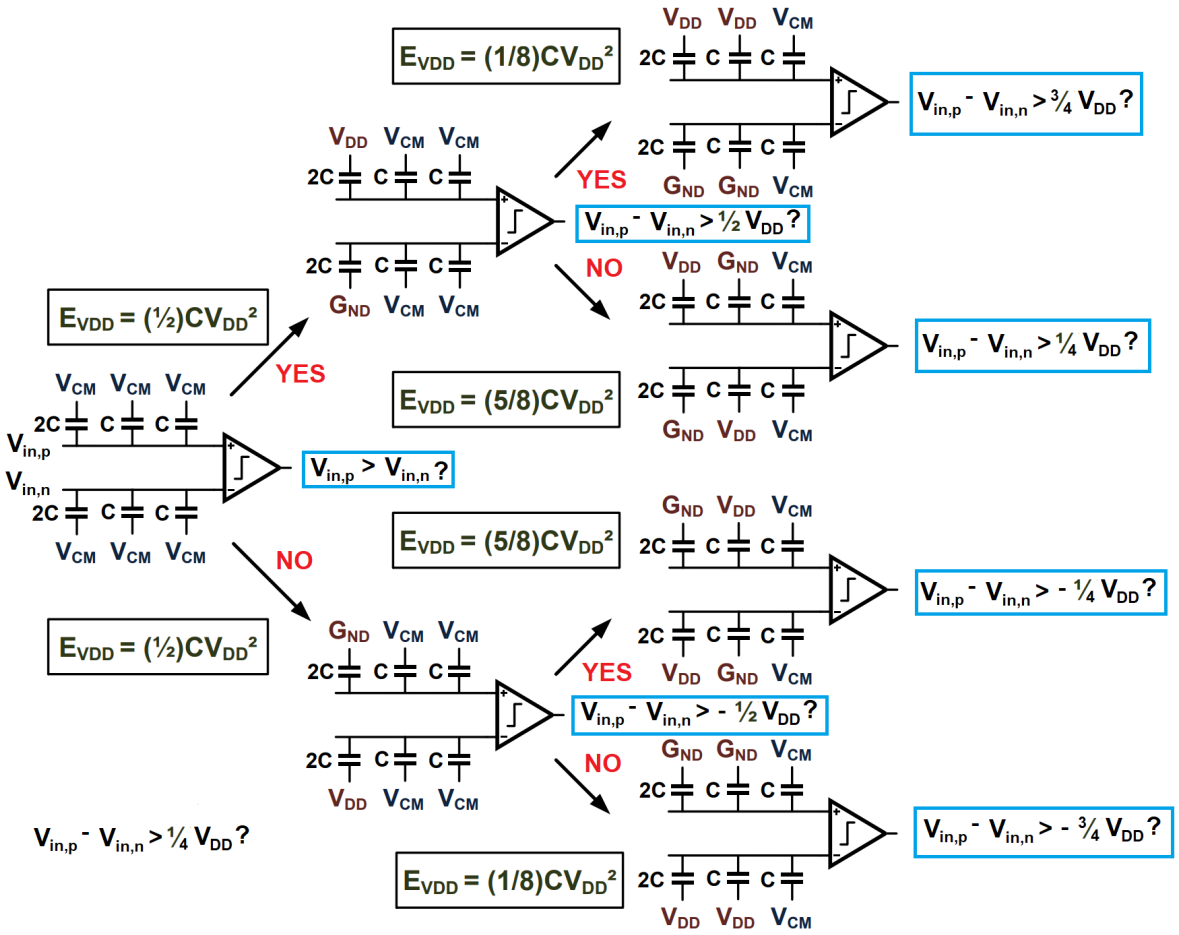

Figure 3.3: MCS ADC SAR switching diagram [13]

The comparator determines the polarity of the input and this first decision is stored directly in the SAR register. Subsequent conversion steps selectively switch capacitor bottom plates between V_{DD} and ground, based on the comparator result, to add or subtract differential voltage. Each cycle adjusts the DAC output by a binary-weighted step, starting from the second bit. This switching method minimizes power consumption by centering capacitor transitions around V_{CM} and eliminating unnecessary switching for the MSB.

The average switching energy of a capacitive DAC array directly impacts the power efficiency of a SAR ADC. In a conventional N-bit switching scheme, capacitors are repeatedly charged and discharged between V_{REF} and ground, resulting in a high total energy consumption. The average energy can be approximated by [19]:

$$E_{\mathrm{avg,conv}} = \sum_{i=1}^{N} 2^{N+1-2i} \times (2^i - 1) C V_{\mathrm{DD}}^2, \tag{3.1}$$

where C is the unit capacitance and V_{DD} is the reference voltage.

In contrast, the MCS algorithm improves energy efficiency by minimizing unnecessary transitions in the capacitor array. The average energy for the MCS scheme is given by [19]:

$$E_{\text{avg,mcs}} = \sum_{i=1}^{N-1} 2^{N-3-2i} \times (2^i - 1) C V_{\text{DD}}^2. \tag{3.2}$$

3.3 Segmentation of DAC

The split-capacitor architecture is commonly used when minimum sized capacitors with good matching properties are not available. Instead of using very small unit capacitors, which may exhibit poor matching, larger capacitors are used in combination with a split structure. This approach allows achieving a smaller effective capacitance while preserving the binarity and accuracy required for high-resolution operation. The capacitor array is divided into two sections: an MSB array (M bits) and an LSB array (L bits), connected through an split capacitor C_a, as shown for the single-ended version in Figure 3.4. For an N bit DAC, the resolution is partitioned such that

$$N = L + M, \tag{3.3}$$

where L and M represent the number of bits assigned to the LSB and MSB arrays, respectively.

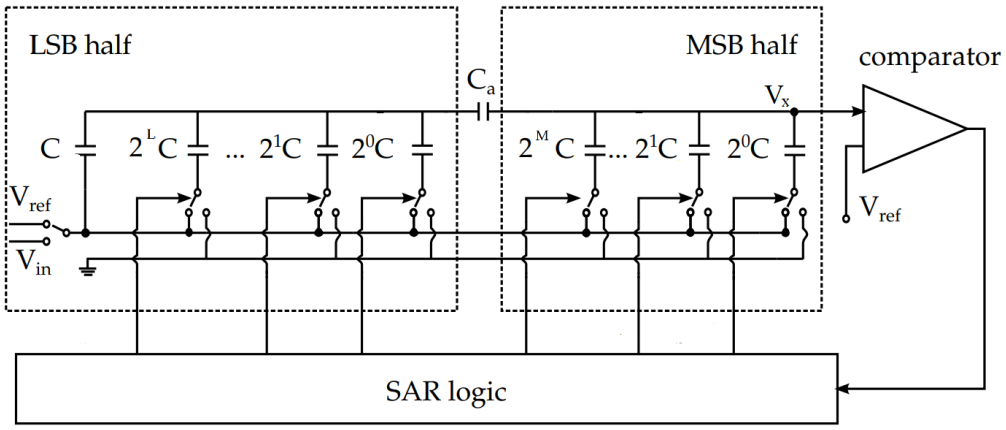

Figure 3.4: Split capacitor array DAC [20]

To ensure binary charge redistribution between the MSB and LSB arrays, the value of the split capacitor C_a must be correctly selected. When only the i-th capacitor from the MSB array is connected to V_{REF}, the voltage at the internal node $V_{x(M_i)}$ is given by:

$$V_{x(M_i)} = \frac{V_{\mathrm{REF}}}{\sum C_M + \left(\frac{C_a \cdot \sum C_L}{C_a + \sum C_L}\right)} \cdot C_{M_i}, \tag{3.4}$$

where $\sum C_M$ is the total capacitance of the MSB array and C_{M_i} is the i-th capacitor in the MSB array.

Similarly, when only the i-th capacitor from the LSB array is connected to V_{REF}, the voltage at the internal node $V_{x(L_i)}$ is:

$$V_{x(L_i)} = \frac{V_{\mathrm{REF}}}{\sum C_M + \left(\frac{C_a \cdot \sum C_L}{C_a + \sum C_L}\right)} \cdot C_{L_i} \cdot \frac{C_a}{C_a + \sum C_L}, \tag{3.5}$$

where $\sum C_M$ is the total capacitance of the MSB array and C_{L_i} is the i-th capacitor in the LSB array.

For a 10-bit ADC with $M = 6$ and $L = 3$, and assuming the LSB array is composed of $C_{L_i} \in \{C, 2C, 4C\}$, the total LSB capacitance is $\sum C_L = 7C$. To maintain binarity between both sub-arrays, the voltage contributions should follow:

$$\frac{V_{x(L_2)}}{V_{x(M_0)}} = \frac{1}{2}. \tag{3.6}$$

Solving this relationship yields:

$$\frac{C_a}{C_a + \sum C_L} = \frac{1}{8}, \tag{3.7}$$

which implies:

$$C_a = C, \tag{3.8}$$

The new design is based on an existing split-capacitor architecture that demonstrated optimal performance with a 6-1C-3 configuration presented in Figure 3.5. This partitioning splits the array into six MSB capacitors and three LSB capacitors, achieving good matching accuracy with the unit capacitance equal $C = 26.2$ fF implemented as high-precision Metal-Insulator-Metal (MIM) capacitor.

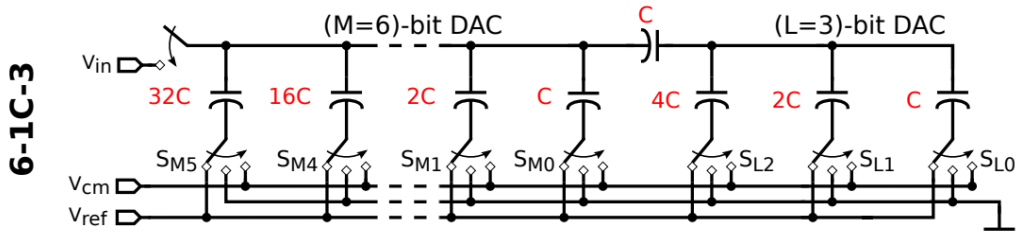

Figure 3.5: Used 6-1C-3 DAC segmentation [2]

3.4 Bootstrap switch

In particle physics applications, precise signal storage with sampling capacitors is crucial. Detector readout systems often process fast, low-amplitude pulses, where even minor sampling errors distort energy measurements.

Conventional MOS sampling switch shown in Figure 3.6 offers simplicity but exhibit significant limitations due to nonlinear on-resistance and charge injection errors that compromise accuracy. The main advantage is high operating speed and simplicity.

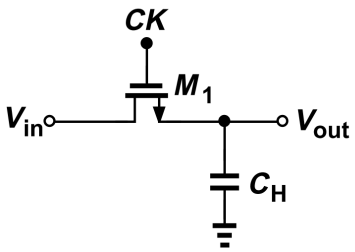

Figure 3.6: Schematic diagram of the switch [29]

A basic MOS sampling switch utilizes an NMOS transistor (M1) controlled by the clock signal CK. When CK drives the gate voltage V_G above the threshold V_{T}, the transistor enters the triode region with almost zero drain-source voltage ($V_{\mathrm{DS}} \approx 0$), acting as a low resistance path between input (V_{in}) and the hold capacitor C_H. One of the main limitations of this structure is the dependency of the overdrive voltage ($V_{\mathrm{DD}} - V_{\mathrm{in}} - V_{\mathrm{T}}$) on the input signal, which causes significant variation in the switch resistance across the input range.

The channel charge Q_{CH} stored during conduction is given by:

$$Q_{\mathrm{CH}} = W_1 L_1 C_{\mathrm{ox}}(V_{\mathrm{DD}} - V_{\mathrm{in}} - V_{\mathrm{T}}), \tag{3.9}$$

where W_1/L_1 are the transistor dimensions, C_{ox} is the gate oxide capacitance per unit area, and V_{DD} is the supply voltage. This charge injection becomes critical during switch turn-off, as Q_{CH} partially transfers to C_H, introducing nonlinear errors proportional to V_{in}.

For these reasons, a key feature of the bootstrap switch shown in Figure 3.7 is to make resistance independent of the amplitude of the input signal, by maintaining a constant V_{GS} in transistor M_S. This is achieved by maintaining a constant voltage on the capacitance C, approximately equal to the supply voltage. A more detailed description of the scheme can be found in the literature [28].

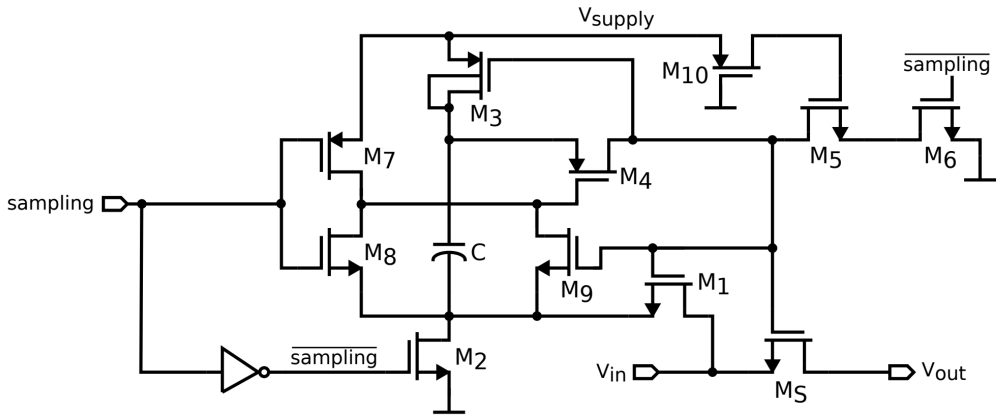

Figure 3.7: Schematic diagram of the bootstrap switch [28]

3.5 Dynamic Comparator

A voltage comparator is one of key components in ADC's analog part, functioning as a one-bit analog-to-digital converter. Its primary role is to compare two input voltages (v_P and v_N) and generate a binary output:

$$v_O = \begin{cases} V_{\text{OH}} & \text{if } v_P - v_N > 0 \\ V_{\text{OL}} & \text{if } v_P - v_N < 0 \end{cases},$$

where V_{OH} and V_{OL} represent the high and low output logic levels. The comparator's behavior is governed by differential input voltage $v_D = v_P - v_N$, producing a steep voltage transfer curve (VTC) with very high gain in the transition region as presented in Figure 3.8.

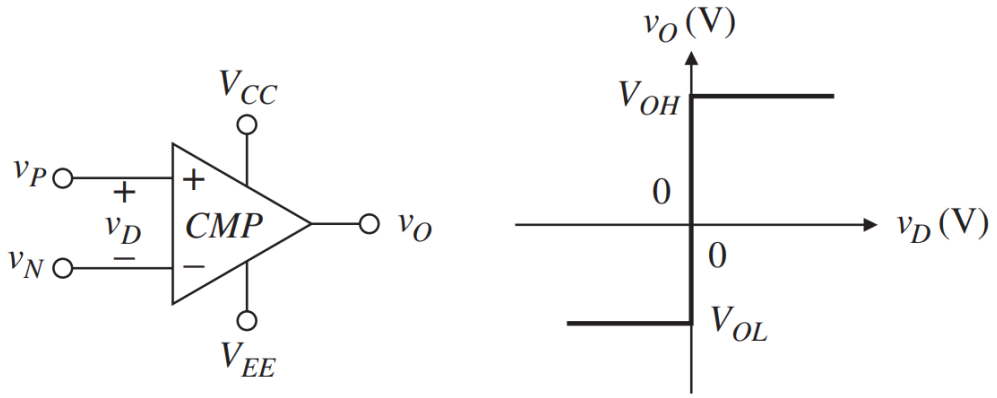

Figure 3.8: Comparator symbol and ideal VTC [8]

To eliminate static power consumption, the dynamic latched comparator, was used. The implemented circuit, shown in Figure 3.9, consists of two gain stages followed by an output latch. This architecture achieves fast decision times, while maintaining ultra-low power consumption. More details can be found in the literature [26].

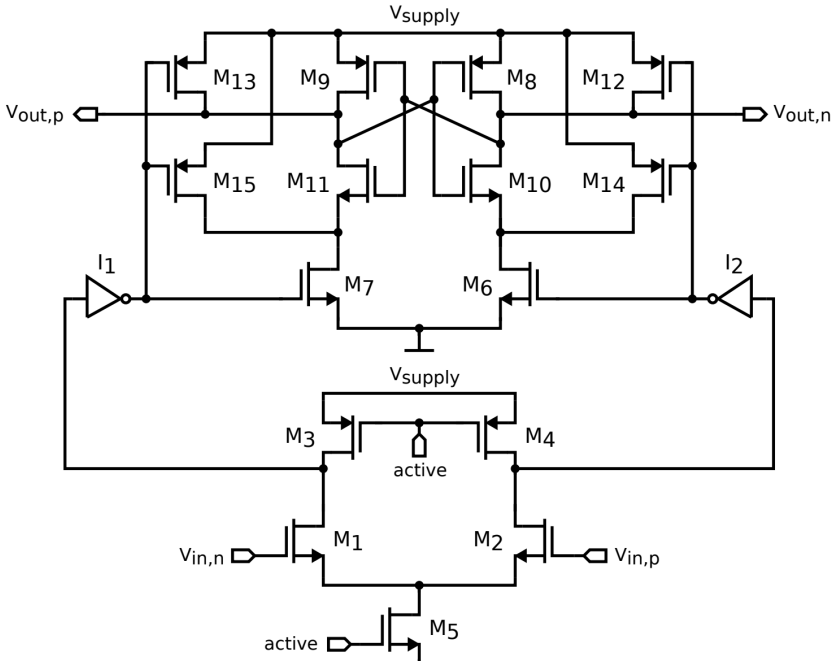

Figure 3.9: Schematic diagram of the dynamic comparator [26]

The comparator's accuracy is limited by random offset voltages coming from threshold voltage (V_{TH}) mismatches and load capacitance imbalances. These offsets propagate through three stages: differential input pair, inverter amplification stage and output latch.

3.6 Control logic

Figure 3.10 illustrates the control logic responsible for managing the bit conversion sequence. Apart from the analog part, the digital control logic plays an equally important role in ensuring proper operation of the ADC. To minimize power consumption, which is critical in multi-channel systems, the control logic, in this design, is implemented asynchronously and relies heavily on dynamic flip-flops and activates only during the conversion process.

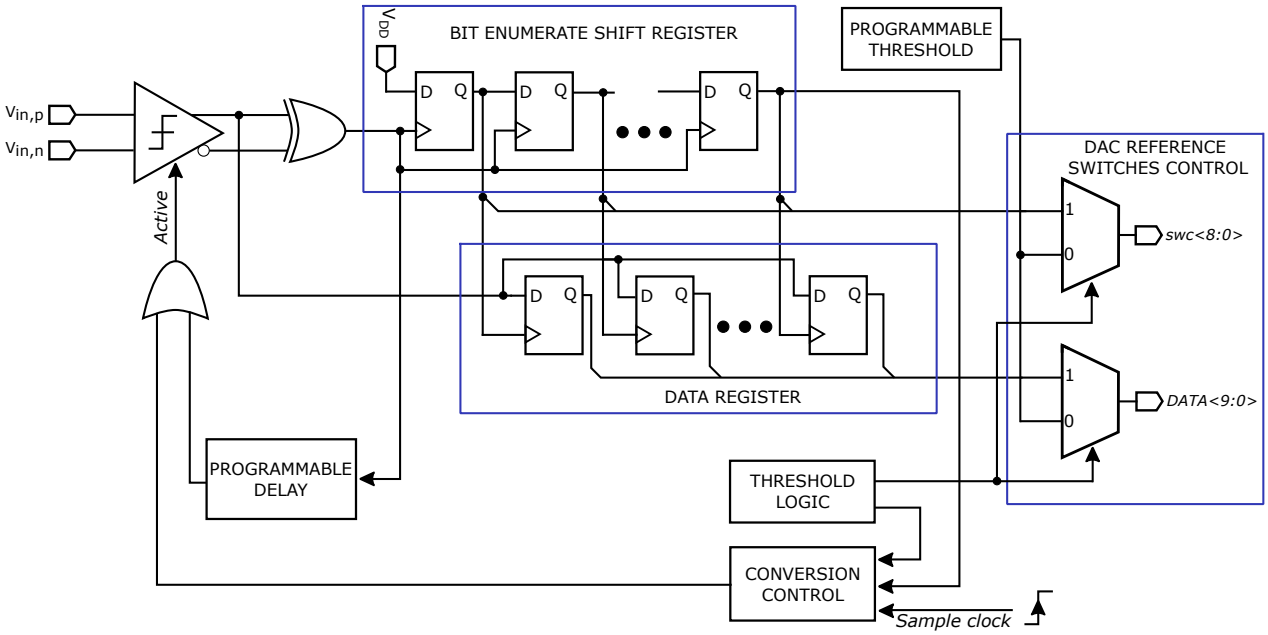

Figure 3.10: Schematic diagram of digital control logic

After the input signal is sampled, the comparator is triggered through the *Active* signal by the rising edge of the sampling clock. Since the comparator takes some time to take a decision after triggering, a XOR gate at its output has been added to detect when a valid decision has been performed. This triggers the Shift Register which enumerates the bit being currently processed. In parallel, the comparison result is provided to the Data Register, where it is stored in flip-flop respective to the currently processed bit. Next, the control logic updates the configuration of the DAC switches through swc<9:0> signals, and the Data Register determines the bit value of MSB. After a short delay, provided by the Programmable Delay block, required for the DAC output to settle, the comparator is triggered again to determine the next bit. In a conventional 10-bit design, this procedure is repeated ten times. Once the LSB bit is resolved, an end-of-conversion signal is sent to the Conversion Control block, which resets all flip-flops and waits for the next rising edge of the clock.

In the proposed ADC with a programmable threshold, an additional control logic block, called Threshold Logic, is introduced to configure the DAC switches in such a way that allows comparison with the threshold voltage.

3.6.1 Threshold implementation

The conversion process with the threshold is shown in Figure 3.11, where differential signals at the comparator input and the ADC output are plotted for signals above (left) and below (right) the threshold. One additional comparison step is inserted after the MSB is resolved, using a user-defined threshold value with 8-bit resolution. This ensures that the comparator is not exposed to input levels that might exceed oxide breakdown voltage. The threshold is then applied to the DAC by appropriately switching the reference voltages of the less significant bits. If the threshold voltage V_{th} is higher than the remaining signal and MSB=0, the conversion is ended early and all remaining bits are set to 0. If V_{th} is lower, the threshold is removed and the conversion proceeds as normal, and the second most significant bit is determined. When MSB=1, the condition $V_{in} > V_{th}$ is always fulfilled by definition, so the conversion of the remaining bits (D[8]–D[0]) is always processed.

The threshold comparison can be disabled, allowing the ADC to behave identically as the existing ADC [2] without this feature.

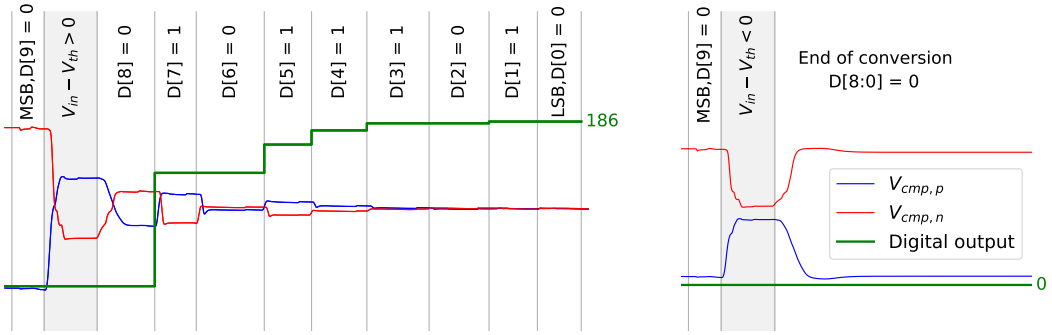

Figure 3.11: Example of ADC transient simulation for a signal higher (left) and lower (right) than the threshold. Signals $V_{cmp,p}$, $V_{cmp,n}$ are inputs to the comparator, while *Digital output* is the result of the ADC conversion. A grey background indicates the additional comparison cycle with the threshold

3.6.2 Programmable delay

The maximum conversion rate is achieved by precisely controlling the delay before each comparator activation. A 4-bit Programmable Delay block with about 175 ps resolution was implemented for this purpose. The delay grouping differs depending on whether the user-defined threshold is enabled or disabled as presented in Figure 3.12.

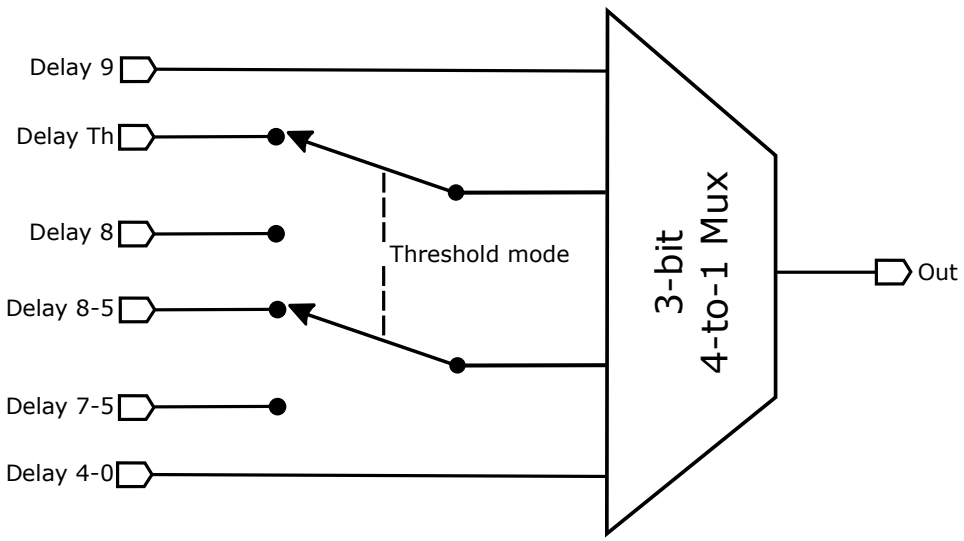

Figure 3.12: Diagram of the delay block with enabled threshold

When the threshold is disabled, the ADC uses four delay groups: the first two registers control delays for the MSB and subsequent bit, the third handles bits 7-5, while the last, often with shortest delay, is for bits 4-0.

With the threshold enabled, the grouping changes to prioritize threshold comparison cycle. The second register controls the delay for threshold cycle, which requires larger delay due to the simultaneous switching of multiple capacitors accompanied by large voltage transitions. The third register then controls delay for bits 8-5, while maintaining the same fast timing for bits 4-0 is done through the fourth register.

3.6.3 Threshold Logic

To integrate threshold comparison, additional logic was implemented. An extra cycle is inserted when the programmable threshold is enabled; otherwise, the standard conversion sequence executes. This functionality is governed by a two-input multiplexer, that selects between threshold or direct conversion mode. The structure and truth table of multiplexer are detailed in Figure 3.13.

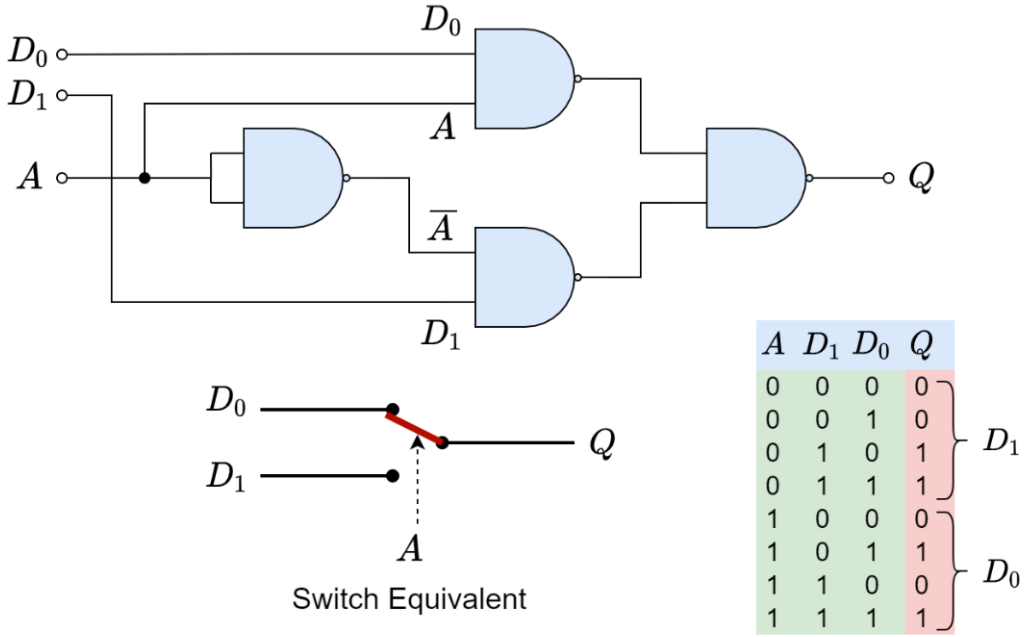

Figure 3.13: The 2-to-1 Multiplexer along with Truth Table and Switch Equivalent [30]

The operation of the 2-to-1 multiplexer is defined by the Boolean equation:

$$Q = (D_0 \wedge A) \vee (D_1 \wedge \neg A), \tag{3.10}$$

where D_0 and D_1 are the input signals, A is the selector input and Q is the output signal. When $A = 0$, the output Q selects input D_1, while $A = 1$ input D_0.

In the proposed ADC, the multiplexer is also implemented in the DAC Reference Switches Control block, which is responsible for modifying capacitor switching based on the user-defined threshold value. When $A = 0$, the DAC reference voltages are reconfigured to represent the value provided externally by the user as a programmable threshold (D_1). When $A = 1$, the reference voltages are controled by the conversion process according to the standard SAR algorithm (D_0).

The decision to switch between these two modes is handled by static CMOS logic based on standard logic gates, as shown in Figure 3.14. In addition to the user input enabling threshold mode, the logic checks that the most significant bit $MSB = 0$, for which the DATA<9> and swc<8> signals are responsible. This conditional activation prevents unnecessary switching and ensures proper sequencing of the conversion process for other bits through swc<7:0>.

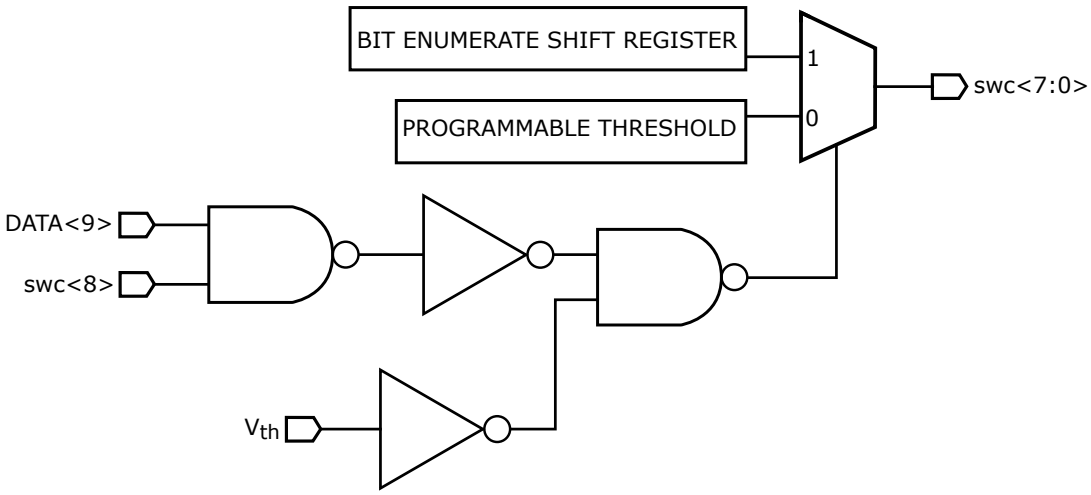

Figure 3.14: Diagram of threshold logic

In future work, the author plans to replace this static logic with a dynamic implementation to evaluate potential improvements in ADC speed and power efficiency. This modification could further optimize performance for high-channel-count particle detector systems.

3.7 Layout Implementation

The physical design of the ADC was implemented in Cadence Virtuoso. The layout prioritizes compactness for integration into multi-channel readout ASIC, with a fixed pitch of 80µm per channel. The final dimensions of the ADC measure 560µm × 80µm and its layout is shown in Figure 3.15.

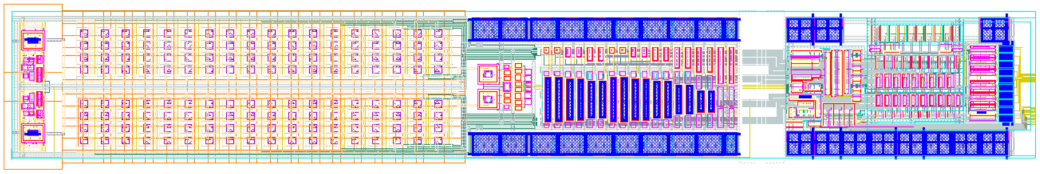

Figure 3.15: Layout of the ADC [2]

The ADC layout arranges blocks from left to right: bootstrapped sampling switches, capacitive DAC arrays, the dynamic comparator, reference voltage switches for DAC bit transitions and digital control logic with threshold. The DAC dominates the layout, occupying around 50% of the total area. A substantial portion of this space is dedicated to the DAC reference voltage switches and their driver circuits. These drivers ensure rapid charging of capacitor nodes, critical for maintaining high sampling rates. However, their operation contributes significantly to the ADC's overall power consumption, creating a direct trade-off between speed and energy efficiency.

The project underwent iterative verification, starting with schematic-level simulations and proceeding to post-layout extraction with parasitic capacitances and resistances. Design Rule Checking (DRC) and Layout Versus Schematic (LVS) verification were performed using Cadence Assura, the same toolchain used for the previous ADC. This consistency ensures accurate parasitic extraction and reliable correlation between post-layout simulations and silicon measurements, as validated in the prior design.

Apart from DRC and LVS verification, corners simulations are also important part of ADC's verification. Design corners are transistor models, which represent the extreme combinations of process variations and environmental conditions under which integrated circuits must operate reliably. These variations encompass transistor speed (nMOS and pMOS), supply voltage and temperature. For CMOS technologies, these corners form an interdependent envelope rather than discrete points, as parameters like oxide thickness often track coherently across devices. The term corner refers to an imaginary field that surrounds the typical performance of the circuits, as shown in the Figure 3.16. Where the letters F, T, and S, stand for fast, typical and slow.

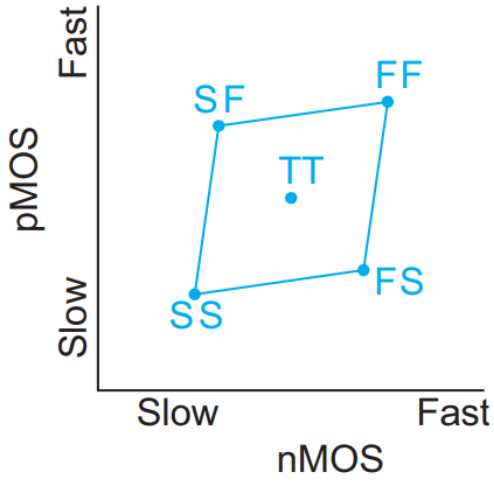

Figure 3.16: Design Corners [31]

4 Simulation results

The design was simulated at the schematic and post-layout level. At the beginning, simulations were performed at the schematic level to check the full ADC functionality. For quantitative understanding, both in terms of speed, power consumption, and resolution, post-layout simulations are relevant. Results of both simulations are presented in this work.

The ASIC containing the designed ADC has not yet been fabricated. However, the analog front-end—comprising the capacitive DAC array, bootstrapped sampling switches, and the dynamic comparator—remains identical to a previously fabricated and verified ADC design. Since these components primarily determine the static linearity, performance metrics such as INL and DNL can be reliably inherited from the earlier implementation.

Figures 4.1 and 4.2 present the measured static linearity of the original ADC. At 10 MSps, the INL remains below 0.4 LSB, and the DNL stays below 0.3 LSB across the full input range, fulfilling 10-bit resolution requirements. Asynchronous control logic ensures sampling rate independence, verified up to 50 MSps.

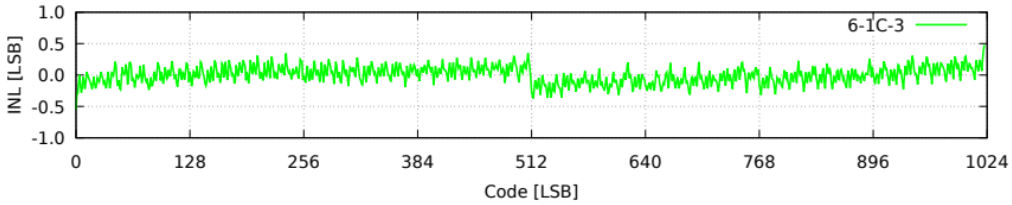

Figure 4.1: INL for ADC measured at 10 MHz sampling frequency [2]

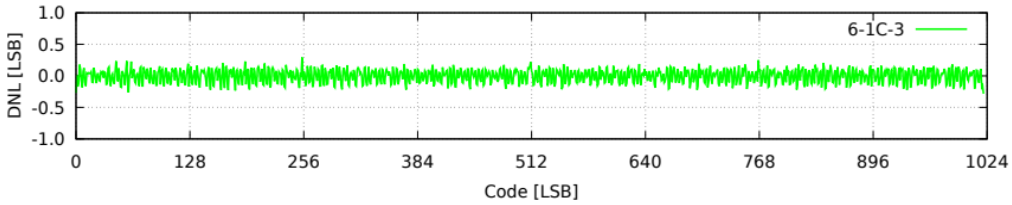

Figure 4.2: DNL for ADC measured at 10 MHz sampling frequency [2]

4.1 Schematic simulations

Schematic-level simulations were conducted to verify the correct functionality of the ADC architecture prior to layout implementation. The input signal was a sinusoidal waveform with amplitude close to full scale, ranging from 5 LSB to 1018 LSB. The frequency of the signal was set to the Nyquist frequency and number of samplest to 256. For simulations with the programmable threshold, the threshold delay was set to maximum value of 7 bits, corresponding to approximately 1225 ps. Other delays were set to default value equal 4.

Figure 4.3 presents the Effective Number of Bits (ENOB) as a function of sampling frequency for two operating modes: with the threshold functionality disabled and with the threshold set to 0 LSB, ensuring that the input always exceeds the threshold ($V_{in} > V_{th}$).

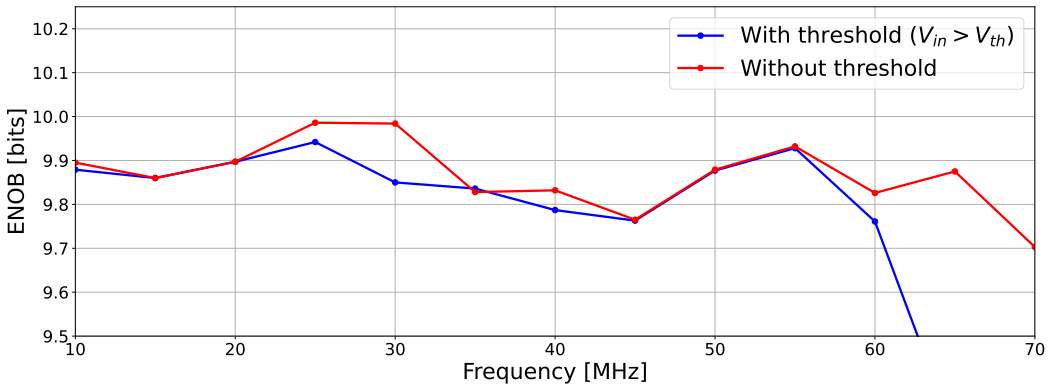

Figure 4.3: Effective number of bits versus sampling frequency in schematic simulation. Threshold mode uses $V_{th} = 0$, ensuring all input signals trigger a full conversion

The results demonstrate that ENOB exceeds 9.8 bits almost across the entire operational frequency range. The threshold mode configuration operates correctly up to 60 MSps, while the ADC with disabled threshold allows slightly higher sampling rates. The 10% difference is caused by the additional bit cycle required for threshold evaluation.

The power consumption versus sampling frequency is presented in Figure 4.4, showing three cases: threshold disabled, threshold enabled with $V_{in} > V_{th}$ (threshold 0 LSB corresponding to 100% hit occupancy) and with threshold in case when $V_{in} < V_{th}$ (threshold set to 100 LSB corresponding to 0% hit occupancy).

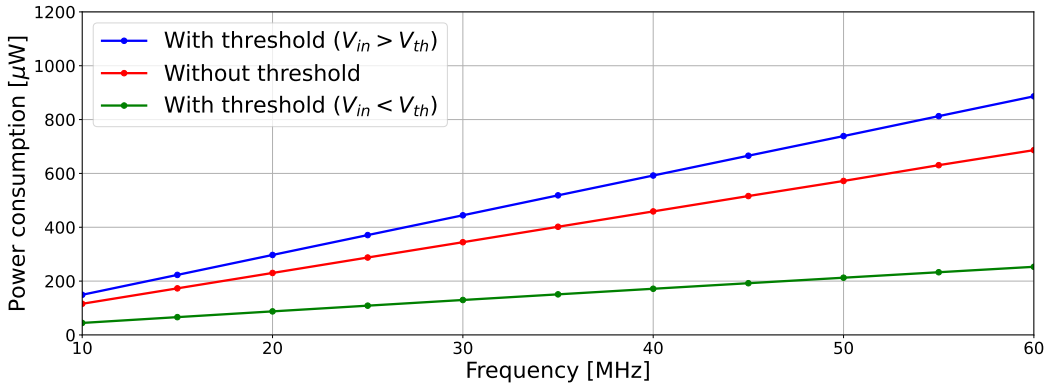

Figure 4.4: Power consumption versus sampling frequency in schematic simulation for three threshold configurations

The fastest conversion (only 2 bit cycles) with the lowest possible power occurs in the mode with threshold in case of $V_{in} < V_{th}$. In contrast, the slowest conversion (11 bit cycles) with the highest power consumption takes place in the threshold mode, with the signal ($V_{in} > V_{th}$), which corresponds to the 100% hit occupancy.

These simulations confirm that the design operates correctly at the schematic level, meeting the expected resolution and energy efficiency. The programmable threshold provides a mechanism for power reduction, particularly valuable in sparse data environments typical for high-energy physics readout systems with low particle occupancy. The ratio between the highest and the lowest power consumption is about 3.5.

4.2 Post-layout simulations

Post-layout simulations were done under the same conditions as the schematic simulations: the input signal was a near full scale ranging from 5 LSB to 1018 LSB, sampled at the Nyquist frequency with 256 points. In threshold mode cases, the delay for threshold comparison was set to the maximum value of 7 bits.

These simulations provide the most accurate performance prediction, incorporating parasitic capacitances, resistances, interconnect delays, and layout-level mismatches. While process variations can be evaluated at the schematic level, post-layout simulations capture layout-specific effects that are essential for validating the ADC's behavior. Figure 4.5 shows the post-layout ENOB versus sampling frequency.

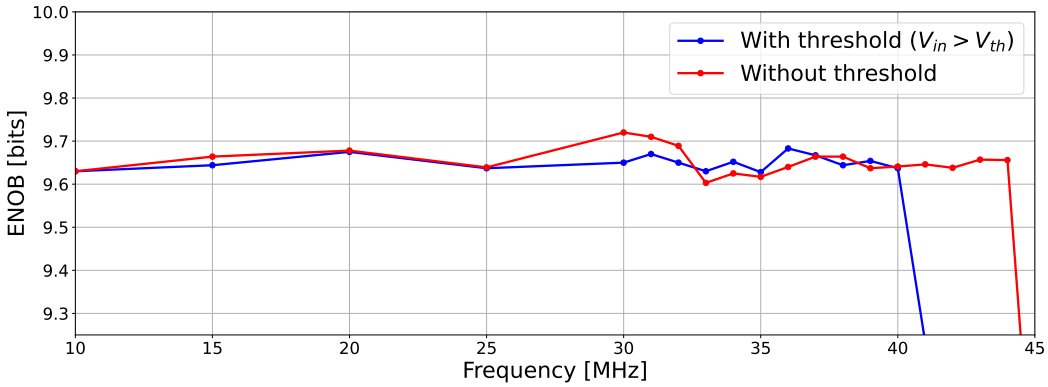

Figure 4.5: Effective number of bits versus sampling frequency

In post-layout simulations, an ENOB of > 9.6 bits at the Nyquist frequency was obtained. Compared to pre-layout results, the 0.2 bit degradation comes mainly from parasitic coupling in the DAC array. The ENOB remains stable up to 40 MSps with threshold and up to 44 MSps with same delays without threshold.

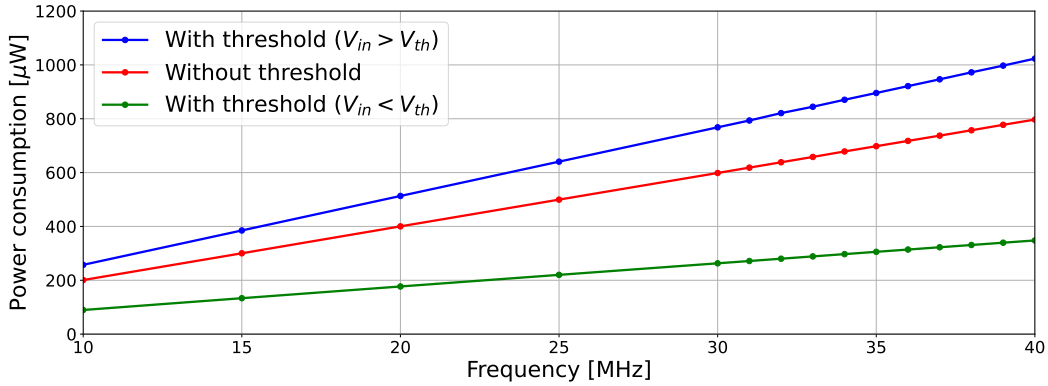

Figure 4.6: Power consumption versus sampling frequency

The post-layout power consumption, presented in Figure 4.6 increases about 1.7 times versus schematic estimates due to parasitic resistances in the DAC switches and clock distribution network. Power consumption at 40 MSps is around 350 μW in case of $V_{in} < V_{th}$ and 1000 μW when $V_{in} > V_{th}$.

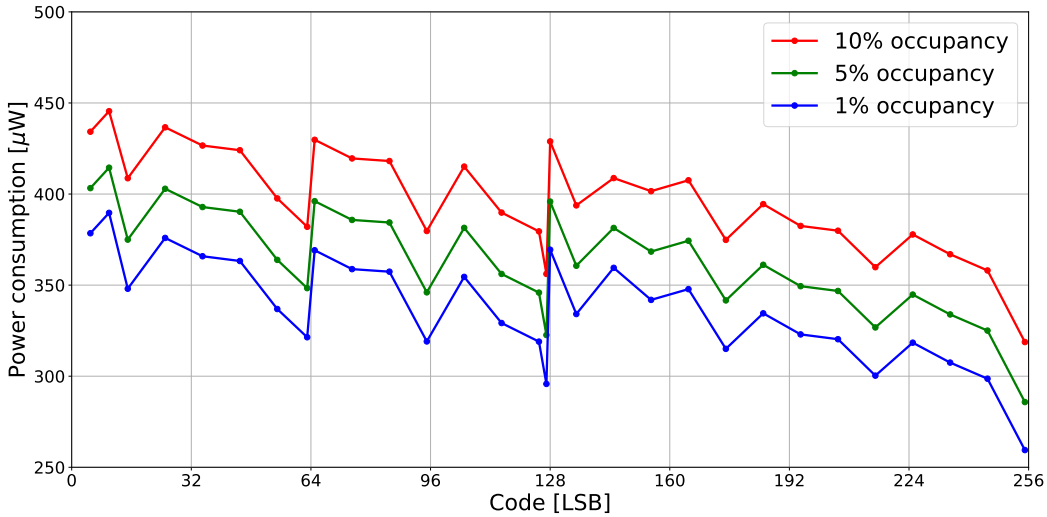

Figure 4.7: Power consumption versus threshold for different occupancies @40 MSps

For low particle occupancies, Figure 4.7 confirms significant power savings. At 40 MSps, average consumption drops to about 350 µW, which is 50% lower than in threshold-disabled mode. These results validate the design's suitability for high-energy physics applications with low occupancy.

4.3 Worst Case simulations

Validating the ADC's reliability under extreme process and environmental variations is critical for high energy physics applications, where radiation-induced shifts and manufacturing tolerances must be accounted for. Figure 4.8 illustrates the ENOB across seven design corners:

- **TT (Typical-Typical):** Nominal transistor model, used as the reference.
- **FF (Fast-Fast):** Both nMOS and pMOS transistors operate at maximum speed.
- **SS (Slow-Slow):** Minimal switching speed for both transistor types.

In addition to these corners, extended four-letter marked process corners were also used. The first two characters indicate parasitic capacitance and resistance conditions — **FF** for low parasitics, resulting in faster operation, and **SS** for high parasitics, leading to slower transitions. The last two letters define the individual speed characteristics of the nMOS and pMOS transistors, respectively. For example, **FF_SF** represents low parasitic capacitance, with a slow nMOS and fast pMOS device.

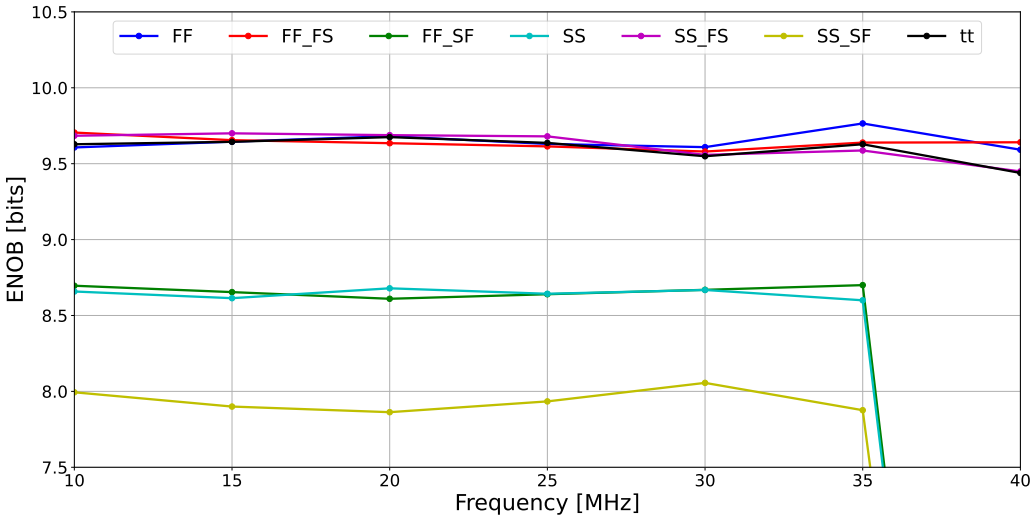

Figure 4.8: ENOB of all corners versus sampling frequency

The worst performance is observed in corners with slow nMOS transistors (FF_SF, SS_FS, SS_SF), as the pull-down speed limits the comparator's decision window and DAC settling time. In particular, the SS_SF corner shows the lowest ENOB due to the combination of slow devices and large parasitic capacitance, which introduces significant delay.

Although the ADC includes a programmable 4-bit delay block to compensate for corner-related timing shifts, in extreme cases this is not sufficient. Increasing delay helps stabilize operation, but directly reduces the maximum sampling frequency. Since the ADC reaches 41 MHz under nominal conditions, any further delay would decrease the ADC speed below the 40 MHz minimum required for readout in LHC type detectors. Delay configuration is also critical for achieving satisfactory ENOB, particularly in threshold-enabled operation. Figure 4.9 illustrates the relationship between ENOB and the programmable delay bit for threshold.

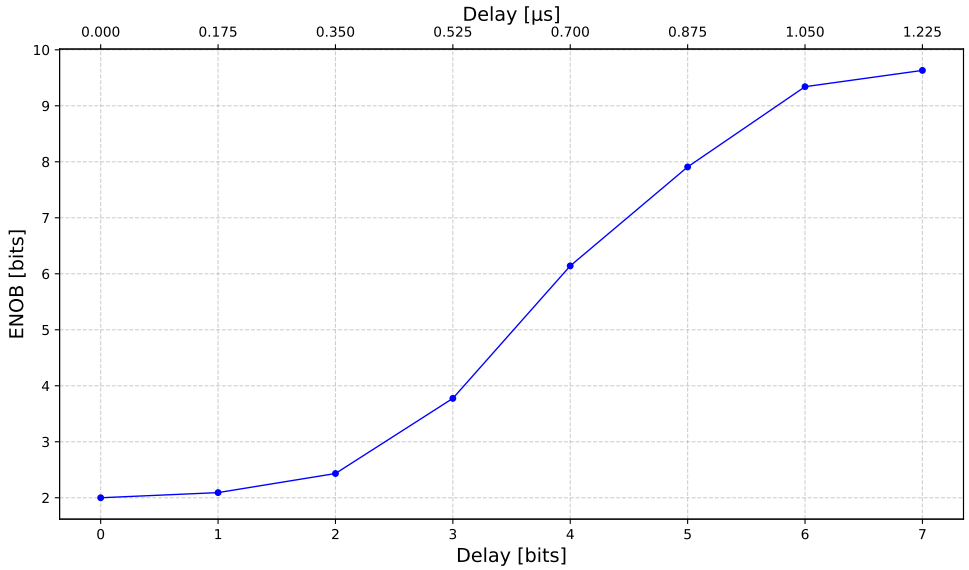

Figure 4.9: ENOB versus threshold delay bit

To address this limitation, the author plans to extend the threshold delay by adding an even number of inverters to the critical path. However, this modification would preclude achieving the target 40 MSps sampling rate in the current 130 nm technology. It is anticipated that going to more advanced nodes (e.g., 65 nm or 28 nm) will resolve this problem, as smaller transistor dimensions enable faster switching.

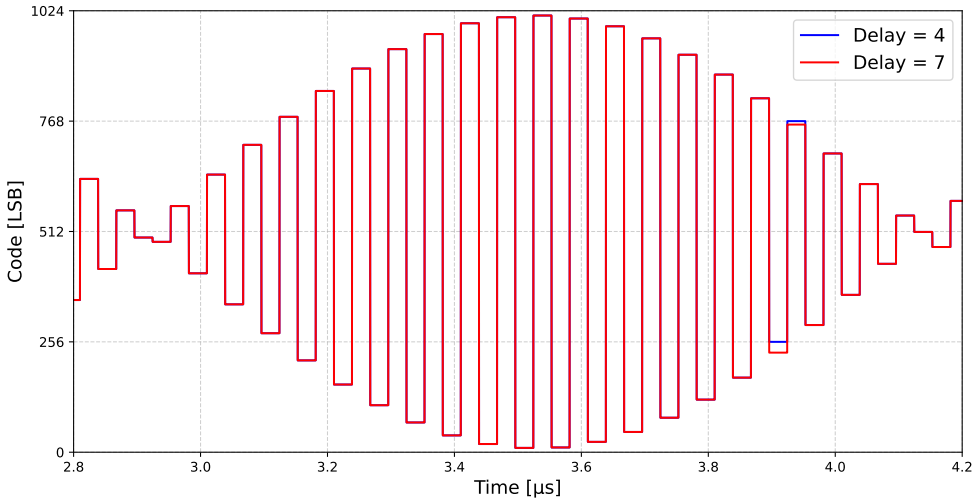

Figure 4.10: Simulation results for threshold delay bit 4 and 7

Figure 4.10 compares amplitude results obtained with sine input signal for threshold delay 4 and 7. Differences are small and localized to specific codes, primarily caused by transient voltage overshoot during rapid DAC switching.

4.4 Monte Carlo simulations

Monte Carlo simulations were performed for 100 samples of the ADC design with randomized component parameters. These simulations were conducted at the schematic level, as the post-layout equivalent would require over 5 hours per point, while schematic simulations complete within approximately 30 minutes. Figure 4.11 presents the results for ENOB, which is the most critical performance parameter in this design and most sensitive to component mismatch.

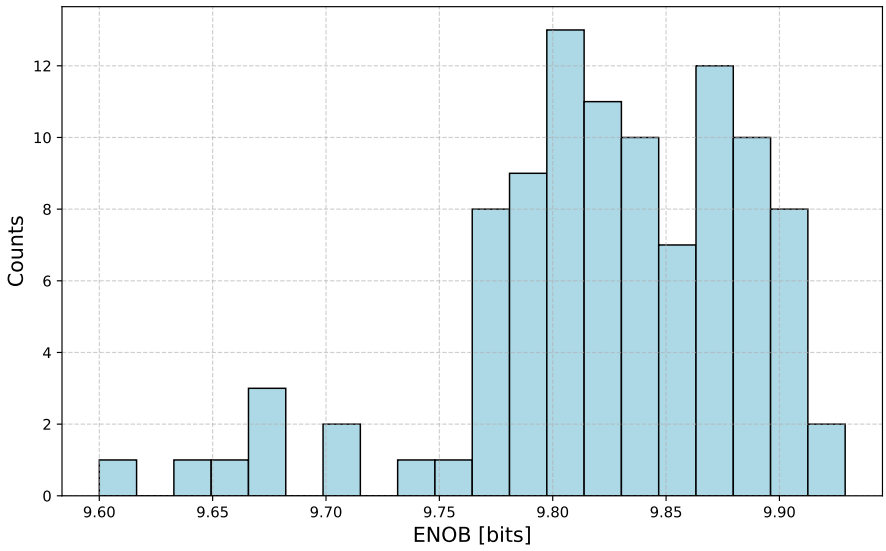

Figure 4.11: Monte Carlo simulation of ENOB

The simulation conditions match those used in previous performance analyses, including the sampling rate of 40 MHz. The resulting ENOB values are centered between 9.8 and 9.9 with limited variation and no significant outliers, few lowest results appearing around 9.6. Despite the absence of layout parasitics in this simulation, the schematic-level Monte Carlo provides meaningful insight into statistical sensitivity and performance margins. Given the high computational cost of post-layout Monte Carlo analysis, the schematic approach is a practical and informative compromise at the current design stage. This confirms that the design is robust under process-induced variations and meets the reliability requirements for high-energy physics front-end systems.

4.5 Comparison with existing SAR ADCs

In Table 4.1, the key parameters of the designed 10-bit SAR ADC are compared to state-of-the-art 10-bit ADCs implemented in the same 130 nm CMOS technology. The proposed ADC achieves an excellent FOM of **10 fJ/conv.-step**, as defined in Equation 2.3. This result represents a significant improvement in energy efficiency for 130 nm technology, made possible by the programmable threshold functionality under low occupancy conditions.

The physical area of the ADC is compact and equals 0.048 mm^2, making it suitable for multi-channel readout ASICs used in HEP detectors. The design maintains an 80 µm pitch, which is important for integration into large scale detector systems.

Importantly, the programmable threshold functionality allows the ADC to reduce its average power consumption from 680 µW without threshold to approximately 350 µW at 40 MSps for low occupancy, giving at least a 50% reduction. This feature makes the ADC especially suitable for sparse data environments, such as those found in tracking or calorimeter systems at the LHC and future colliders.

Table 4.1: Comparison of the designed SAR ADC with state-of-the-art implementations in same technology, sorted by FOM

	[35]	[34]	[32]	[33]	[2]	This work [1]
CMOS [nm]	130	130	130	130	130	130
Supply Voltage [V]	1.2	1.2	1.2	1.2	1.2	1.2
Area [mm^2]	0.32	0.095	0.088	0.052	0.048	0.048
$f_{\mathbf{sample}}$ **[MHz]**	40	20	30	50	50	40
Power [μW][a]	550	620	660	826	850	350[b]
Max INL [LSB]	1.55	0.47	∼0.5	1.36	0.4	0.4
Max DNL [LSB]	0.78	0.34	∼0.5	0.91	0.3	0.3
ENOB [bits]	8.11	9.32	9.25	9	9.6	9.65
FOM [fJ/conv.-step]	50	48	37	32	21.5	10.6[b]

[a] In all ADCs an external reference voltage is used, [b] For low particle occupancy

The FOM achieved by the ADC presented in this work is more than two times lower than the best previously reported value for SAR ADC implemented in CMOS 130 nm technology. This demonstrates the efficiency of power reduction method due to the implemented programmable threshold. Furthermore, as shown in Table 4.2, the comparison includes ADCs fabricated in more advanced process nodes such as 90 nm, 65 nm, 40 nm, and even 28 nm.

Table 4.2: Comparison with state-of-the-art SAR ADCs in advanced technologies, sorted by FOM

	[39]	[38]	[37]	[36]	This work [1]	[40]
CMOS [nm]	65	90	40	65	130	28
Supply Voltage [V]	1.0	1.1/1.3	1.2	1.2	1.2	0.55
Area [mm^2]	0.039	0.024	0.027	0.014	0.048	0.030
f_{sample} [MHz]	50	50	100	40	40	100
Power [μW][a]	820	664	1090	402	350[b]	160
Max INL [LSB]	0.82	0.45	0.82	0.89	0.4	1.5
Max DNL [LSB]	0.72	0.36	0.73	0.52	0.3	0.86
ENOB [bits]	9.1	9.26	9.06	9.32	9.65	8.79
FOM [fJ/conv.-step]	29.7	21.68	20.4	15.69	10.6[b]	3.6

[a] In all ADCs an external reference voltage is used, [b] For low particle occupancy

Despite the natural advantages of scaling (e.g., lower parasitic capacitance, higher speed), almost none of these designs achieve a comparable level of FOM. In fact, most of them either require significantly higher power or deliver lower resolution under similar sampling conditions.

This confirms that the design presented in this thesis is competitive not only within the same technology node, but also outperforms many solutions implemented in more advanced CMOS processes. The result highlights the effectiveness of architectural optimizations, such as MCS, DAC segmentation, asynchronous logic and programmable threshold, in reducing overall power consumption without sacrificing resolution.

The design presented in this work is based on the verified existing ADC, suggesting that the same simulated performance can be obtained after fabrication. However, it must be noted that the presented results are based on post-layout simulations. Experimental verification of prototype ADC with measurements is needed for confirmation of these results.

Summary

This thesis presents the design, implementation and simulation of a 10-bit Successive Approximation Register (SAR) Analog-to-Digital Converter (ADC) optimized for High Energy Physics applications. The work focuses on minimizing power consumption while preserving resolution and speed, in order to support multi-channel readout systems in modern particle detectors. The key innovation introduced in this design is the implementation of a programmable input threshold, allowing the conversion process to be terminated early for low-amplitude signals. This mechanism significantly reduces average power consumption under low input occupancy, without affecting the ADC's resolution and with not significantly reducing the speed.

The work was structured into four main chapters. The first chapter introduced the context of High Energy Physics experiments, including a brief overview of the Standard Model and current large-scale facilities such as the LHC and DESY. The second chapter focuses on Analog-to-Digital Converters, as one of the key blocks of signal processing in modern ASICs. It discusses fundamental principles of ADC operation, performance parameters and commonly used architectures in low-power applications. Key performance parameters such as ENOB, INL, DNL, and FOM are discussed in detail, providing a solid foundation for understanding the design challenges. In next chapter, author presented the design of the proposed 10-bit SAR ADC in 130 nm CMOS technology. Aside from several already used techniques to reduce power consumption using the Merged Capacitor Switching algorithm, segmented capacitive DAC or asynchronous dynamic control logic, author implemented a programmable threshold logic to detect low-level input signals and skip unnecessary bit cycles, reducing overall power consumption. Detailed schematic and layout-level implementation are provided, especially the logic behind the programmable threshold. The fourth chapter focuses on schematic and post-layout simulations, particularly on power consumption, speed and resolution results.

In the proposed design, the analog part remained unchanged and includes the original DAC architecture, the dynamic comparator and the bootstrap switches. These blocks were verified to meet performance requirements and did not require changes. The main modifications were made in the digital block, primarily in the control logic responsible for the conversion process. Several improvements were implemented to enable programmable threshold functionality. The Programmable Delay block was redesigned and now second delay group controls threshold delay instead of delay for bits 8 and 7 in threshold mode. The Enumerate Shift Register was updated to include an extra conver-

sion step, enabling the integration of programmable threshold functionality. Furthermore, in the DAC Reference Switches Control block, additional multiplexers were added to allow switching based on the Threshold Logic output. The comparison with the programmable threshold now occurs only when the threshold mode is enabled and only after the MSB result.

Schematic-level simulations showed that the ADC achieves an ENOB above 9.6 bits across the entire operating frequency range, and the programmable threshold mechanism provides substantial power savings depending on hit occupancy. Post-layout simulations further validate these results. The ADC operates reliably up to 40 MSps with ENOB around 9.6 bits and under low particle occupancy the power consumption drops to approximately 350 μW at 40 MSps. These results represent a 50% reduction in power compared to the previous implementation without the threshold feature.

A comprehensive comparison with other state-of-the-art 10-bit SAR ADCs implemented in 130 nm CMOS technology confirms, that the presented design achieves the best overall energy efficiency. The Figure of Merit (FOM) is approximately 10 fJ/conversion-step, which is more than two times lower than any previously published design in this technology node. Furthermore, when compared to implementations in more advanced technologies, the proposed ADC still outperforms many designs in terms of power and resolution, demonstrating the effectiveness of optimizations over process scaling.

The results of this work were presented by author in poster session at the *TWEPP 2024 Topical Workshop on Electronics for Particle Physics* held in Glasgow, and published in the *Journal of Instrumentation (JINST)* [1]. A prototype ASIC including multiple instances of the proposed ADC is currently under preparation and will be submitted for fabrication in the near future. Further work will focus on silicon measurements and radiation testing, as well as migrating the design to more advanced technology nodes to explore potential improvements in speed and power scaling.

The techniques proposed in this thesis demonstrate that significant energy savings can be achieved in readout systems for HEP experiments without requiring major changes to process technology. By combining circuit-level optimization with application-specific adaptations such as threshold control, it is possible to build scalable, low-power multi-channel readout ASICs for future detectors at the LHC and future experiments.

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Bibliography

[1] P. Prus, M. Firlej, T. Fiutowski, M. Idzik, J. Moroń, K. Świentek, *Development of a 10-bit ultra-low power SAR ADC with programmable threshold in 130 nm CMOS technology*, *Journal of Instrumentation*, 2025.

[2] M. Firlej, T. Fiutowski, M. Idzik, S. Kulis, J. Moron, K. Swientek, *An Ultra-Low Power 10-bit, 50 MSps SAR ADC for Multi-Channel Readout ASICs*, *Journal of Instrumentation*, JINST 18 (2023) P11013.

[3] E. Torassa, *The Standard Model and Higgs physics*, *Progress in Particle and Nuclear Physics*, Vol. 100, May 2018.

[4] J. Knaster, R. Veness, L. Gamez-Mejias, *The vacuum chamber in the interaction region of particle colliders: a historical study and developments implementations in the LHCb experiment at CERN*, 2004.

[5] D. Horváth, *Twenty Years of Searching for the Higgs Boson: Exclusion at LEP, Discovery at LHC*, arXiv:1402.6103, 2014.

[6] Spektrum.de, *DESY*, `https://www.spektrum.de/lexikon/physik/desy/2934`, accessed: 06.03.2025.

[7] J. List, *Status of e+e- Higgs factory projects*, in *Proceedings of The European Physical Society Conference on High Energy Physics — PoS(EPS-HEP2023)*, 2023.

[8] S. Franco, *Design with Operational Amplifiers and Analog Integrated Circuits* (4th ed.), 2014.

[9] X. Tang, J. Liu, Y. Shen, S. Li, L. Shen, A. Sanyal, K. Ragab, N. Sun, *Low-Power SAR ADC Design: Overview and Survey of State-of-the-Art Techniques*, *IEEE Transactions on Circuits and Systems I: Regular Papers*, 2022.

[10] W. Kester, *ADC Architectures III: Sigma-Delta ADC Basics*, January 2011.

[11] O. Aytar, A. Tangel, K. Şahin, *A 5-bit 5 Gs/s flash ADC using multiplexer-based decoder*, *Turkish Journal of Electrical Engineering & Computer Sciences*, 2013.

[12] B. P. Ginsburg, A. P. Chandrakasan, *An Energy-Efficient Charge Recycling Approach for a SAR Converter With Capacitive DAC*, *IEEE Journal of Solid-State Circuits*, 2005.

[13] J. Guerber, V. Hariprasath, T. Oh, U.-K. Moon, *Enhanced SAR ADC energy efficiency from the early reset merged capacitor switching algorithm*, in *2012 IEEE International Symposium on Circuits and Systems (ISCAS)*, 2012.

[14] R. Hedayati, *A Study of Successive Approximation Registers and Implementation of an Ultra-Low Power 10-bit SAR ADC in 65nm CMOS Technology*, 2011.

[15] S. Arar, *ADC Offset and ADC Gain Error Specifications*, All About Circuits, July 17 2022. `https://www.allaboutcircuits.com/technical-articles/adc-offset-and-gain-error-specifications/`, accessed: 09.03.2025.

[16] K. H. Lundberg, *Analog-to-Digital Converter Testing*, MIT. `https://www.mit.edu/~klund/A2Dtesting.pdf`, accessed: 09.03.2025.

[17] R. J. Baker, *CMOS Circuit Design, Layout, and Simulation* (3rd ed.), Vol. 3, Chapter 29: *Data Converter Architectures*, Wiley-IEEE Press, 2010.

[18] Curtiss-Wright Defense Solutions, *This Matters: Spurious Free Dynamic Range (SFDR)*, 2015. `https://www.curtisswrightds.com/media-center/blog/spurious-free-dynamic-range-sfdr`, accessed: 09.03.2025.

[19] V. Hariprasath, J. Guerber, S.-H. Lee, U.-K. Moon, *Merged capacitor switching based SAR ADC with highest switching energy-efficiency*, 2010.

[20] D. Osipov, Y. Bocharov, *Behavioral model of split capacitor array DAC for use in SAR ADC design*, 2012.

[21] F. Bouyjou, G. Bombardi, F. Dulucq, A. El Berni, S. Extier, M. Firlej, T. Fiutowski, F. Guilloux, M. Idzik, C. De La Taille, A. Marchioro, A. Molenda, J. Moron, K. Swientek, D. Thienpont, T. Vergine, *The front-end readout ASIC for the CMS High Granularity Calorimeter*, *Journal of Instrumentation*, JINST C03015 2022.

[22] T. Niknejad, E. Albuquerque, A. Benaglia, A. Boletti, R. Bugalho, F. De Guio, M. Firlej, T. Fiutowski, R. Francisco, M. Gallinaro, A. Ghezzi, M. Idzik, M. Lucchini, M. Malberti, J. Moron, L. Oliveira, M. Pisano, N. Redaelli, J.C. Silva, R. Silva, M. Silveira, K Swientek, T. Tabarelli de Fatis, J. Varela, *Results with the TOFHIR2X Revision of the Front-end ASIC of the CMS MTD Barrel Timing Layer*, 2021 IEEE Nuclear Science Symposium and Medical Imaging Conference Record (NSS/MIC).

[23] J. Moron, *FLAME SoC readout ASIC for electromagnetic calorimeter*, September 19–23 (2022), TWEPP2022 Topical Workshop on Electronics for Particle Physics, `https://indico.cern.ch/event/1127562/contributions/4904506/`, accessed: 15.03.2025.

[24] S. Conforti Di Lorenzo, A. Afiri, S. Bolognesi, G. Bombardi, F. Bouyjou, S. Callier, C. De La Taille, P. Dinaucourt, O. Drapier, F. Dulucq, A. El Berni, S. Extier, M. Firlej, T. Fiutowski, F. Gastaldi, F. Guilloux, M. Idzik, A. Marchioro, A. Mghazli, A. Molenda, J. Moron, J. Nanni, B. Quilain, L. Raux, K. Swientek, D. Thienpont and T. Vergine, *HKROC: an integrated front-end ASIC to readout photomultiplier tubes for the Hyper-Kamiokande experiment*, *Journal of Instrumentation*, January 2023.

[25] M. Dessouky and A. Kaiser, *Input switch configuration suitable for rail-to-rail operation of switched opamp circuits*, *Electron. Lett. 35*, 1999.

[26] L. Sumanen, M. Waltari, K. A. I. Halonen, *A 10-bit 200-MS/s CMOS Parallel Pipeline A/D Converter*, *IEEE Journal of Solid-State Circuits*, July 2001.

[27] V. Hariprasath, J. Guerber, S.-H. Lee and U.-K. Moon, *Merged capacitor switching based SAR ADC with highest switching energy-efficiency*, *Electron. Lett. 46* (2010) 620

[28] H.J. Jeon, Y.-B. Kim and M. Choi, *Offset voltage analysis of dynamic latched comparator*, in the proceedings of the *2011 IEEE 54th International Midwest Symposium on Circuits and Systems (MWSCAS)*, 2011

[29] S. Naghavi, M. Nematzade, N. Sharifi, T. Moradi Khanshan, A. Abrishamifar, Z. Kuzekanani, J. Sobhi, *A Simple and Efficient Charge Injection Error Compensation Structure for MOS Sampling Switches*, *Journal of Circuits, Systems and Computers*, 2017.

[30] M. Shahid, *The Multiplexer*, Electronics-Lab.com. `https://www.electronics-lab.com/article/the-multiplexer/`, accessed: 15.03.2025.

[31] N. H. E. Weste, D. M. Harris, *CMOS VLSI Design: A Circuits and Systems Perspective* (4th ed.), 2010.

[32] M. Firlej, T. Fiutowski, M. Idzik, S. Kulis, J. Moroń, K. Świentek, *A fast, ultra-low and frequency-scalable power consumption, 10-bit SAR ADC for particle physics detectors*, *Journal of Instrumentation*, 2015.

[33] C.-C. Liu, S.-J. Chang, G.-Y. Huang, Y.-Z. Lin, *A 10-bit 50-MS/s SAR ADC With a Monotonic Capacitor Switching Procedure*, *IEEE Journal of Solid-State Circuits*, April 2010.

[34] S.-M. Park et al., *A 10-bit 20-MS/s asynchronous SAR ADC with controllable analog input voltage range and meta-stability detection circuit*, in *2014 International SoC Design Conference (ISOCC)*, Jeju, South Korea, 2014.

[35] S.-H. Cho, C.-K. Lee, J.-K. Kwon, S.-T. Ryu, *A 550-uW 10-b 40-MS/s SAR ADC With Multistep Addition-Only Digital Error Correction*, *IEEE Journal of Solid-State Circuits*, 2011.

[36] M. Firlej, T. Fiutowski, M. Idzik, J. Moroń, K. Świentek, *Ultra-low power 10-bit 50–90 MSps SAR ADCs in 65 nm CMOS for multi-channel ASICs*, *Journal of Instrumentation*, 2024.

[37] Y. Shen, X. Tang, X. Xin, S. Liu, Z. Zhu, N. Sun, *A 10-bit 100-MS/s SAR ADC With Always-On Reference Ripple Cancellation*, *IEEE Transactions on Circuits and Systems I: Regular Papers*, 2022.

[38] C.-C. Lu, D.-K. Huang, *A 10-Bit 50-MS/s SAR ADC Based on Area-Efficient and Low-Energy Switching Scheme*, *IEEE Access*, vol. 8, pp. 106941-106950, 2020.

[39] M. Yoshioka, K. Ishikawa, T. Takayama, S. Tsukamoto, *A 10-b 50-MS/s 820-uW SAR ADC With On-Chip Digital Calibration*, *IEEE Transactions on Biomedical Circuits and Systems*, 2010.

[40] Y. Zhao, C. Chen, J. Yang, *A 0.55V 10-Bit 100-MS/s SAR ADC With 3.6-fJ/Conversion-Step in 28nm CMOS for RF Receivers*, *IEEE Transactions on Circuits and Systems II: Express Briefs*, June 2023.