AGH University of Science and Technology

Doctoral dissertation

New pixel detectors in SOI technology for particle physics applications

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Declaration of Authorship

Declaration of the author of this dissertation:

Aware of legal responsibility for making untrue statements I hereby declare that I have written this dissertation myself and all the contents of the dissertation have been obtained by legal means.

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Declaration of the dissertation Supervisor:

This dissertation is ready to be reviewed.

(Prof. dr hab. inż. Marek Idzik)

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Date: _____

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Dedication

This dissertation is lovingly dedicated to my mother, late Lateefa Begum, a smart woman whom I still miss every day. Her constant love, encouragement, and support have sustained me throughout my life. One more day closer to meet her.

"And the heaven We constructed with strength, and indeed, We are [its] expander."

(The Qur'an, 51:47)

AGH UNIVERISTY OF SCIENCE AND TECHNOLOGY

Abstract

Faculty of Physics and Applied Computer Science

Doctor of Philosophy

New pixel detectors in SOI technology for particle physics applications

by Mohammed Imran AHMED

Semiconductor detectors play an important role in many areas of science and research. The variety of available semiconductor technologies allows the production of devices which match the stringent requirements of scientific experiments. For particle physics applications, detectors must show very good efficiency for recording ionising radiation, precise timing, high spatial resolution, truly 2-Dimensional readout, resistance to radiation and low mass. These requirements are often contradicting each other and can be only overcome by the exploration of new ideas on detectors and new technologies. During the last decade, significant research and development activities have taken place in the field of Silicon On Insulator (SOI) CMOS technology resulting, in improvements in wafer size, wafer resistivity, radiation tolerance and spatial resolution. Profiting from the insulator Buried OXide (BOX) layer separating devices from the substrate, one can select the substrate that has the required properties. SOI is an ideal choice for fabricating monolithic pixel detectors to replace the established hybrid pixel detectors used in present High Energy Physics (HEP) experiments.

Novel CMOS monolithic pixel detectors designed at KEK in Japan and fabricated at Lapis Semiconductor using 200 nm SOI technology are presented. The potential of SOI CMOS technology has been successfully demonstrated by designing several novel pixel detectors which are gradually entering into the application phase. These include the INTegration type PIXel (INTPIX), Dual mode Integration type PIXel (DIPIX), and CouNTing type PIXel Detector (CNTPIX) detectors. The development of integration type pixel detectors is of interest for the physics communities because it combines optimisation of design and simplicity of production, meaning lower cost, and reduction of detector material budget.

In this dissertation the characterization and performance of integration type pixel detectors (i.e. INTPIX3a, INTPIX3b, and DIPIX) are presented. A method of mitigating the back gate effect using Technology Computer Aided Design (TCAD) simulation is also presented, which limiting the application of a large bias voltage and making the detector only partially depleted. Both detectors (INTPIX3a and INTPIX3b) consist of several pixel topologies which differ in the dimension of p+ implant and Buried P-Well (BPW). The test results of all regions were obtained with the visible laser and Americium 241 (Am-241) source and compared. Electrical measurements of both prototype parameters were also performed. The DIPIX detectors were fabricated on three different wafer resistivities (CZ-n, FZ-n, and FZ-p), which have been measured using visible and infrared lasers to study the full depletion voltage. The measurement of Equivalent Noise Charge (ENC) and pixel current at three different temperatures (i.e. 20^{o}C, 5^{o}C, and -20^{o}C) are also presented. The measured performance demonstrates that SOI technology is a feasible choice for future applications.

Contents

Introduction

The theory which describes matter and the interaction between elementary particles is the so called Standard Model (SM). It is well accepted by the physics community as the state of the art of fundamental particle interactions. However many basic questions, mainly neutrino masses, gravitational force, spontaneous breaking of the electroweak symmetry, and antimatter in the universe, remain unanswered. Nowadays, the particle physics world tries to find new physics beyond, the SM using two complementary approaches: the energy frontier and the precision frontier.

At present the Large Hadron Collider (LHC) located at European Council for Nuclear Research (CERN) is the high energy particle collider operating in the energy frontier. It is equipped with four multi-purpose experiments: A Toroidal LHC Apparatus (ATLAS) [1], A Large Ion Collider Experiment (ALICE) [2], Compact Muon Solenoid (CMS) [3], and Large Hadron Collider beauty (LHCb) [4], around its perimeter. It is operating and collecting data from the collisions of protons or heavy ions. One of the primary scientific goals of the LHC was to discover the Higgs boson [5]. In 2012 the LHC was operated at higher intensities which helps in mitigating the more challenging conditions and observing the Higgs boson. The Higgs boson was observed with a mass of about 125 GeV/c^2 with a local significance of 5.0 σ by the experiments ATLAS and CMS [6, 7], and this discovery is a fundamental step forward to understand the dynamics of electroweak symmetry breaking [8].

The Belle II experiment and SuperKEKB collider located at High Energy Accelerator Research Organisation (KEK), Tsukuba which is currently in an upgrade phase will be used to operate at the precision frontier and is planned to start operation in late 2015. On the other hand a large international project is under development. Since 10 years the International Linear Collider (ILC) has been discussed and very likely will be built in Japan [9]. The interaction region of the ILC has been designed to host two detectors, which can be moved into the beam position with a push-pull scheme. Both ILC detector concepts, Silicon Detector (SiD) and International Large Detector (ILD), have high precision vertex detectors built of pixels for short particles tagging [10, 11].

In High Energy Physics (HEP) experiments particles can be collided in two ways: one is fixed target where a high energy beam is directed onto a stationary target, and second is a modern colliding beam method in which two beams are accelerated in opposite directions. When they collide with higher and higher energy, massive particles can be created. To detect the properties of these particles huge detector systems are made around the interaction point. The detector systems are equipped with different detectors such as vertex, tracker detector, and calorimeters to measure the parameters of the particle and its identification. Since the detectors involved in tracking have millions of readout channels, it is essential to have an optimised readout electronics system to handle a huge amount of information.

Today almost all particle physics experiments use vertex detectors to reconstruct tracks of particles and to identify and reconstruct primary and secondary interaction vertices. Such detectors are constructed either of strip sensors or, what is advantageous at high densities of tracks, pixel sensors. Currently, experiments at LHC use hybrid pixel sensors as components of their vertex detectors for their truly two-dimensional readout and good performance in radiation environment. Hybrid pixel detectors consist of two chips, one for sensor and another one for readout electronics, connected together by metal bumps thus forming a detector module. The advantage of a such construction is that one can optimise the sensor material (e.g. high resistivity silicon) and the material in which the readout electronics is produced (e.g. low resistivity silicon). The drawback of this solution is the high mass, which affects the precision of tracking (because of multiple scattering) and energy measurements (due to electron scattering and gamma conversions), and also the occupancy. In the last few years detector developers have started to explore the possibility of building monolithic active pixel sensors [12, 13, 14, 15], which have a potential to replace hybrid pixel detectors by offering higher granularity, thus lowering occupancy, better spatial resolution, and having lower material budget. One of the option is to fabricate Complementary Metal-Oxide-Semiconductor (CMOS) devices on Silicon On Insulator (SOI) wafers, consisting of low resistivity material for electronics fused by thin silicon oxide with the high resistivity material of the sensor. CMOS monolithic pixel detectors described in this dissertation have been developed at KEK and fabricated at Lapis Semiconductor Co., Ltd, using 200 nm SOI technology.

The main objective of this dissertation is to validate the performance and characterisation of the prototypes of integration type pixel detectors designed in SOI technology. The electrical measurements of prototype parameters are performed. A test set-up was built to study the response of the detector to laser and radiation sources. The Technology Computer Aided Design (TCAD) simulations (ENEXSS 5.5) were done to study the back gate effect from the electric field distribution and transistor characteristics. The depletion study using two laser wavelengths (660 nm and 1060 nm), the measurements

of Equivalent Noise Charge (ENC) using an Americium 241 (Am-241) radiation source, and the measurements of leakage current at lower temperature, were performed on the detector prototypes. These studies were done on three different wafers (Czochralski n type wafer (CZ-n), Float Zone n type wafer (FZ-n), and Float Zone p type wafer (FZ-p)) and measurements results were compared.

The dissertation is organised as follows:

- In chapter 1, the physics motivation will be discussed which contains a brief description of the vertex and tracking detector. A method to determine the momenta, secondary vertices and impact parameter is presented. The need of monolithic pixel detectors for future upgrades of HEP experiments is also discussed. In the following section the brief description, advantages and disadvantages of different semiconductor detectors are discussed. In particular, several monolithic pixel detectors are discussed. Finally, the advantages of SOI CMOS technology and issues which were mitigated are listed.

- In chapter 2, the importance of TCAD simulation software and the physics of semiconductor devices will be explained, followed by the description of different tools available in Environment for NEXt Simulation System (ENEXSS) TCAD software. The simulation results of SOI prototype performed using Hyper Device-Level Electrical Operation Simulator (HyDeLEOS) tool are presented. It is shown that the transfer characteristic of N-type Metal-Oxide-Semiconductor (NMOS) IO transistor obtained with cadence is similar to the TCAD simulation results. Also the mitigation of the back gate effect is clearly seen from the electric field distribution.

- Chapter 3 is divided into two parts: the first part presents the test set-up and data analysis methods, which were used for the measurements of both the INTegration type PIXel (INTPIX)3 and Dual mode Integration type PIXel (DIPIX)2 detectors. The second part presents the measurements of test structures implemented in the INTPIX3a detector. It is followed by the description of the INTPIX3a and INTPIX3b architecture and measurements. The measurement results include the comparison of different regions of INTPIX3a and INTPIX3b in terms of long time stability, performance using a laser, and ENC measurements using a radiation source Am-241.

- In chapter 4, the architecture, stability test, laser and radiation source measurements of DIPIX2 detector are presented. The performance study of the DIPIX2 detector was done with an Am-241 radiation source, and with 660 nm and 1060 nm wavelength lasers . Several pixels were scanned using both lasers to confirm its linearity and pixel size accuracy. The development of a depletion layer was studied

using a synchronised laser for three different wafer resistivities. The measurements of ENC and gain at room temperature (+20^{o}C), +5^{o}C, and -20^{o}C were performed using an Am-241 radiation source for two wafers, CZ-n and FZ-p. The pixel current and noise were also studied for better understanding of the ENC quantitative results. Finally, the summary and conclusions are given.

Chapter 1

Semiconductor Detectors in Particle Physics

In 1974 particles with charm quark were discovered [16] having lifetime in 10^{-13}s range [17]. This means that they decay path was at most a few millimetres. To measure this range fast and with high spatial resolution vertex detectors were in need. The bubble chambers were not able to handle large data rates, gaseous detectors were fast but not enough precise. Physicist started to look into solid state technologies, which were developing rapidly. In the 1980's research and development in the field of semiconductor detectors and Very Large Scale Integration (VLSI) readout [18] gain rapid importance for tracking and reconstruction of particles in HEP experiments. Thanks to the planar process introduced by J. Kemmer [19], silicon detectors were fabricated to provide the required speed and good spatial resolution. High quality detectors were developed after replacing the surface barrier technology [20] with planar process [19]. For tracking, the importance of semiconductor detectors was realised by the high-energy physics community when the planar silicon diodes were used in a fixed target experiment. The silicon strip detectors as well as Charge Coupled Detector (CCD) pixel detectors were used by the experiments NA11/NA32 at CERN in 1981-82 [21, 22, 23] for particle tracking and the measurements of vertices of short-lived particles. Since more than 30 years the favourite technologies for researchers in HEP experiments are semiconductor and gaseous detector.

In this chapter the importance of developing monolithic pixel detector and its application in HEP experiments are discussed. Various silicon detectors will be described and the advantages of SOI monolithic pixel detector over other silicon detector technologies will be presented.

1.1 Physics motivation

Particle physics is a study of interaction of subatomic particles such as electrons, protons or positrons. Due to new challenges in particle physics, many new projects and upgrades are being planned for HEP experiments. The essential component in HEP experiment is the detector system, in particular the tracker. The main aim of detector systems is to track particles taking part in the interaction and to determine their various parameters, such as the origin, direction, charge, momentum, energy and mass, and for short lived particles the production and decay vertex. All the mentioned quantities cannot be measured by one detector, therefore a specialised sub-detectors are joined together to form a detector system. The detector system is a combination of different detectors to reconstruct primary and secondary vertices and particle identification.

To exploit the detector system for use in HEP experiments it should have high granularity, fast readout, radiation hard, work with higher occupancy, have good impact resolution, low material budget, and low cost. However, the goal of several HEP experiments are different and have their own specifications and requirements for tracking detector. Nevertheless, the requirement toward optimal detector for HEP experiments must have high level of radiation hardness (see table 1.1), high resolution in the order of few microns, high read-out speed, and low power consumption. All should be achieved with low cost.

The following table 1.1 shows the radiation levels needed in different HEP experiments [24]:

Table 1.1: Radiation levels in different HEP experiments.

Experiment	TID (kGy)	Fluence 1 MeV(n_{eq}/cm^2)	Time (years)
ATLAS	500	1 x 10^{15}	10
CMS	840	3 x 10^{15}	10
ALICE	2.7	1 x 10^{13}	10
LHCb	50	1.3 x 10^{14}	1
STAR	1.5	3 x 10^{12}	1
Belle II	19	1.2 x 10^{13}	1

The progress in the development of monolithic pixel detectors (1.2.4) makes them very good candidates to be included in the future trackers close to the interaction point.

1.1.1 Detector System

To track the particles and to measure their momentum, detectors are necessary to be placed around the interaction point inside a magnetic filed. When the particle interacts

with detector material, a fraction of energy is deposited in the detector material, generating an electrical signal, and the position of the particle can be measured. To reconstruct the particles trajectory several position measurement are used. Figure 1.1 (left) shows the deflection of the particle in the presence of magnetic field. The particle trajectory is curved since the detector system is immersed in the magnet. The radius of curvature and deflection of the particle determine the magnitude of transverse momentum and its charge sign respectively. Figure 1.1 (right) represent the particle track curvature with several hits and its measurement of transverse momentum.

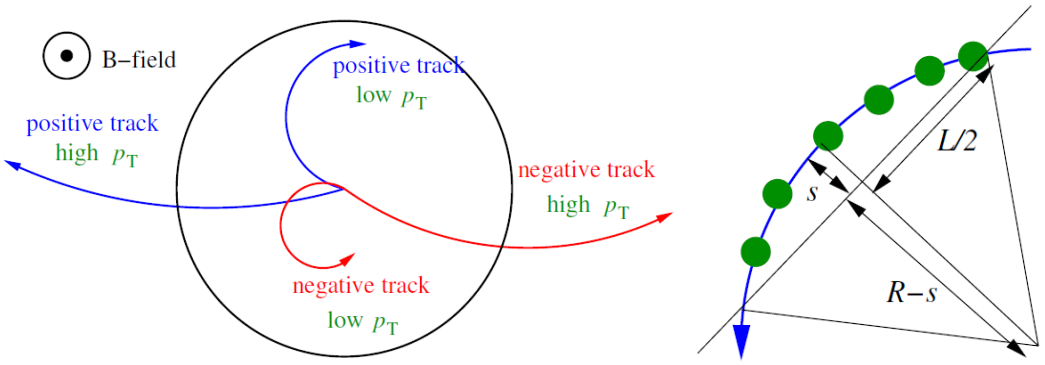

FIGURE 1.1: The deflection of particle track due to a perpendicular magnetic filed (left) and its measurement (right). After [25].

The transverse momentum of the charged particle can be calculated as [25]:

$$p_T = \frac{0.3BL^2}{8s}, \tag{1.1}$$

where p_T is transverse momentum, B is magnetic field and curvature radius (R) can be calculated with sagitta (s) and L is distance between planes.

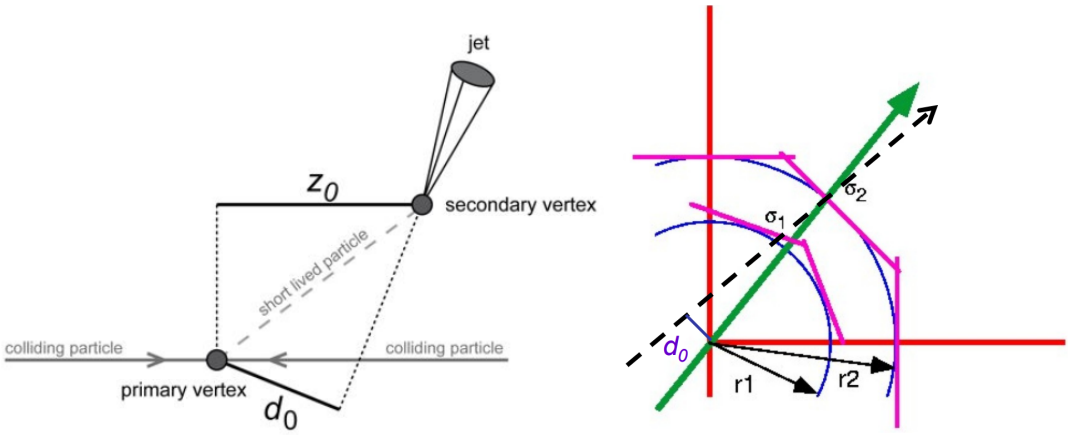

FIGURE 1.2: Illustration of impact parameters of short lived particle just a few μm (left) and simplified model of vertex detector to determine the impact parameter resolution (right). After [26, 27].

To determine the decay point of short living particles like baryons (Λ) or mesons (D, B), vertex detectors are used. The vertex detector is placed very close to the interaction point to precisely measure the vertex position, impact parameter and to reconstruct secondary vertices. Figure 1.2 (left) shows the primary vertex at the particle interaction and short lived particle decay into daughter particles before it reaches the detector. The secondary vertices can be determined by reconstructing the charged tracks left by daughter particles. The track parameters such as transversal impact parameter (d_0) and longitudinal impact parameter (z_0) can be determined using track fitting techniques (Least squares estimation and Kalman filter) [28].

The impact parameter resolution (σ_{d0}) based on geometry can be derived by considering a simplified case of vertex detector with two measurement layers, shown in figure 1.2 (right) [25].

$$\sigma_{d0}^2 = \frac{r_2^2\sigma_1^2 + r_1^2\sigma_2^2}{(r_2 - r_1)^2}, \tag{1.2}$$

where the r1, r2 are radii of the two layers and σ_1, σ_2 are the intrinsic measurement errors.

The multiple scattering of particles, whilst interacting with detector material, is one of the most important factor to be considered, as it degrades the precision of the impact parameter resolution. The best precision can be achieved with small radius (r) and minimum thickness (x). Equation 1.3 shows how the resolution depends on the detector geometry, material thickness ($\frac{X}{X_0}$ radiation lengths), and momenta of particles p [25].

$$\sigma_{d0} = \sqrt{\frac{r_2^2\sigma_1^2 + r_1^2\sigma_2^2}{(r_2 - r_1)^2}} \oplus \frac{r}{psin^{3/2}\theta} 13.6MeV\sqrt{\frac{X}{X_0}}, \tag{1.3}$$

Figure 1.3 shows how the impact parameter resolution depends on momenta. The four experiments at LHC have different geometry and design but all are expected to have excellent capabilities for heavy-flavour measurements [29].

1.1.2 Example of ALICE Inner Tracking System and its upgrade

Figure 1.4 shows a current Inner Tracking System (ITS) layout of ALICE. It consist of 6 concentric barrels which include three different technologies. First two innermost layers are built of hybrid Silicon Pixel Detectors (SPDs), middle layers are of Silicon Drift Detectors (SDDs) and two outer layers are made of double sided Silicon micro-Strip Detectors (SSDs). The momentum of the particle is determined by supplying ITS with

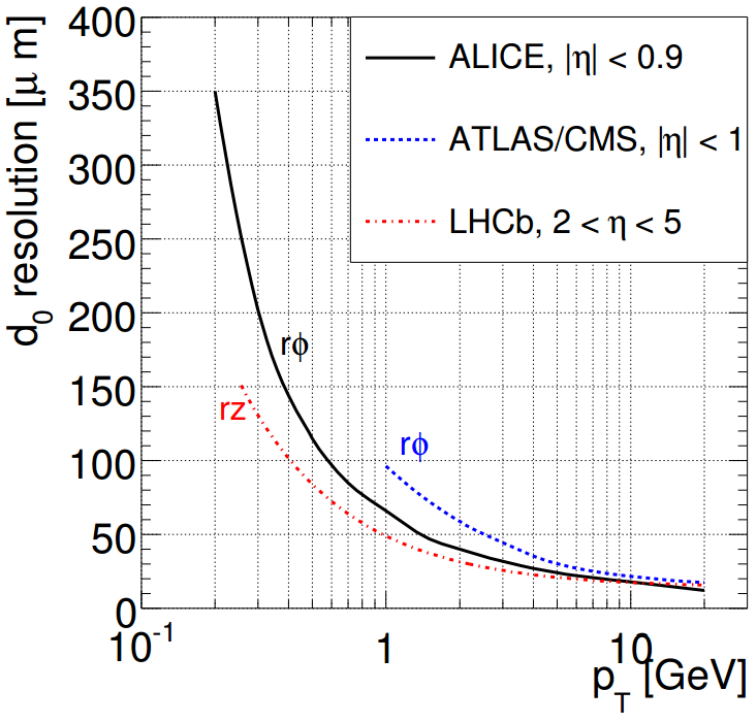

FIGURE 1.3: Track impact parameter resolution for the four LHC experiments. After [29].

magnet. If the charged particle travels inside a magnetic field it obtains spiral trajectory and the curvature of projected circle will be proportional to the transverse momentum. The impact parameter resolution of the present ALICE ITS is limited to 75 μm to study the charm and beauty mesons of transverse momentum above 1 GeV/c. However, the ALICE ITS requires to upgrade its detector system to study Λ_c baryons in heavy ion collisions, whose mean decay length ($c\tau$) is only 60 μm and heavy flavours of low p_T at maximum achievable readout rate [30]. To achieve the physics goals as outlined above, the frontier Monolithic Active Pixel Sensor (MAPS) technology is planned to be used in ITS upgrade of ALICE [31].

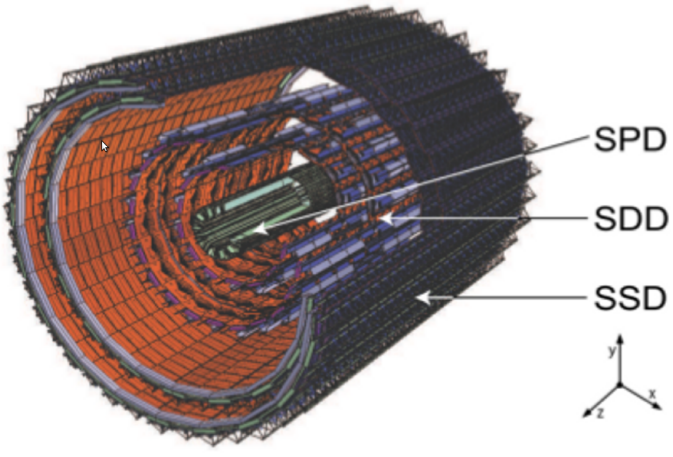

FIGURE 1.4: ITS layout of ALICE.

By building seven layers of MAPS instead of six layers of pixel detectors, the new ITS of ALICE will feature the following improvements [32]:

- **Improving impact parameter resolution:** Reduction of radial distance between the beam and first inner layer to 2.2 cm compared to present value of 3.9 cm, and reduction in layer thickness to 50 μm from 350 μm, will improve the track resolution by a factor of $\sim$ 3.
- **High Granularity:** The pixel density will be increased by implementing smaller pixel size 20 x 20 μm^2 instead of 50 x 425 μm^2, thanks to the MAPS technology the expected spatial resolution is 5 μm.
- **Material budget:** The use of MAPS results in low material budget for the inner barrel of upgraded ITS, 0.3 % of radiation length compared to 1.14 % in current ITS and for outer barrel 0.8 % of X_0 per layer.

The maturity level of monolithic pixel detector in CMOS technology has reached to a level to be used in tracking and vertex detectors. Beside ALICE upgrade, the monolithic sensors are already used in the vertex detector of the Solenoidal Tracker At RHIC (STAR) experiment at the Relativistic Heavy Ion Collider (RHIC) [33] and will be used in next long run of Belle II at KEK [34].

1.2 Semiconductor detectors in particle physics

The advantages of solid state detector medium comparing to gas-filled detector are; the dimension of detector is smaller, the densities are 1000 time greater [35] and the generation of free charge carriers needs lower ionisation energy (see table 1.2) [36]. In HEP, silicon detectors are considered over germanium due to higher resistivity, larger energy gap and lower leakage current at room temperature. The theory presented in this dissertation is based on standard books and articles [35, 36, 37, 38, 39].

TABLE 1.2: Energy needed to generate free charge carriers/ion pair/photons.

Detector	Ionisation Energy (eV)
Semiconductor	$\simeq$ 3
Gaseous	$\simeq$ 30
Scintillation	$\simeq$ 100

1.2.1 General concept of Silicon detectors

The applications of silicon detectors are broad. Silicon detectors can be used in digital cameras to detect light, in astrophysics to detect visible and infrared light, gamma and X-rays, in particle physics to detect charged particles and in many other fields of science and technology. The silicon detectors for HEP applications are discussed in this dissertation. The highest probability to find silicon detector is in tracking chamber. These detectors are basically ionisation chambers. The basic working principle of silicon detector is shown in figure 1.5. A voltage is applied between a pair of electrodes to built an electric field in the detection volume. When the photon or ionising particle pass through this medium it liberates charge pairs and their number is proportional to absorbed energy of the particle. These charge carriers drift under the influence of electric field towards the nearest electrode and induce a current in the external circuit. The position information of the ionising particle can be deduced by segmenting the electrode. The signal measured at a given electrode represents the position information of the particle. The detector volume can be realised by joining n-type bulk silicon material with a shallow p-type silicon material on the surface. This arrangement is known as p-n diode. In more complex design the p-n diodes are segmented into strips or pixels. These detectors will be discussed in next sections.

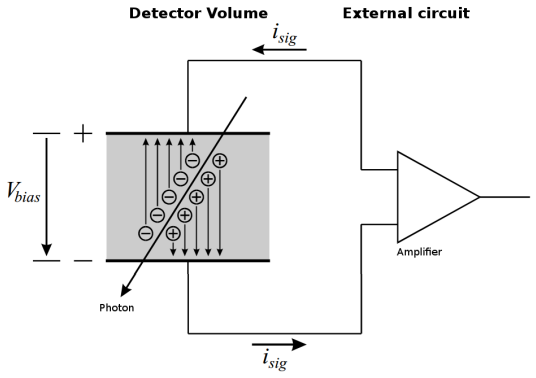

FIGURE 1.5: Charge collection concept.

Signal formation in silicon sensors

When an ionising particle traverses through the sensitive volume of the sensor free charge carriers are generated. The drift of charge carriers in the electric field induces a current pulse at the collecting electrodes and stimulates the current flow instantaneously. The current flow stops when the whole charge is collected and the total time is known as charge collection time. The change in the induced charge on the electrode is observed when the free charge carriers move through the sensor resulting in induced current. The measurement of induced charge is not possible directly, however it can be observed

indirectly by integrating the induced current. The derivation for the induced current is elegantly formulated by Ramo's theorem [40]. The magnitude of instantaneous induced current can be calculated using the following expression:

$$i = q\vec{v}\vec{E_Q}, \tag{1.4}$$

where i is instantaneous induced current for a charge q which moves with velocity $\vec{v}$ in the applied electric field, and $\vec{E_Q}$ is weighting field. The weighting filed is determined by setting the specific electrode potential to one and all other electrodes potential to zero [37]. Note that the weighting field depends only on geometry and is distinctly different from electric field.

1.2.2 Strip detectors

As discussed previously, silicon strip detectors are widely used as precise tracking detectors. The basic working principle of silicon strip detector is illustrated in figure 1.6. At the surface of n-type silicon bulk a highly doped p^+-type silicon is implanted to produce a p^+-n junction. Strips are formed by segmenting p^+ implants. An external reverse bias voltage is applied to p^+n junction to deplete the sensor. The electron-hole pairs are created when an ionising particle traverses the depleted region. The charges drift in electric field and the signal at the electrode is induced which is further processed by the readout chip. To utilise the full depth of the n-type silicon bulk, it is necessary to fully deplete the detector region by applying high enough reverse bias voltage. The position of the ionising particle can be identified based on which strip the charge is collected. Each strip exhibit small reverse bias current (DC current). The amplifiers in the readout chip should be protected from this DC current. A large capacitor is incorporated between p^+ implant and the amplifier to block DC fraction of current and allow AC signal. These capacitors are produced by deposition of isolator layer (SiO_2) with a thickness of 100–200 nm between strip (p^+ implant) and aluminium, see figure 1.6 ([41]). The quality of dielectric can be increased by using second layer of Si_4N_4.

In practise the minimum pitch of strip between 20 and 50 μm can be achieved and the length of the strip is the full length of the sensor. As a result only 1-Dimensional (1-D) information about the ionising particle can be obtained. In simple case the geometry of the electrode can be used to determined the position resolution. It is given as pitch/$\sqrt{12}$, for binary readout, when the charged particle hits single strip. However due to several reasons such as capacitive coupling, diffusion, and inclined tracks, the signal is distributed over several strips. The analogue information of several strips is exploited to determine

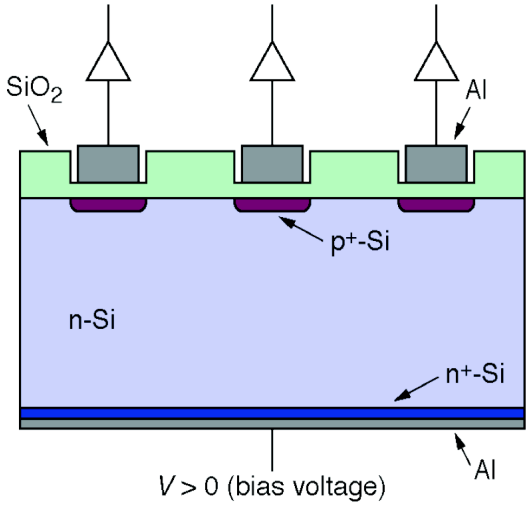

FIGURE 1.6: Schematics showing a single-sided AC coupled silicon strip detector. After [42]

the improved position resolution by interpolation [39]. A Double-sided Silicon micro-Strip Detector (DSSD) were also designed by segmenting both sides of n-type silicon bulk with p^+ and n^+ implants, see figure 1.7 ([43]). It was developed by Detector with Lepton, Photon and Hadron Identification (DELPHI) collaboration. Beside many benefits such as 2-Dimensional (2-D) readout and material budget, this design has additional problems. Three main limitations of DSSD are; it needs p-stop, p-spray techniques for insulation of n-side electrodes, detection of ghost hits at high particle occupancy, and very complicated design .

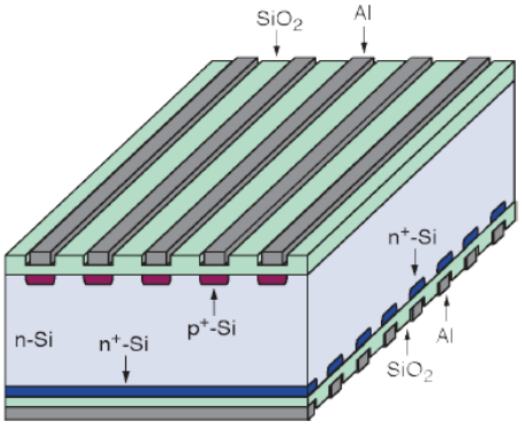

FIGURE 1.7: Schematics showing a double-sided silicon strip detector. After [42]

1.2.3 Pixel detectors

In the field of electronic imaging sensors, CCDs have been the leader because of its better resolution and image quality. The CCD has a long historical link together with microstrip

detectors in providing few μm level tracking precision for the detection of short-living charm particles. The microstrip detectors found more extensive application particularly to measure lifetime and mass of the charm mesons. However CCDs can be used for vertex detection where fast readout response is not needed and other experimental conditions are appropriate, such as rare events and low background. For more detail description of CCD as vertex detector, readers are refer to [44, 45]. Since the task and requirements of vertex detectors are more and more demanding in terms of material budget, spatial resolution, high speed, radiation hardness, and low cost, in last years the interest of physics community has dramatically increased towards CMOS technology.

Presently most pixel detectors in the field of HEP use the CMOS technology. The strips are segmented along their length to small sensing element shaped rectangular or quadratic named as pixel. This process increases the number of sensing elements in a pixel detector which is of the order of 10^3 - 10^4 channels. Consequently, the connection of pixels to readout electronics is not possible with a low-cost mature ultrasonic wire bonding [46]. The solution is to sandwich a readout electronics on top of the sensor using "bump bond [47, 48] techniques and this process is known as hybridisation. The small change in the segmentation of strips into pixels offers 2-D readout with some consequences. The following are the three main consequences for hybridisation [49]:

- Vertical connection between pixel sensor and readout chip,
- Exact matching between the size of pixel and the size of readout chip channel,
- Readout must be very close to the pixel sensor.

In hybrid pixel detector, a high resistivity-depleted sensor is connected to a low resistivity readout chip realised in standard CMOS technology via bump bonding, see figure 1.8. The p-n junctions are formed by introducing a p^+ implant (diode-implant) in a n-type substrate (doped silicon). The size of readout chip and sensor must be the same and the distribution of readout cells must be the same as the pixels implants in the sensor. The pitch of pixels is very small, in the order of 100 μm. In 100 nm CMOS technology the pixel size could be as small as 10 x 80 μm^2 or 25x25 μm^2 for a square geometry [49]. The bump bonding limits the pixel pitch to about 10–15 μm and the smallest pitch obtained so far is 15 μm [50].

In HEP experiments pixel detector is the technology of choice for next generation at fixed target and colliding beam experiments. Pixel detectors were first used in WA97 [51] and DELPHI [52] experiments for the reconstruction of tracks in vertex detector. The need for larger area detector can be fulfilled by pixel detectors. However the present availability of industrial processes and bonding technology are limited to meet the requirements of

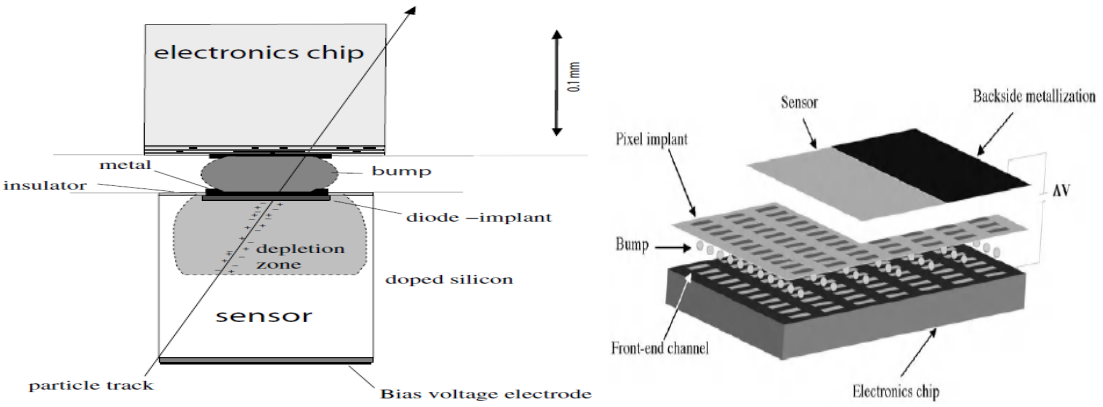

FIGURE 1.8: Schematic view of one pixel cell and a hybrid pixel detector. After [49].

future HEP experiments. The demands of smaller pixels, lower material budget and high speeds are in particular some of the drawbacks of hybrid pixel detectors.

1.2.4 Monolithic pixel detectors

To overcome the drawbacks of hybridisation process, the idea of implementing both sensor and readout in single technological process is favoured by many research groups. Silicon was chosen as base material by the developers to find the possibility of monolithic rather than hybrid because of its availability and physic characteristics. Today, the development in monolithic detectors is promising and adopted by most of the future HEP experiments.

The CMOS pixel sensor can be realised in two ways: Passive Pixel Sensor (PPS) and Active Pixel Sensor (APS). In PPS there are no amplifiers in the pixels, each pixel contains a photo-diode to convert photons to electric signal and a selection switches, which connect photo-diodes to readout line. In case of APS each pixel is integrated with an amplifier and it buffers the signal from ionising particles. Due to several advantages of APS as discussed by R. Turchetta [53], the monolithic detectors contain APS as pixel sensor. Since 1990's several attempts were made in the process of developing monolithic pixel detector [53, 54, 55, 56]. Some of the promising technologies are listed below:

- Monolithic Active Pixel Sensor (MAPS) and Depleted Monolithic Active Pixel Sensor (DMAPS)
- High Voltage CMOS (HV-CMOS)
- DEPleted Field Effect Transistor (DEPFET)
- Silicon On Insulator (SOI)

MAPS and DMAPS

The cross section of MAPS is shown in figure 1.9. The detection medium is realised in a lightly doped p-type EPItaxial (EPI) silicon layer (thickness in order of 15 – 20 μm) on top of a low resistivity highly doped p^{++} substrate. The n-well and p-type EPI layer act as p-n junction. The generated electron-hole pair by Minimum Ionising Particle (MIP) in the un-depleted EPI layer is transferred to n-well through thermal diffusion of charge carriers and thus the charge collection time is long ($\sim$ 100 ns). In the EPI layer $\sim$ 80 e-h/μm per MIP are produce. The presence of potential barrier between handle substrate/p-well and EPI layer deflects electrons and guide towards the n-well of the diode. Each pixel is equipped with a simple three transistor circuit for amplification and selection of respective pixel. The position resolution of this detector is good because of small pixel size (10 x 10 μm^2) possible [53]. Other advantages are low power consumption, reduced material budget and minimal multiple scattering by the substrate thinned down to 50 μm. The disadvantages of MAPS are slow and unordered charge collection by thermal diffusion and that only NMOS transistors can be used for the electronic part, what limits the complexity of the circuits. However latter can be solved by using deep p-well process [57], which allows fabricating the P-type Metal-Oxide-Semiconductor (PMOS) transistors in active area and former can be solved by using high resistivity partially depleted EPI layer.

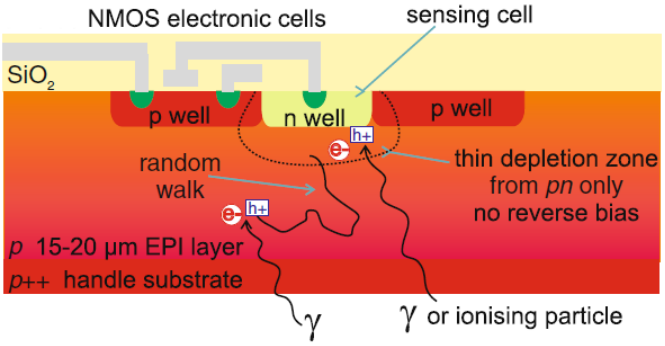

FIGURE 1.9: Schematic view of one pixel cell of a MAPS. After [38].

The CMOS process with high resistive partially depleted EPI layer and deep p-well is shown in figure 1.10. The resistivity of EPI layer $>$ 1 kΩcm (high resistivity thin EPI layer) is used as active volume. The depletion region can be increased to several micrometres by applying small voltage at n-well of p-n junction, however the detector is partially depleted. A deep p-well is implanted underneath a n-well for the fabrication of PMOS transistors. This kind of CMOS process was developed in a commercially available XFAB-0.6 technology. The performance of high resistivity and low resistivity EPI layers can be compared from the test results of prototype chips MIMOSA[1]-25 and

[1]MIMOSA stands for Minimum Ionising particle MOS Active pixel sensors.

MIMOSA-15 respectively [58]. The charge collection of high resistivity EPI layer is two times higher and yields higher Signal to Noise Ratio (SNR) than that of low resistivity EPI layer.

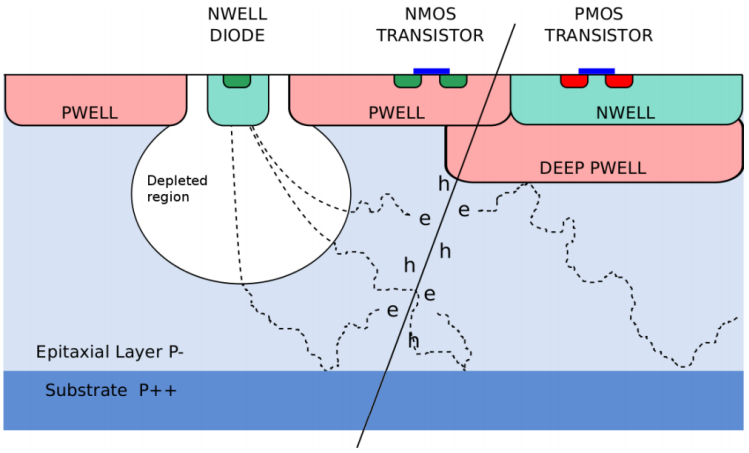

FIGURE 1.10: Schematic view of one pixel cell of a deep p-well with high resistivity partially depleted EPI layer. After [59].

The Depleted Monolithic Active Pixel Sensor (DMAPS) is another concept based on the idea of MAPS. Figure 1.11 shows the cross section view of single pixel. The DMAPS consist of high resistivity n-type silicon (bulk) acting as detection medium and n-well is implanted in the bulk to work as charge collection electrode. However, n-well do not form p-n junction, rather they form an electric drift field in the depleted bulk by creating regions with high electric potentials. The deep p-well (p-substrate) is implanted in the bulk for the integration of CMOS circuitry. Transistors are fabricated in the deep n-well, which allow setting the potential of p-substrate independently. The depletion region is formed at the boundaries of bulk-backplane and bulk-p-substrate. The main features of this process are fast signal collection by drift, large signal about 4000 electron per MIP and small sensor capacitance [60].

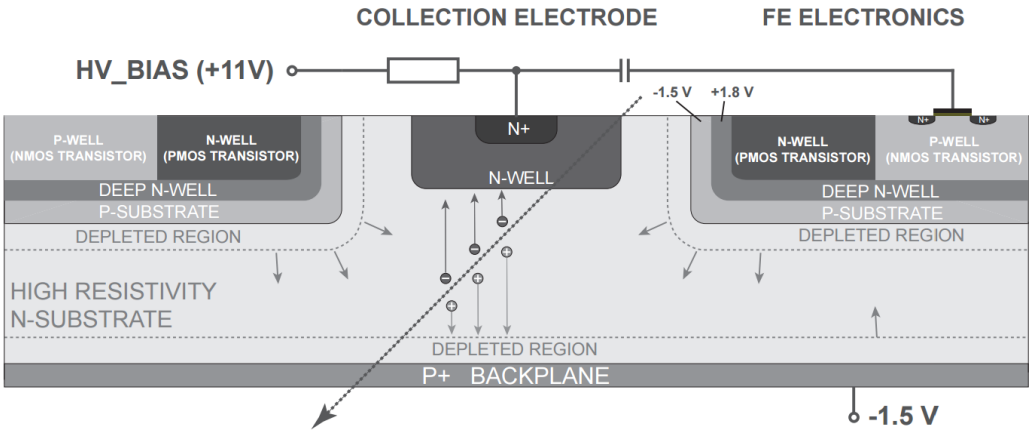

FIGURE 1.11: Schematic view of one pixel cell of a DMAPS. After [60].

HV-CMOS

The High Voltage CMOS (HV-CMOS) is yet another approach to a monolithic pixel detector which allows to use any deep sub-micron CMOS technology featuring twin-well option and avoid relying on EPI layer. The schematic view of single pixel is shown in figure 1.12. The deep n-well is used as signal collecting electrode and the substrate for the CMOS electronics. It is implanted and reverse biassed with respect to the p-substrate. Most of the HV-CMOS detectors are designed in AMS[2] 350 nm HVCMOS-process. The typical reverse bias voltage in this technology is 60-100 V resulting in about 15 μm of depletion thickness with a substrate resistivity of about 20 Ωcm and fast charge collection time ($\sim$ 200 ps). The HV-CMOS detectors allow implementation of thin, low cost, high time resolution, and radiation tolerant detectors [61].

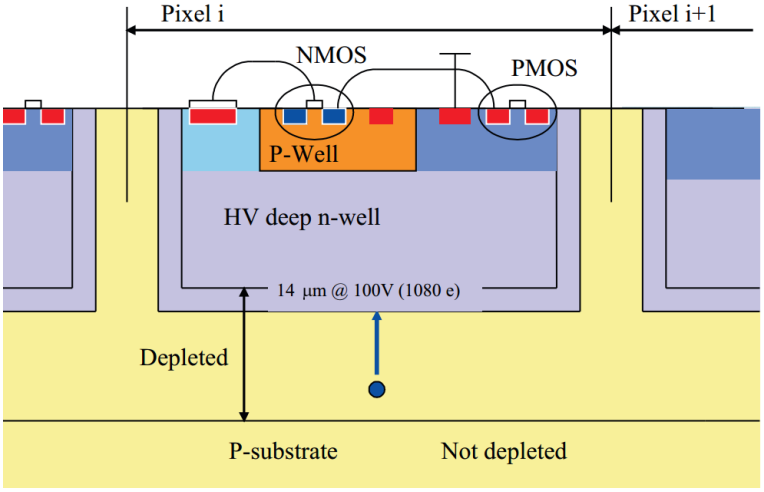

FIGURE 1.12: Schematic view of one pixel cell of a HV-CMOS. After [62].

The development of HV-CMOS technology opened a new alternative to produce bumpless hybrid pixel-detector known as Capacitive Coupled Pixel Detector (CCPD) implemented in CMOS technology. The CMOS electronic layer of HV-CMOS detector contains a Charge Sensitive Amplifier (CSA). The output voltage of CSA is connected to the electrode placed at last metal layer. The readout electronics chip is glued to the HV-CMOS detector chip in such a way that a capacitor is form between HV-CMOS electrode and the readout input pad, see figure 1.13. The depletion zone can be extended to 15 μm by applying 60 V bias voltage. When MIP traverses through the depleted layer it generates about 1080 electron-hole pairs. This low signal is amplified directly in the pixel and transmitted to the readout chip using capacitive AC coupling. Several advantages such as high bulk and CMOS electronic radiation hardness, no bump bonding, low material budget, and low cost for the tracking application can be obtained by placing HV-CMOS

[2] Austria Micro Systems

together with capacitive coupling. Beside these advantages the sensor consumes large power [63].

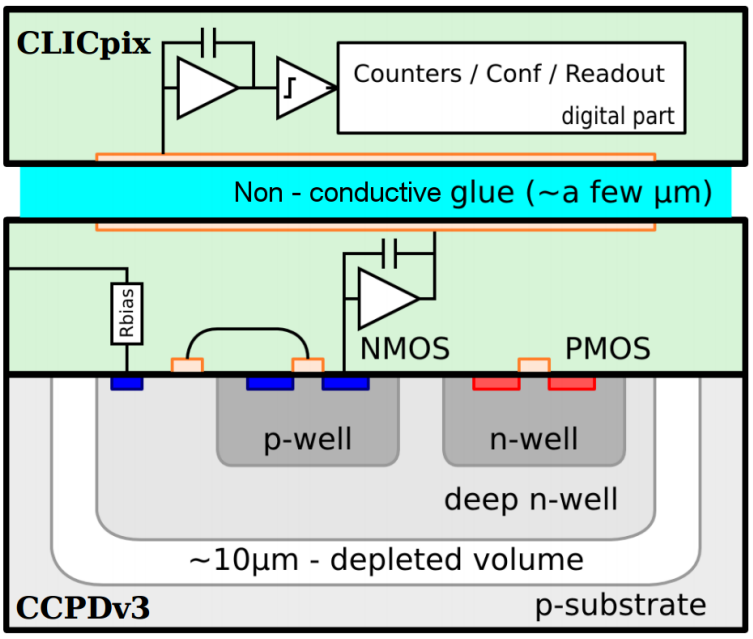

FIGURE 1.13: Schematic view of one pixel cell of a CCPD. After [64].

DEPFET

The DEPleted Field Effect Transistor (DEPFET) is another monolithic detector concept proposed by Kemmer and Lutz in 1987 [65]. In early 90's the first CMOS readout electronics was processed on a fully depleted sensor substrate (refer to [66]). The principle of operation of DEPFET detector is shown in figure 1.14. An amplifying transistor (Metal Oxide Semiconductor Field Effect Transistor (MOSFET) or a Junction gate Field-Effect Transistor (JFET)) is integrated onto a high-resistivity silicon substrate. Underneath the transistor a potential minimum for electrons is created by means of an additional n-implant and it is an internal gate of the transistor. From the generated electron-hole pairs in the fully depleted silicon substrate, electrons are collected and stored in the internal gate and holes drift to the p+ implant at the back side of the detector. The electrons accumulated in the internal gate cause changes in the transistor current. Since the capacitance of internal gate is very small of the order of 10 fF, it leads to a low noise operation. Because of fully depleted operation this technology produces large signal and short charge collection time. In the readout operation only the active rows dissipate power while all other pixels are switched off. But still they are sensitive to the charged particles. This approach results in low power consumption. The fabrication process of DEPFET is complicated and expensive.

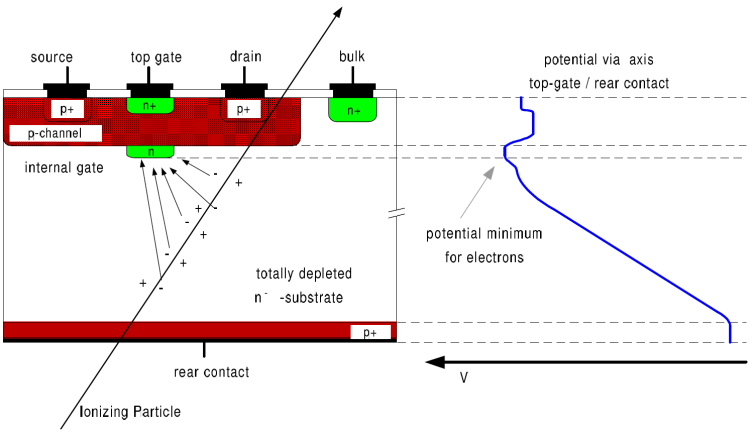

FIGURE 1.14: Schematic view of one pixel cell of a DEPFET. After [67].

1.2.5 SOI Pixel detectors

The trend of Bulk CMOS technology makes conventional scaling less feasible while the demand for high speed and low power Large Scale Integration (LSI) circuits is continuously high [68]. After incubated for more than 20 years, the SOI CMOS technology is a promising candidate to overcome these fundamental limits of scaling [69]. The SOI pixel detector is a novel detector towards a monolithic pixel detector. The SOI technology is based on connecting CMOS circuit with sensor part using wafer bonding process. This technology allows to use thick high resistivity silicon and thin low resistivity silicon on the same processed wafer [70]. The development of first monolithic SOI pixel detectors started with Silicon Ultra fast Cameras In Medical Application (SUCIMA) project in 2001 [71] with the collaboration of Institute of Electron Technology (ITE) in Warsaw, AGH University of Science and Technology and Institute of Nuclear Physics in Krakow, and several other institutes. In 2005 the collaboration of KEK and OKI Electric industry in Japan made use of a commercial SOI process for detector prototypes. Presently the KEK detector technology development known as Silicon On Insulator PIXel detectors (SOIPIX) [72] is carried on and since 2005 many different designs and prototypes in the SOI technology have been produced.

Figure 1.15 shows the cross section view of SOI detector. A Buried OXide (BOX) layer ($\sim$ 200 nm thick) is used as an insulator (SiO_2) between a thick high resistivity silicon substrate (sensor part) and a thin low resistivity silicon (electronic part). The pixels are formed by implanting an opposite heavy doped material below BOX layer. The sensor part can be depleted by applying reverse bias voltage to backside of the sensor. The p-n junction is formed between the p^+ implant and the sensor substrate. If charged particle traverses through the depleted zone of sensor part, the generated electron-hole pairs drift in electric field and their signal is processed in the CMOS circuitry. High resistivity wafer (i.e. sensor part) can be thinned down to 50 μm - 100 μm using TAIKO process [74]

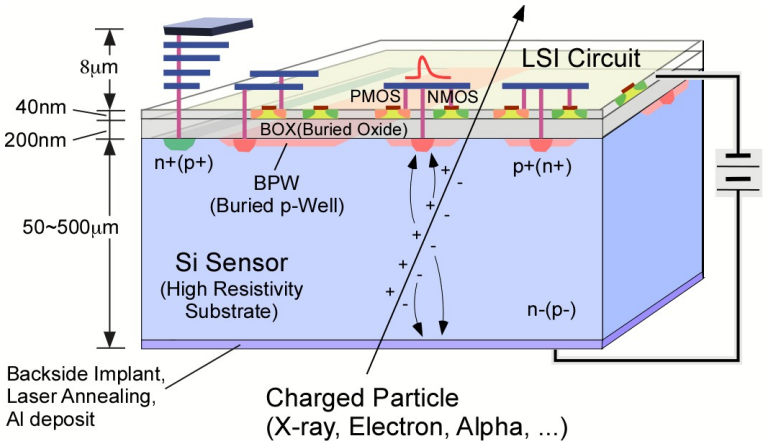

FIGURE 1.15: Schematic view of one pixel cell of a SOI detector. After [73].

to reduce material budget and also allowing for lower biassing voltages. The details of SOI 200 nm CMOS process specifications are listed in table 1.3. The Fully Depleted SOI (FD-SOI) detector can be realised on three sensor wafers i.e. CZ-n, FZ-n and FZ-p.

TABLE 1.3: LAPIS semiconductor FD-SOI Process Specification.

Process	200 nm Low-Leakage Fully-Depleted SOI CMOS 1 Poly, 5 Metal layers. MIM Capaitor (1.5 fF/μm^2), DMOS Core (I/O) Voltage = 1.8 (3.3) V
SOI wafer (SOITEC)	Diameter: 200 mmϕ, 720 μm thick Top Si: CZ-p, ~18 Ω cm, ~40 nm thick Buried Oxide: 200 nm thick
Sensors	Cz-n = ~0.7 kΩ cm, thickness = 250 μm FZ-n = ~2 kΩ cm, thickness = 500 μm FZ-p = ~7 kΩcm, thickness = 500 μm
Backside process	Mechanical Grind, Chemical Etching, Back side Implant, Laser Annealing and Al plating

The major drawback of other monolithic technologies have been overcome in SOI CMOS technology. Those are: 100 % fill factor [75], complex CMOS circuitry in the pixel is possible with NMOS, PMOS, and Depletion type Metal-Oxide-Semiconductor (DMOS) transistor, and Metal Insulator Metal (MIM) capacitor, large signal and short collection time due to sensor operation in a full depletion mode. The other advantages of SOI technology are listed below:

- Since it is a monolithic technology no mechanical bump bonding is required, which minimises multiple scattering, gives low material budget, low cost, and feasibility to design smaller pixel size. At present smallest pixel size achieved in SOI technology is 8 μm [76]. Smaller pixel size results in high resolution.

- The parasitic capacitance of sensing node is small, yielding a large conversion gain (V=q/C) and low noise.
- The SOI CMOS circuitry have less parasitic capacitance and smaller leakage current due to smaller layout area comparing to bulk CMOS circuitry. The CMOS circuitry is built on thin low resistive SOI layer, which helps to speed up the circuitry and consume less power.
- Immune to 'latch-up' and Single Event Effect (SEE) problems, since the top silicon layer (CMOS circuitry) is isolated from bulk silicon layer (detection volume) by BOX layer (thin oxide). This arrangement helps to put transistors close together.
- No leakage path from the CMOS circuitry to detection volume, so low to high temperature operation is possible (4 K - 600 K) [77].
- 3-Dimensional (3-D) vertical integration is possible by using μ-bump technology [78]. Thus complex logic and memory can be implement inside the pixel with smaller pixel size.
- SOI CMOS technology is based on Industrial standard. So additional growth in the development and low cost is expected.

The back gate effect was observed in the first prototype of SOI detector designed at KEK [79]. This effect present a serious challenge to SOI technology due to the change of transistors threshold while applying detector bias voltage. This effect was mitigated by modifying the SOI process. One such solution is by placing lightly doped layer of the same type of pixel implant. In figure 1.15 a Buried P-Well (BPW) is connected to the pixel below BOX layer as a protecting layer [80]. This simple modification in the process resolved the back gate effect by shielding the sensor electric field but yield some drawbacks, increase of pixel capacitance and parasitic coupling between the electronics and the pixel. The solution to latter drawback has been discussed [81]. Another solution to back gate effect is Double-Silicon On Insulator (D-SOI) protection (see figure 1.16). It contains an additional thin silicon layer inside the BOX layer. This layer behaves similarly to BPW and in addition completely removes the drawback of increased pixel capacitance. The results obtain using D-SOI confirm the mitigation of back gate effect [82]. Other advantages of using D-SOI are suppressed crosstalk between electronic and sensor and the possibility of reduction of Total Ionisation Damage (TID) effect [83].

The targeted application fields of SOI CMOS technology are HEP, nuclear physics, medical physics, synchrotron radiation, and x-ray application for industries. The recent research and development in SOI CMOS technology has made impactful progress and

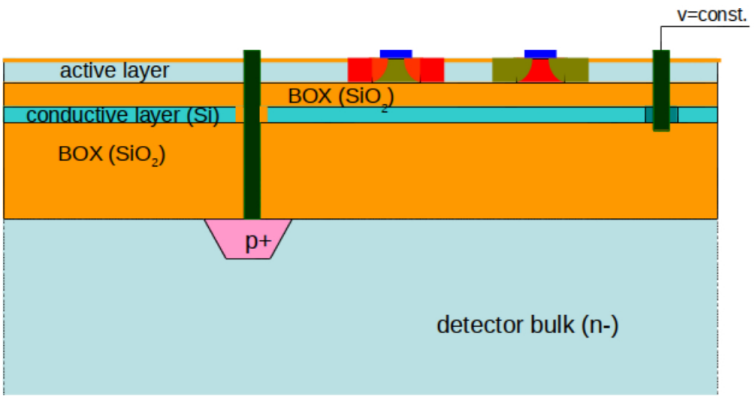

FIGURE 1.16: The concept of Double-SOI. After [84].

SOI CMOS become a promising technology for radiation applications. Among the challenges the SOI CMOS technology faced, the following are the issues which have been mitigated:

- The back gate effect was suppressed by BPW process. In this process a p-type dopant is implanted under the BOX layer at the sensor node to shield the sensor electric field. The doping level of sensor node is at least 3 order of magnitude larger than the BPW.
- In HEP application thin wafer is essential. Thanks to the TAIKO process provided by DISCO Corp. [85], wafer can be thinned down to 50 μm [86].
- High resistivity wafers are utilised to operate SOI detector at low detector bias voltage. Floating-zone wafer with resistivity of 7 kΩcm is successfully used in developing SOI pixel detector. The full depletion voltage for 500 μm wafer thickness is 80 V, refer section 4.3.2. Smaller full depletion voltage can be achieved by reducing the wafer thickness using TAIKO process.
- The advantages of using D-SOI process are: mitigation of back gate effect, increase of radiation tolerance (reduction of TID effect), and immunity to crosstalk between sensor node and CMOS circuitry. The recent results of D-SOI pixel detector are promising. The pixel sensor irradiated to 100 kGy recovered its functionality by applying a bias to the D-SOI electrode [83].

Chapter 2

SOI Detector Simulation

This chapter presents basics theory of semiconductor device physics and equations used for TCAD simulations [87]. It also includes brief discussion on how to use the tools available in TCAD simulation software, mainly ENEXSS. Lastly, the design and simulations results of DIPIX2 detector will be presented. In this work the TCAD simulations are performed to study the back gate effect (refer 1.2.5) and its influence on the characteristic of transistors and electric field in the detector.

In the past few decades the boost in technology took place at an extremely fast pace. The semiconductor technology is the fastest growing technology and its applications are global. The structure of the semiconductor industry is like a pyramid, see figure 2.1. Lower level is the wafer and Electronic Design Automation (EDA) tools followed by device engineering, design, manufacturing, software development and final product. The top level (final product) of the pyramid requires lower levels (wafer, EDA tool and device engineering) to function properly. So the lower level of the pyramid is the backbone of the final product. Computer aided design in the semiconductor industry is known as Technology Computer Aided Design. TCAD is a part of EDA tool. TCAD tools are mostly used in the lower level and the next level of the pyramid to understand the process of the device and the device physics. It helps in measuring the immeasurable parameters of the device without fabrication. A virtual prototyping (without fabricating real prototype) is possible using TCAD. This helps designer to solve the issues present in the previous design and also to predict the device properties under different operating conditions. Several institutes came up with TCAD software but its was first founded by the research group of Prof. Robert W. Dutton at Stanford university in 1977. In last 37 years TCAD software become more mature and available with many distinguished features and presently it is one of the most commonly used tools in semiconductor industries. In these years different research groups in collaboration with semiconductor

industry came up with their own TCAD simulators but in time some of them merged. For example: Technology Modelling Associates (TMA) merged into Synopsys [88] in 2001 and Integrated Systems Engineering (ISE) merged into Synopsys in 2004 [89]. On the other hand Silvaco [90] acquired licence of TCAD simulation software from Stanford university and developed a commercial alternative such as ATHENA [91] and ATLAS [92]. Beside Synopsys and Silvaco, ENEXSS TCAD simulation project was started in Japan. An association known as SEmiconductor Leading Edge TEchnology (SELETE) was established in 1994, founded as a voluntary organisation by ten Japanese semiconductor manufacturers [93]. This group had started in 1996 and the project ENEXSS was ended in 2011. Presently Synopsys possess more than 85 % of the whole TCAD market share, which make it close to monopoly [94].

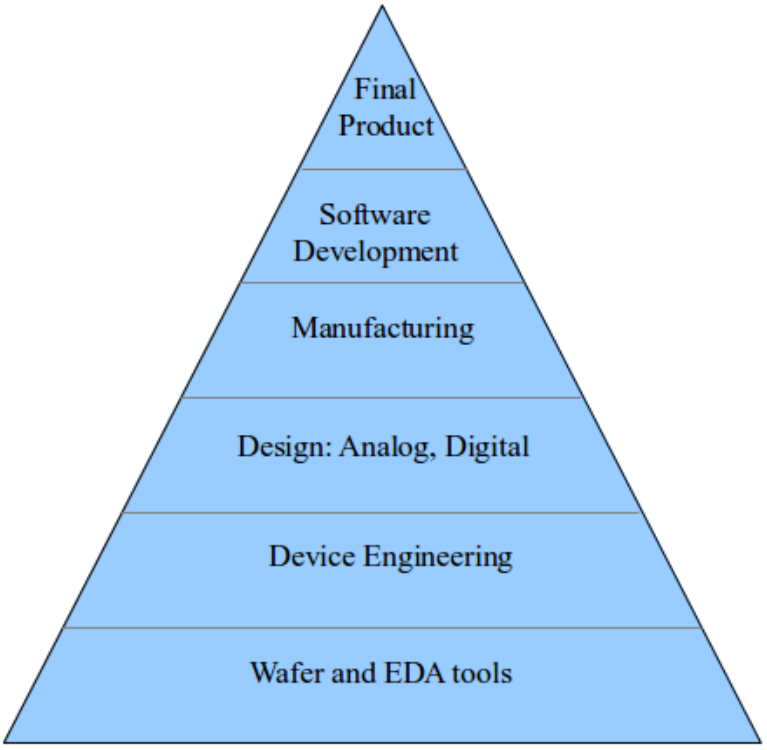

FIGURE 2.1: Pyramid of the semiconductor industry. After [95].

2.1 Physics of semiconductor devices

Solid-state materials are classified into three classes : conductors, insulators, and semiconductors. The resistivity of conductor is $<10^{-2}$ Ω cm, for insulator it is $>10^{5}$ Ω cm and in between there are semiconductors. Semiconductor is a most important material for electronic applications and it is classified into two categories; elemental and compound semiconductors. In periodic table the elemental semiconductors are available in group

IV and they have four valance electrons. From this group only silicon and germanium are treated as intrinsic semiconductors in solid state electronics, because the properties of these materials are relevant for electronic applications. The special combination of elements from group III and V are compound semiconductors. In this category there are many other possible compound semiconductors, refer textbook [96]. Gallium arsenide is a compound semiconductor having good optical properties and used in high speed applications. The main core of this dissertation is silicon based detector and the basic electrical properties of this material are discussed, based on canonical material and textbooks ([35, 96, 97, 98, 99, 100, 101]).

2.1.1 Electrical properties of semiconductors

The atomic number of elemental silicon is 14 and it belongs to IVth group of periodic table with four valance electron. Each valance electron is involved in covalent-bond and crystallises in the diamond lattice structure. The energy bands are formed when the isolated silicon atoms are bring together. The bandgap (E_g) of silicon at temperature of 300 K is 1.12 eV. The formula for E_g is given by equation 2.1:

$$E_g = E_c - E_v, \tag{2.1}$$

where E_c is conduction band energy and E_v is valance band energy.

Semiconductor is said to be intrinsic or pure, when the concentration of electrons (n) in the conduction band is equal to the concentration of holes (p) in the valence band. The density of charge carriers is determined by the properties of the material (density of states function and the Fermi distribution) with no impurity atoms. The mathematical equations for the distribution of electrons in the conduction band and holes in the valence band are given in equation 2.2:

$$n(E) = g_c(E) f_F(E) \quad \text{and} \quad p(E) = g_v(E)[1 - f_F(E)], \tag{2.2}$$

Where $g_c(E)$ is the density of quantum states in the conduction band, $g_v(E)$ is the density of quantum states in valence band and $f_F(E)$ is the Fermi-Dirac probability function. The electron and hole concentration (n_o and p_o) at thermal-equilibrium can be calculated by integrating the equation 2.2 throughout the conduction and valence band energy. After applying Boltzmann approximation one gets an approximate formula:

$$n_o = N_c\, exp\left[\frac{-(E_c - E_F)}{k_B T}\right] \quad \text{and} \quad p_o = N_v\, exp\left[\frac{-(E_F - E_v)}{k_B T}\right], \tag{2.3}$$

where n_o is electron concentration, p_o is hole concentration, N_c is effective density of states in the conduction band, N_v is effective density of states in the valence band, k_B is Boltzmann constant, and T is absolute temperature. At $T = 300$ K, the value of N_c and N_v for silicon is 2.8 x 10^{19} cm^{-3} and 1.04 x 10^{19} cm^{-3} respectively. The product of electron and hole concentration in equation 2.3 yields:

$$n_o p_o = n_i^2 \text{ (in thermal equilibrium)}, \tag{2.4}$$

For silicon the commonly accepted value for n_i is of the order of 10^{10} cm^{-3}.

Extrinsic semiconductors are produced by introducing dopant or impurity atoms in the crystal and it results in additional energy levels in the energy gap. The doping process is a controlled procedure and can change the electrical characteristics of the semiconductor. If the doping atom is donor (example Phosphorous (P)) it adds electron to the conduction band and it is called n-type semiconductor. If the doping atom is acceptor (example Boron (B)) it adds hole to the valance band and it is called p-type semiconductor. The energy required to transport electron/hole into the conduction/valance band is referred as ionisation energy. Equation 2.4 is valid for extrinsic semiconductor but for n-type material $n_o > p_o$ and for p-type material $p_o > n_o$.

To understand the electrical properties of semiconductor, it is important to know the densities of charge carriers (electrons and holes). The movement of free carriers in the semiconductor is possible due to external electric filed (drift) or because of concentration gradient (diffusion) and this process is called carrier transport. Since the charge carriers are not associated with lattice they are basically free carriers. They scatter in all directions due to thermal vibrations, doping atoms and defects within the lattice. For silicon the thermal velocity of electron is $\sim 10^7$ cm/s at T = 300 K. The average distance between collisions is called the mean free path and typical value is $\sim$ 100 nm, and the average time between collisions is called the mean free time (τ) and its typical value is about 10 $^{-12}$ s.

The average displacement of free carriers due to random motion in the absence of an electric field is zero. If an electric field is applied to the semiconductor the charge carrier will accelerate and move under the influence of electric field. The net drift of charge is known as drift current. The drift current density can be defined as the product of the volume charge density (ρ) and average drift velocity (υ_d). Equation 2.5 represents the electron and hole drift current density:

$$J_{ndrf} = qn\mu_n E \quad \text{and} \quad J_{pdrf} = qp\mu_p E, \tag{2.5}$$

where q is electronic charge, n is electron concentration, μ_n is electron mobility, μ_p hole mobility, and E is electric field (the product of mobility and electric field is average drift velocity and the product of electronic charge and electron concentration is volume charge density).

The transportation of free carriers from higher concentration to lower concentration leads to current component called the diffusion current. Its density is mathematically written as:

$$J_{ndif} = qD_n \frac{dn}{dx} \quad \text{and} \quad J_{pdif} = -qD_p \frac{dp}{dx}, \tag{2.6}$$

where D_n, D_p are the diffusion constants and $\frac{dn}{dx}$, $\frac{dp}{dx}$ are gradients of the carrier concentration.

The total current density is the sum of equation 2.5 and 2.6:

$$J_n = qn\mu_n E + qD_n \frac{dn}{dx} \quad \text{and} \quad J_p = qp\mu_p E - qD_p \frac{dp}{dx}, \tag{2.7}$$

The mobility and diffusion coefficient indicate the transport of charge carrier due to electric field and density gradient respectively. The relation between the mobility and diffusion coefficient in thermal equilibrium is:

$$D_{n,p} = \frac{k_B T}{q} \mu_{n,p}, \tag{2.8}$$

2.1.2 Basic equations

In device simulation the behaviour of real semiconductor device can be described by basic equations. Different modelling techniques have been used to describe the behaviour of device physics. The Drift Diffusion (DD) model is the simplest and widely used model in device simulation. It consists of a system of 5 partial differential equations of the standard semiconductor devices. The relation between the electrostatic potential ψ and the concentration of the electrons and holes is given by Poisson equation:

$$\frac{d^2\psi}{dx^2} = -\frac{\rho}{\varepsilon} = -\frac{q(n - p - N_D + N_A)}{\varepsilon}, \tag{2.9}$$

where ε is the isotropic dielectric permittivity which is material-dependent, n and p are the electrons and holes concentrations, and N_D, N_A is the doping concentration of donors and acceptors.

The current-density equations for steady-state condition contain two components: drift caused by applied electric field and diffusion caused by carrier concentration gradient (refer section 2.1.1). For a 1-D case, the current-density equation for electron and hole by using 2.7 and 2.8 is written as:

$$J_n = q\mu_n\left(nE + \frac{kT}{q}\frac{dn}{dx}\right), \tag{2.10}$$

$$J_p = q\mu_p\left(pE - \frac{kT}{q}\frac{dp}{dx}\right), \tag{2.11}$$

where J_n and J_p are the current densities of electrons and holes respectively. These equations are valid for the low electric fields. If the electric field is sufficiently high and the energies of electron and hole are greater than the thermal energies, then the term $\mu_n E$ or $\mu_p E$ should be replaced by the saturation velocity υ_s.

The continuity equations for electrons and holes are:

$$\frac{\partial n}{\partial t} = \frac{1}{q}\frac{\partial J_n}{\partial t} - U_n, \tag{2.12}$$

$$\frac{\partial p}{\partial t} = -\frac{1}{q}\frac{\partial J_p}{\partial t} - U_p, \tag{2.13}$$

where U_n and U_p are the net recombination rates.

Recombination and mobility models

The equations 2.14 and 2.15 represent the Shockley-Read-Hall (U_{SRH}) and Auger (U_{Auger}) recombination respectively [102]:

$$U_{SRH} = \frac{np - n_{ieff}^2}{\tau_n(p + p_{1ieff}) + \tau_p(n + n_{1ieff})}, \tag{2.14}$$

$$U_{Auger} = (c_p p + c_n n)(pn - n_{ieff}^2), \tag{2.15}$$

where τ_n and τ_p are the lifetime of electron and hole, n_{ieff} is the electron effective intrinsic concentration, n_{1ieff} and p_{1ieff} are auxiliary quantities (electron and hole concentration close to effective intrinsic level), and c_n, c_p are proportionality constants.

The variety of mobility models have been developed to be simply applied in the device simulation and reader is referred to [88]. The following equation represent the Canali model [103] to calculate mobility:

$$\mu_{can}(E) = \frac{\mu_o}{\left(1 + \left(\frac{\mu_o E}{\upsilon_{sat}}\right)^{\beta}\right)^{1/\beta}}, \tag{2.16}$$

Boundary conditions are needed in the model to impose on a semiconductor device. Basically boundary conditions are of three type; Neumann (reflective) boundaries, Insulator boundary and Dirichlet boundary. The details of these methods can be found in the PhD thesis of Baravelli ([104]).

2.2 TCAD simulation software

The TCAD is an important tool for semiconductor to predict the performance of a concept device before it is finally designed and fabricated in the reality; the TCAD simulation allows us to examine the issues and/or improvements required in a very new or immature technology. This procedure reduces the cost of development and promises a better outcome. Since a decade the SOI technology is used in pixel detectors developed for particle physics and medical applications. A SOIPIX group in KEK designed several detectors and used the TCAD ENEXSS/Synopsys software to solve some issues such as the back gate effect and search for the best performance in terms of radiation hardness by introduction of double SOI [76].

ENEXSS is used as a TCAD simulation software and in this section the tools available in ENEXSS will be discussed. The advantage of using ENEXSS beside Synopsys is that it supports the manufacturing processes that are used to fabricate real SOI detectors. The process simulation tool was developed by taking in consideration the SOI process involved in manufacturing the real detector.

Broadly, ENEXSS TCAD simulator consist of three tools:

1. Process simulator (Hyper Synthesised Process Simulator (HySyProS))
2. Device simulator (HyDeLEOS)
3. Plotting tool (SGraph)

In some simulators (for example Synopsys) the Graphical User Interface (GUI) is also present, it allows easy structure control (device structure can be edited using mouse) and it is user friendly. In ENEXSS all the steps of process simulation and/or device geometry have to be drawn by writing a separate line of code. The scripting language used for writing this code is the Simulation Control Language (SCL). The latest version of ENEXSS also allows 3D simulation.

2.2.1 Process Simulator (HySyProS)

The various steps involved in the fabrication of the SOI detector are generated in virtual environment using the process simulator. Such steps include deposition, etching, implantation, etc. In general the TCAD simulator requires robustness of the 3D process simulator (especially 3D meshing and 3D topography). It also needs large amount of memory and calculation time. HySyProS is a 3D simulator which was developed to have a robust topography calculation and meshing. It also includes functions to reduce calculation time and memory requirements. In 3D TCAD process simulation the key task is to predict the impurities doping profile. It can be predicted by solving the diffusion equations over the simulation mesh. HySyProS is also known as a 3D impurity simulator.

To simulate a real semiconductor-device, the HySyProS simulator includes several steps and uses different models, as follows [105]:

1. Impurities diffusion: Diffusion is one of the important steps used in the process simulation. Different models have been developed and some of them are available in HySyProS simulator and those are: Fair-Tsai [106], Mulvaney [107], Ghaderi's 3/5 variable [108], Dunham's 3/5 stream [109] models.
2. Oxidation: For the proper modelling of the stress, oxide and nitride have to be considered as viscoelastic materials. Viscoelastic treatment of thermal oxidation has the valuable advantages [110].
3. Ion implantation: Monte-Carlo models are used to solve the equation for ion implantation. Monte-Carlo model is a traditional approach for crystalline targets based on the calculation of a large number of "distinct" ion trajectories [111].

HySyProS software developers allow us to choose the appropriate models according to the constraints of the process simulator. All the microscopic information is provided to the process simulator and the generated file is the input to the device simulator. The real device process flow is followed in the actual process simulation tool. The expert who have a good theoretical background of the impurity diffusion will use this tool to implement a realistic virtual device.

2.2.2 Device Simulations (HyDeLEOS)

Several properties such as electrical, mechanical, thermal and optical of the semiconductor device can be modelled using the device simulators. The device simulator can work in connection with a process simulator or in standalone mode by defining the structure of the device manually. HyDeLEOS is a device simulator tool available in ENEXSS. The fundamental physics for this simulator is the same as for other TCAD software suites. It solves the DD equation (see section 2.1.2), quantum mechanical calculations and optical modes computations. The applications of HyDeLEOS are: single device (threshold voltage, saturation and leakage current, capacitance, etc.), circuit design (wire resistance and capacitance, propagation delay), and the defect analysis (Electro Static Discharge (EDS) and latch-up). The behaviour of the device is predicted by providing the geometry, characteristics, and internal operating conditions of the device to HyDeLEOS. The program to execute device simulation is divided into three sections. Those are described below:

1. Preprocessing section (deleos_shell) : In "deleos_shell" the device structure, dopant distribution, electrode name and position, and mesh methods are defined. The file generated using deleos_shell will be used in the calculation section "deleos". The semiconductor device simulator (HyDeLEOS) can be used in two modes: first a standalone mode that defines the structure and properties of the device manually by using input commands. In second mode the device simulation works in connection with a process simulation. The device simulator HyDeLEOS uses a file which was previously generated by the process simulation HySyProS to configure the dopant density and mesh information. A standalone mode is used in this study. It is possible to realise the device in one, two, and three dimensions. Two implementation methods are available: polygonal mixed meshes can be generated using HySyProS, or orthogonal mesh is built up semi-automatically by providing the material boundary, location of a p-n junction, etc.

2. Calculation section (deleos) : In "deleos" section the simulator solves the basic equations of a semiconductor using the device structure (defined in deleos_shell), boundary conditions, and electrical characteristics such as terminal current (defined in deleos). The DD module is treated as main part of HyDeLEOS simulation. The list of equations grouped in DD module includes: Poisson's equation and electron and hole current continuity equation (see section 2.1.2). The other possible calculation modules available in HyDeLEOS are: heat conduction, electron and hole energy transportation equations, electrical conduction equation, and

circuit equations. The calculation section is also used to define the type of analysis. HyDeLEOS supports steady-state analysis, Alternate Current (AC) analysis, capacitance analysis, and transient analysis.

3. Post-processing section (deleos_extract) : It is the last part of the device simulator code. The "deleos_extract" is used to extract the parameters of the device. It extracts threshold voltage, drain current, scaling factor, etc. These parameters are used for optimisation function. The file generated in "deleos_shell" is used and the electrode name is provided with the parameter name to extract the characteristic value.

Each section described above can be executed separately or in batch processing using "dswrap" tool. The detail list of methods/modules can be found in the ENEXSS ver.4.1 users manual [112].

Doping

The intrinsic semiconductors are intentionally doped by introducing impurities to control the conductivity. The electrical properties of semiconductors can be defined by the type of impurity atoms used. In this case silicon is use as a semiconductor. The impurity element should belong to group III or V elements to produce p-type or n-type silicon respectively. Type of impurity elements available in TCAD ENEXSS from group III are Boron (B) and Indium (In), and from group V are Phosphorous (P), Arsenic (As), and Antimony (Sb). In the semiconductor industry the doping is incorporated as a crucial ingredient of their device structure. Three types of doping distribution are possible in HyDeLEOS simulation; Homogeneous, Gaussian and Linear distributions. The default value of doping style is homogeneous. The Gaussian and linear distributions can be manually set using the following functions:

$$N(x) = N_{peak} * exp\Big[- \frac{(x - x_{peak})^2}{2\sigma^2} \Big], \tag{2.17}$$

$$N(x) = max\Big(1.0, N_{ref} + slope.\big|x - x_{ref}\big|\Big), \tag{2.18}$$

The dopant density using Gaussian distribution is calculated using equation 2.17. N_{peak} is concentration at the peak and the position of the peak can be specified using x_{peak}. Standard Deviation (SD) can be specified with σ. Equation 2.18 represents the linear distribution at location "x" to calculate the dopant density. Whereas the N_{ref} and x_{ref} represent the referential concentration and reference point respectively. Similarly the dopant density at location "y" or "z" can also be specified [112].

2.2.3 Plotting tool (SGraph)

After the execution of codes written in HySyProS and HyDeLEOS some files are generated. The data in those files can be displayed by the "SGraph" (refer user manual "SGraph" [113]). It is a displaying tool used to plot Graph3D, Graph2D, Graph1D, etc. The device structure, dopant distribution, and potential distribution in the semiconductor devices can be plotted in 3-D space. The other interesting features available in "SGraph" are Bird's eye view of physical values, multiple graph, recording frequently used operations, and cross-sectional view.

2.3 Geometry of SOI prototypes

SOI technology allows us to use thick and thin high resistivity Silicon (Si) and low resistivity Si respectively on the same processed wafer. This technology does not require bump bonding. Before development of real SOI detector prototype, the ENEXSS TCAD tool was used to realise virtually DIPIX pixel detector (refer chapter 4). The geometry of DIPIX pixel detector prototype is described below.

The deleos_shell section is used in HyDeLEOS tool to describe the structure of the DIPIX prototype. The doping level and the material information are prescribed by the foundry. Figure 2.2 shows the structure of DIPIX. To study the back gate effect and transistor characteristics, two pixels with a pitch of 30 μm, and a transistor exactly in the middle between these two pixels, are implemented. The pixel pitch is used as a parameter to observe the back gate effect on the transistor placed on the top Si. The BPW is placed just below the pixel in order to mitigate the back gate effect. To find the optimised length of BPW, it is used as a variable.

The 2-D structure of the device (DIPIX detector) is implemented. The BOX layer with a size of 200 nm is sandwiched with a thin electronic layer and thick sensor layer, see figure 2.2. The thickness of electronic layer is 50 nm. The sensor thickness is used as a parameter in the code and in this case it is set to 250 μm. The doping profile represents the resistivity of the wafer. To realise CZ-n wafer with 700 Ω cm resistivity, the silicon is doped with Phosphorous (P) element homogeneously with 4.00E12 cm^{-3} impurity concentration. The doping style of P-substrate and BPW is Gaussian and the peak impurity concentration is 3.47E20 cm^{-3} and 5.5E15 cm^{-3} respectively. The doping element used is Boron (B). The thin silicon is lightly doped homogeneously with 4.00E17 cm^{-3} impurity concentration and the doping element used is Boron (B). A NMOS transistor is implemented in the electronic layer to study the back gate effect.

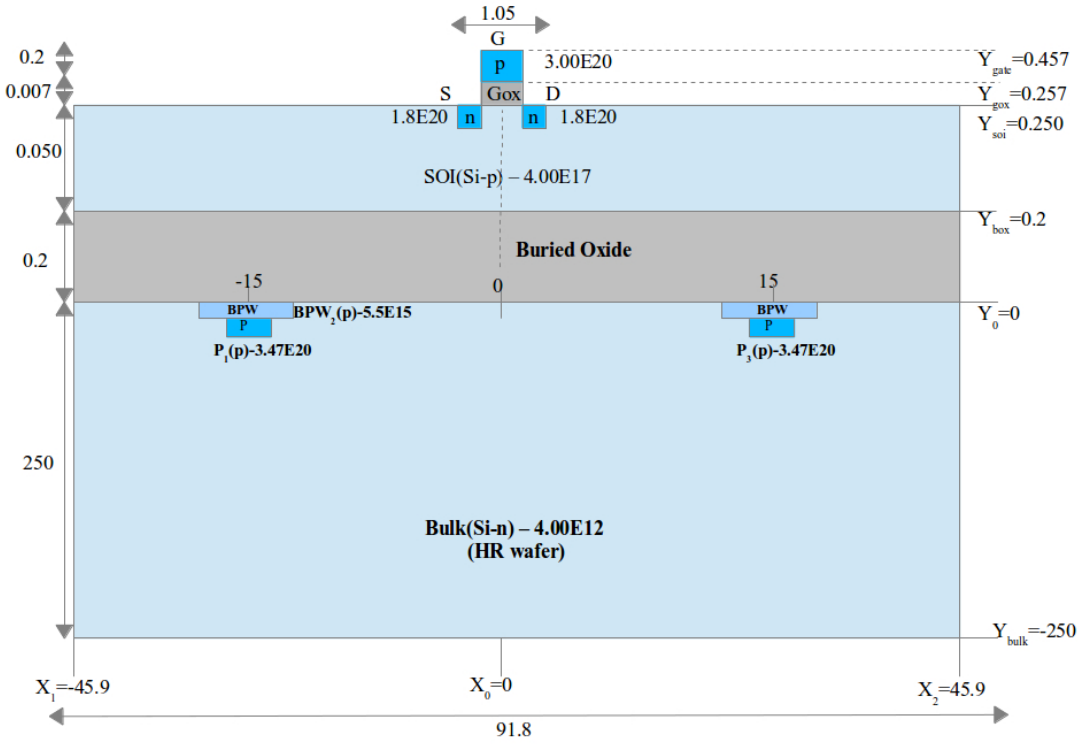

FIGURE 2.2: Geometry of 2-D DIPIX pixel detector prototype with dimensions, material and doping profile details. Note: All dimensions are in μm and not to scale.

The doping concentration in the drain, source, and gate are shown in figure 2.2. Finally, the electrode position and meshing profile is provided.

The "deleos" section describes the calculation methods used in the analysis. Two methods are available for matrix solver; Supernodal and Bi-Conjugate Gradient STABilised (BiCGSTAB). These methods will not be discussed here, please refer to [114] and [115]. The Supernodal is a direct method and for less complicated analysis it is the best option. To reduce the simulation time the iterative method (BiCGSTAB) is recommended. In this example the direct method is used for matrix solver for initial and bias value calculation. To keep the simulation simple the carrier generation and recombination option is switch off and also the parameter of the quantization model is not used. The carrier mobility can be used to set the lattice temperature, dopant density, vertical and horizontal electric field. In this case the lattice temperature dependency is applied and the surface scattering mobility and saturation mobility model is set to LOMBARDI [116] and SCHARFETTER [117] method for vertical and horizontal electric field respectively.

2.4 Results of SOI simulations

The issue of the back gate effect was the main difficulty to take this technology further. It changes the threshold voltage of Metal-Oxide-Semiconductor (MOS) transistors placed at a distance of 200 nm from the sensor. The presence of back gate effect do not allow the electronics part to work beyond 30 V of the substrate (sensor) bias voltage. This effect restricts us to operate the detector not in full depletion. To study this effect ENEXSS TCAD simulation software was used.

2.4.1 Back gate effect and reduction technique

Two configurations are studied in this model. Firstly, the transistor is placed exactly at the top of the pixel in the electronic layer and second, the transistor is placed between the pixels. The effect of back gate is studied by varying the length of BPW, see figure 2.2. The NMOS normal voltage body floating IO type transistor is used and the $\frac{W}{L}$ ratio is $\frac{1}{0.35}$ μm.

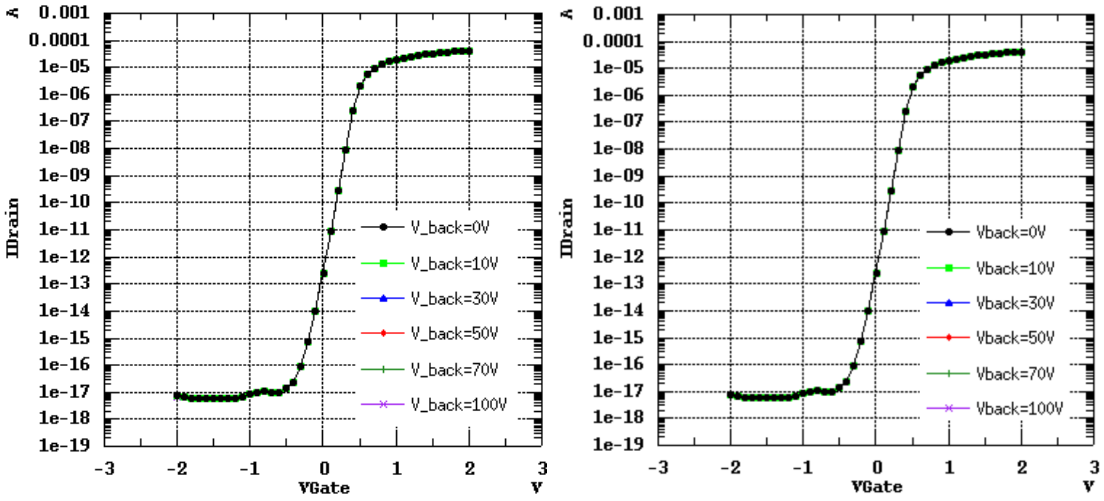

FIGURE 2.3: Transfer characteristic of NMOS IO transistor at different sensor back bias voltages. The transistor is placed at the top of the pixel and back gate effect is studied by varying the BPW size from 1 μm (left) to 8 μm (right).

The transfer characteristic of NMOS body floating transistor is shown in figure 2.3 for the first configuration (transistor placed exactly at the top of the pixel). The detector bias voltage is varied for two different BPW sizes (i.e. 1 μm and 8 μm). As expected, no change in the transistor threshold is observed at different sensor bias voltages. This confirms that the presence of electric field in the sensor part does not affect the operation of transistors available at the top of the pixel, see figure 2.3 (left) and 2.3 (right). In this configuration the back gate effect was not observed, but it restricts us to use only the area available at the top of the pixel, which is not practical.

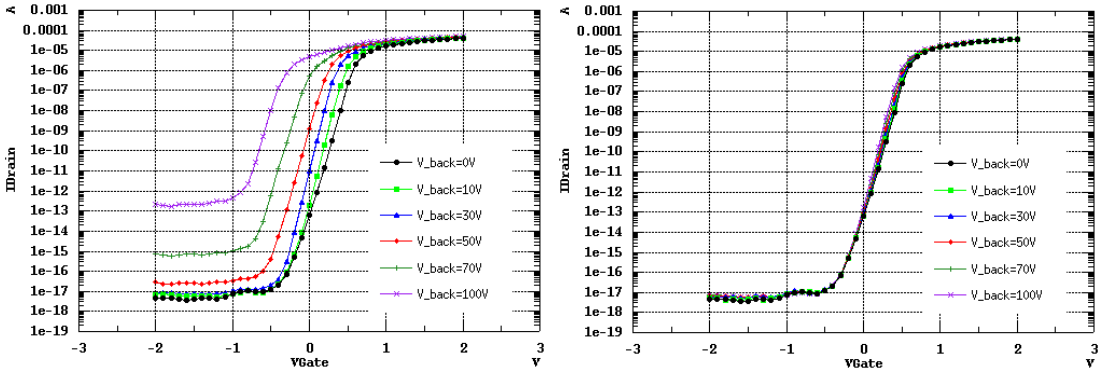

FIGURE 2.4: Transfer characteristic of NMOS IO transistor at different sensor back bias voltage. The transistor is placed between two pixel and back gate effect is studied by varying the BPW size from 1 μm (left) to 8 μm (right).

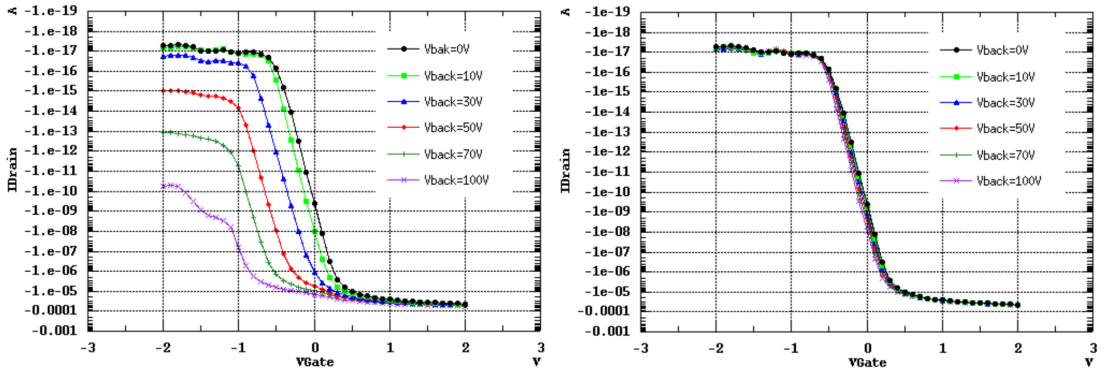

FIGURE 2.5: Transfer characteristic of PMOS IO transistor at different sensor back bias voltage. The transistor is placed between two pixel and back gate effect is studied by varying the BPW size from 1 μm (left) to 8 μm (right).

Figure 2.4 shows the transfer characteristics of the transistor in second configuration (transistor placed between two pixels). At constant drain voltage of 100 mV, the drain current is recorded for different gate voltages and detector bias voltages. Figure 2.4 (left) shows the transfer curve for BPW 1 μm. It is seen that by varying detector back bias voltage from 0 V to 100 V, the transistor threshold voltage is shifted. It clearly shows that above 30 V of detector bias voltage, this effect affects the transistor behaviour. Since the size of BPW is very small, it cannot shield the large electric field produced by increasing detector bias voltage. To optimise the size of BPW, its dimension is increased with a step size of 1 μm until no back gate effect is observed. Figure 2.4 (right) shows no change in transistor threshold at 8 μm of BPW. Similar simulations were done by placing PMOS transistor between the pixel and observed the same result (see figure 2.5). This confirms that by placing a BPW near the pixel the back gate effect is mitigated. In practice, when the BPW size is larger then the gain of the detector is worse because of increased pixel capacitance, see section 3.4.5. The back gate effect can also be mitigated by designing smaller size pixels and not using the BPW layer.

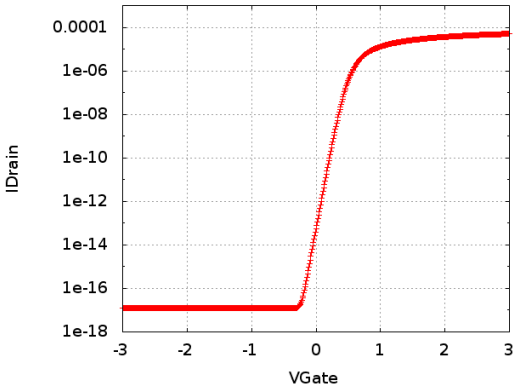

FIGURE 2.6: The transfer characteristic of NMOS IO transistor simulated using Cadence.

The NMOS normal voltage body floating IO type transistor used for back gate effect study is also simulated in cadence for comparison with TCAD simulation, and the size of transistor is the same as used in the TCAD simulation. To plot the transfer characteristic of NMOS, the DC analysis in cadence is selected and a constant 100 mV of drain voltage (V_d) is applied. Figure 2.6 shows the drain current (I_d) as a function of gate voltage (V_g). The resulting characteristic of NMOS transistor in cadence (figure 2.6) is similar to the TCAD simulation, (see left figure 2.4).

2.4.2 Electric field distribution

In principle the electric field in the electronics layer of the detector should be constant regardless of change in detector back bias voltage. The presence of back gate effect on SOI technology results in varying electric field in the electronics layer. The back gate effect can also be studied by observing the electric field across the transistor placed in the top silicon. In this simulation the same geometry is used as described in section 2.3. The bulk size is set to 250 μm with resistivity of about 700 Ω cm.

The electric field in the oxide layer is simulated for different back bias voltages. The transistor (NMOS normal voltage body floating IO type) is placed between two pixels and the effect of BPW is observed. Figure 2.7 shows the simulation result of electric field in oxide layer at position $Y_{box} = 0.2$ μm (see figure 2.2). Each pixel is provided with 1 μm and 8 μm BPW shown in figure 2.7 top and bottom respectively. In figure 2.7 (top) the size of BPW is very small and the electric field effect can be easily seen on transistors. The electric field at the transistor is increasing as the detector back bias voltage increases. In case of larger BPW in the pixel a very small change in electric field is observed, see figure 2.7 (bottom).

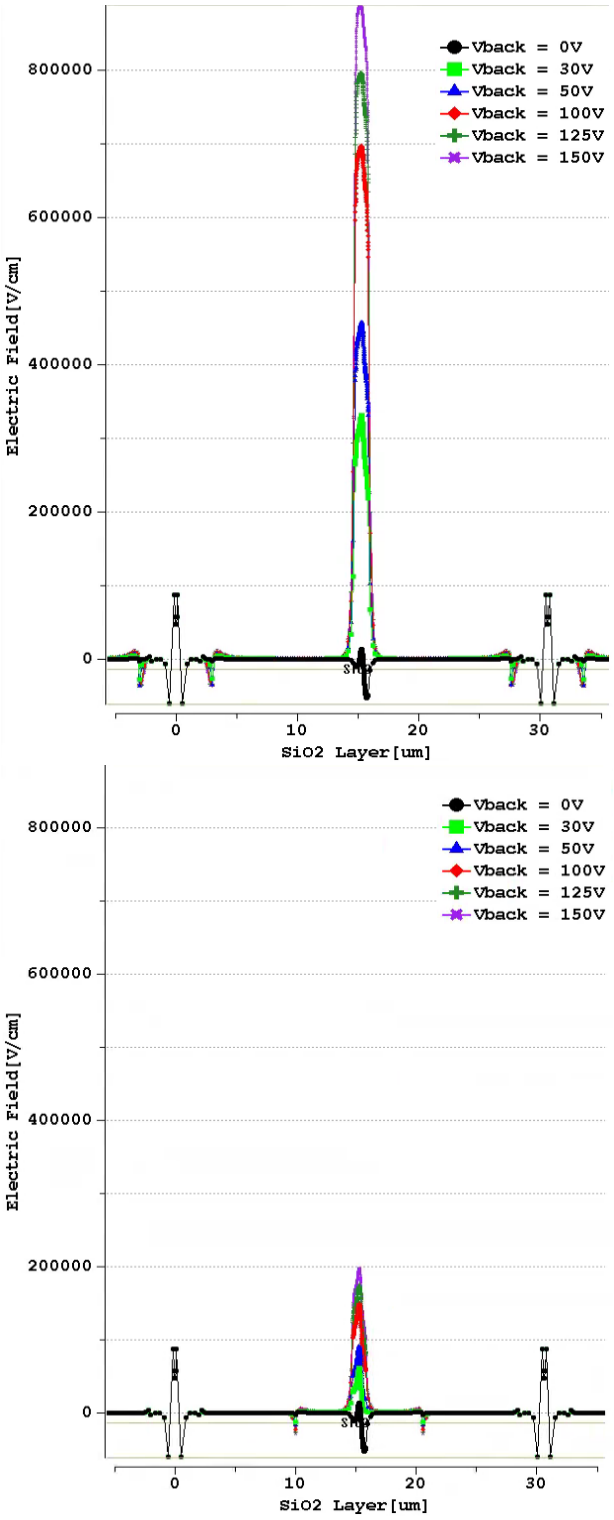

FIGURE 2.7: The back gate effect on transistor is studied by varying BPW size. The electric filed distribution of SOI pixel sensor in the oxide layer is shown for two BPW sizes, 1 μm (top) and 8 μm (bottom).

Chapter 3

Test set-up and INTPIX3 detectors

During the last decade, significant research and development activities have taken place in the field of CMOS SOI technology resulting, in improvements in wafer size, wafer resistivity, radiation tolerance, and spatial resolution. Several ideas have been tested successfully and are gradually entering into the application phase. Some of the novel concepts exploring SOI technology are pursued at KEK. The SOI pixel detector prototypes are tested to confirm their usefulness for future high energy, nuclear physics, satellite and medical applications, where charged particle imaging is required. As a first step to fulfil a set of basic and demanding requirements, a detail studies were carried on the detectors, designed and prototyped in SOI technology. Several prototypes of INTPIX and DIPIX detectors have been produced and are described briefly in section 3.1. The feasibility of the novel techniques for high energy applications, were evaluated and presented [79, 118, 119].

This chapter mainly focuses on the test set-up's and measurements of INTPIX detectors. The set-up for the laboratory tests and the detector measurement procedures are discussed in section 3.2. The laboratory tests included measurements of test structures, verification of basic electrical parameters, examination of long time stability, measurements of the pedestal and noise, calculation of the laser spot size, pixel scan measurements in the X and Y directions using visible laser light pulses, and calculation of noise and gain using radioactive source.

3.1 Details of INTPIX and DIPIX SOI detectors

A number of detectors have been designed in SOI technology, INTegration type PIXel (INTPIX) and Dual mode Integration type PIXel (DIPIX) are among the main families.

The INTPIX is a pixel detector prototype first designed and implemented in the 150 nm SOI CMOS technology. The technology was developed by OKI Electric Industry and the INTPIX detector was designed by Y. Arai at KEK in Japan. In 2006 INTPIX2 was designed in the same technology and the back gate effect was found. This was the main issue with SOI technology which did not allow the front end electronics to work beyond 30 V of back bias voltage. A 3-D TCAD simulator was used to understand the back gate effect [120]. After an intense research and discussions late in 2009, INTPIX3 was designed to study the remedies to back-gate effect observed in previous prototype (INTPIX2). INTPIX3 is a signal integration type pixel detector, fabricated in SOI 200 nm process. The pixels are of the integration type, where the charges are integrated on the pixel input capacitance for the defined time period.

DIPIX is also a integration type pixel detector with some advanced features included in the pixel and readout. The first flavour of this detector (DIPIX1 and DIPIX2) was designed in 2010. Each pixel is provided with Correlated Double Sampling (CDS), supposed to reduce the DC level shift of the signal and to give lower frequency noise. Both digital and analogue modes of readout are possible thanks to the on-chip ramp-compare type Analogue to Digital Converter (ADC) [121]. The circuit is also prepared to work both with the N-type and P-type sensors.

In this dissertation the measurements and results of INTPIX3a, INTPIX3b [1], and DIPIX2 (CZ-n, FZ-n and FZ-p) pixel detectors will be discussed in detail.

3.2 Test set-up and procedures for detector measurements

The test set-up is the backbone of the measurement and it is very important to discusses how it was prepared. The test set-up described below is for the X-ray and laser measurements. An overview of data analysis shall be also given in this section.

3.2.1 Test set-up for radiation source

The INTPIX3 and DIPIX2 detectors were extensively tested with ionising radiation to measure the effect of incident charged particles. All chips were exposed to soft X-rays from a radioactive source. The source used for these measurements was the Am-241. The activity of an Am-241 source was 10 mCi (=370 MBq). Table 3.1 gives the radiation data of the Am-241 source. The Alpha's are the fast moving helium nuclei with high energy, typically in MeV range but due to their large mass, they are stopped by just a

[1] INTPIX3a and INTPIX3b are flavours of INTPIX family

few inches of air or a piece of paper [122]. In the Am-241 source alpha's are already blocked by a mask and only the X-ray (gamma) lines are radiated to generate the charge in the pixels.

TABLE 3.1: Am-241 Radiation Data.

Radiation Data.		
Type	Energy (keV)	Intensity (%)
Am-241 Alpha	5483	84.5
Am-241 Alpha	5443	13.5
Am-241 X-ray	59.5	35.9
Am-241 X-ray	26.3	2.4
Am-241 X-ray	13.9	42
Cu L X-ray	8.01	-
Np L X-ray	17.7	-
Np L X-ray	20.7	-

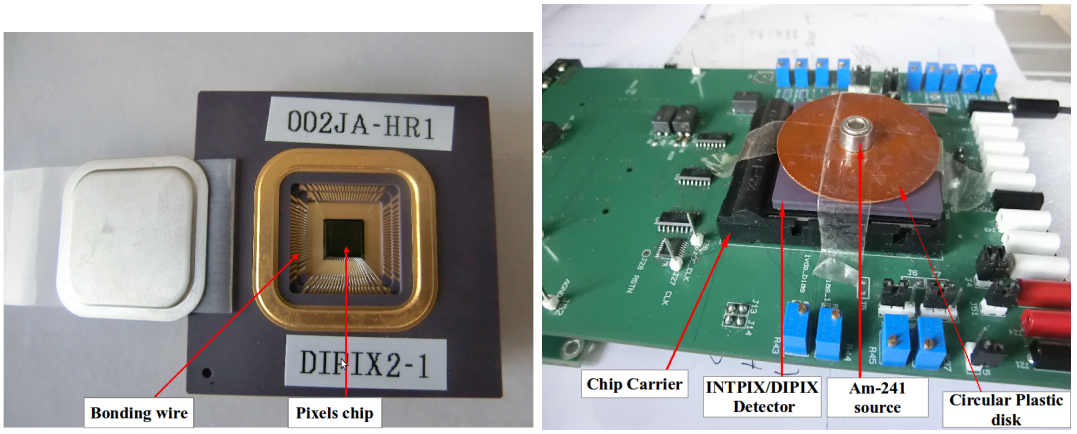

FIGURE 3.1: Radiation source set-up, detector (left) and set-up (right).

The DIPIX2 detector and the set-up with radiation source is shown in figure 3.1. Bonding wires and pixels chip can be seen at front side of DIPIX2 detector, see figure 3.1 (left). The chip carrier on the Printed Circuit Board (PCB) is used for both INTPIX3 and DIPIX2 detectors (figure 3.1 right) and the size of both detectors is 5 x 5 mm^2. Each pixel in INTPIX3 is 20 x 20 μm^2 and in DIPIX2 it is 14 x 14 μm^2 in size. The centre of each pixel is 5 x 5 μm^2 and this part of the pixel has open window (without metal lines and transistors), which enables us to test with visible laser light or light X-rays. The radioactive source can be placed close to the detector with the help of circular plastic disk. It was prepared with a hole in it to hold the source as shown in figure 3.1 (right). The distance between the source and the detector is 3 mm. The scotch tape is placed at one side of the circular disk to hold the source and this can also help in blocking the alpha particles, if there are any. Since the size of pixel matrix smaller than the diameter of radioactive source (7 mm), all pixels can be involved in charge collection. It

was necessary to place the whole set-up in a black box, since the detector is sensitive to visible light.

3.2.2 Test set-up for IR laser

The laser tests were carried out with picosecond pulsed diode laser (PDL 800-D) produced by PicoQuant [123]. The characteristics of the laser source are listed in table 3.2. The wavelengths can be changed simply by plugging in the appropriate laser head. Internal oscillator has two selectable base frequencies, 80 MHz and 1 MHz. The highest repetition frequency that can be attained is 80 MHz and the lowest is 31.25 kHz [123]. Two laser heads with wavelengths 1060 nm (Infra Red (IR) laser) and 660 nm (RED laser) were used to study the depletion in silicon bulk.

TABLE 3.2: Characteristics of the laser source.

Laser	PDL 800-D
Operation mode	pulsed or continuous-wave
Wavelength	1060 nm and 660 nm
Pulse width	70 ps
Spot size	$\sim$ 5 μm (after focusing)
Frequency	31.25 kHz - 80 MHz

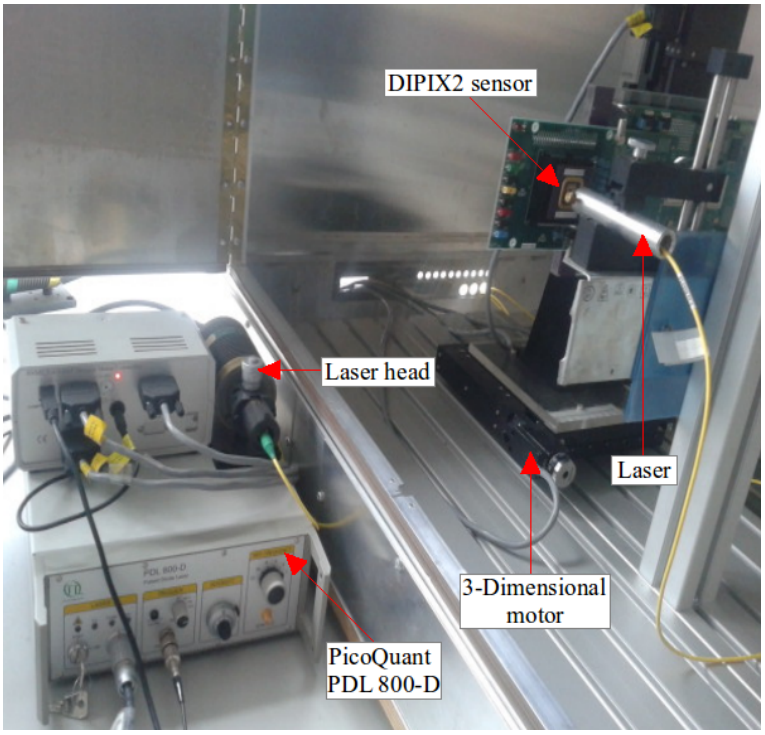

FIGURE 3.2: Laser set-up.

Figure 3.2 shows the set-up used during the laser test. It consists of a 3-D step motor, a PicoQuant laser (PDL 800-D), a laser head, a laser, and a detector with a readout. The

detector was mounted on a movable arm of 3-D step motor using a plexiglass and the laser was mounted on the immovable stand at other end. The detector can move using 3-D step motor to position the laser at a desired position and distance from the detector.

3.2.3 Clustering algorithms

A number of algorithms are available and can be used to reconstruct pixel clusters created by an ionising particle. The main aim of cluster algorithm is to find accurate position and amplitude information. The experimental conditions are important to consider while choosing the cluster algorithm. Depending on the experimental requirements, cluster algorithm method described in paper [124] is adopted for cluster finding. The cluster algorithms are employed for the analysis of the Am-241 data and laser data. The charge deposited from the Am-241 source is mainly from 6 different energies, see table 3.1. Depending on the pixel size and impact point the charge can be deposited in one or more pixels. Possibly, the lower energies can produce event in one or two pixels and higher energies in three, four or more pixels. For the laser, most of the charge induced by the laser radiation can be deposited in one or two pixels, after optimising the laser intensity, position, and distance between the laser and the detector.

The flow chart of cluster algorithm is shown in figure 3.3. To search for clusters created by an ionising particle, the first selection criterion is to find the seed. The seed is a pixel with the highest pixel amplitude and above a predefined threshold. To separate the noise from the signal, the predefined threshold must be set high, at least 5 times larger than the pixel noise sigma [125]. The data analysis were done with several sets of the threshold values and the best result which separate noise and signal were used as the predefined thresholds. All the neighbouring pixels of the seed are checked by comparing their amplitude with the predefined threshold to find other hit pixels. Initially the value of predefined threshold is set to 5.5 times the pixel noise sigma and further, as the cluster size increases the predefined threshold is reduced by one sigma. Since the neighbouring pixels hold only a part of the signal from the total deposited charge, the predefined threshold is reduced by one times the pixel noise sigma for each repetition (see figure 3.3). If the neighbouring pixel amplitude is above the predefined threshold then the pixel is considered as a subset of seed and it is labelled as a hit pixel. Each hit pixel amplitude is added to the cluster sum and treated as a new seed. The search for other hit pixel is recursively applied on all neighbouring pixels until no subset of seed is found. Finally, the computed clusters are filled in the histogram.

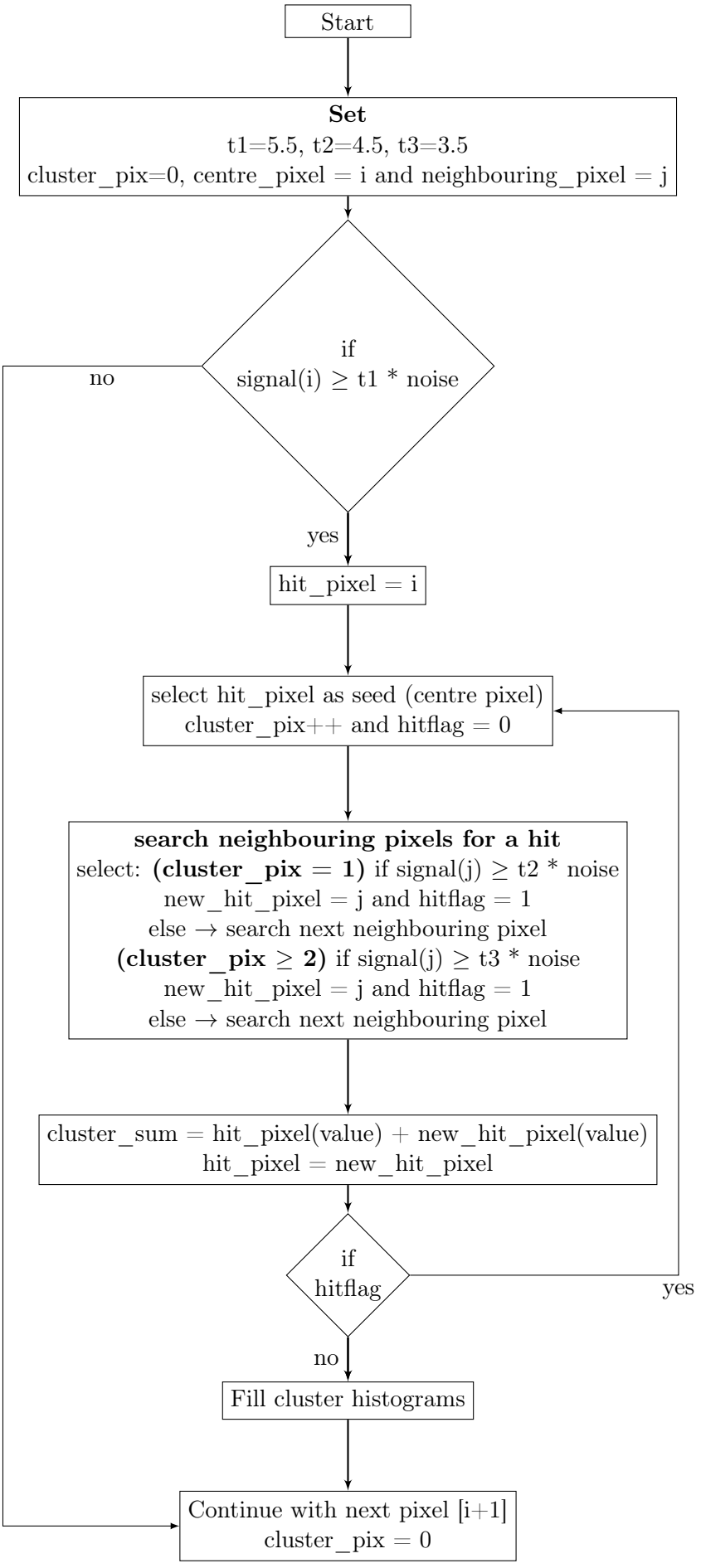

FIGURE 3.3: Flow chart of cluster recognition.

3.2.4 Data analysis

A program was written for the analysis of the Laser and Am-241 data. It focuses on the signal extraction right from the raw data. Signal can be extracted by two methods: offline and online. In offline method, two sets of data were taken: the pedestal run (data collected before placing the source) and the signal run (data collected after placing the source) [125]. Whereas in online method only signal run is recorded after placing the source and the noise is extracted from the signal run by updating the pedestal to trace a slow changes of the pixels Direct Current (DC) level [126]. Depending on the measurement, particular analysis method is used, since both methods give similar noise results. For example in the laser set-up, one can switch off the laser signal from outside without opening the black box. This gives the possibility to take two sets of data: one with the pedestal and other with the laser signal, and the offline method may be applied for the analysis. In case of measurement using an Am-241 source at low temperature, the whole set-up is placed in the fridge to achieve a constant temperature, and we are also interested in the leakage current of the detector. If the fridge is opened during the measurement to place the source between two (pedestal and signal) data taking runs, then most probably this would affect the temperature and also the leakage current. To avoid this the online method is used for the analysis.

Offline method: The flow chart of the offline data analysis is shown in figure 3.4. Two sets of raw data were taken, one without source (pedestal run) and other with source (signal run). In pedestal run 500 events were taken in total from which first 50 events were rejected to allow the voltage levels to settle, and remaining 450 events were used for the pedestal and noise calculations. The pixel matrix may consist of normal, saturated, dead, and hot pixels. The saturated pixels are mostly present at the border of the pixel matrix and they can be removed by masking first and second rows and columns. Dead and hot pixels are masked by introducing a low threshold is 0.5 times noise sigma and high threshold is 5 times noise sigma respectively. Dead and hot pixels are collectively called as bad pixels.

Random noise contributes to each pixel and it is Gaussian distributed with mean zero. A histogram (see figure 3.5 left) is plotted after averaging all the events and the noise (Root Mean Square (RMS)=2.459 ADC counts) is taken as the sigma of the pedestal histogram. The Common Mode (CM) fluctuations can be removed by taking the average over signal after subtracting the pedestal from the raw data. Figure 3.5 shows the histogram of the pedestal before and after removing the CM noise. It is seen that the noise (RMS values) is reduced after CM subtraction, see figure 3.5 (right). The noise is calculated as the sigma of the signal resulting after removing the CM noise, bad pixels, and the pedestal from the raw data. Second sequence of events is taken with the laser signal and signal

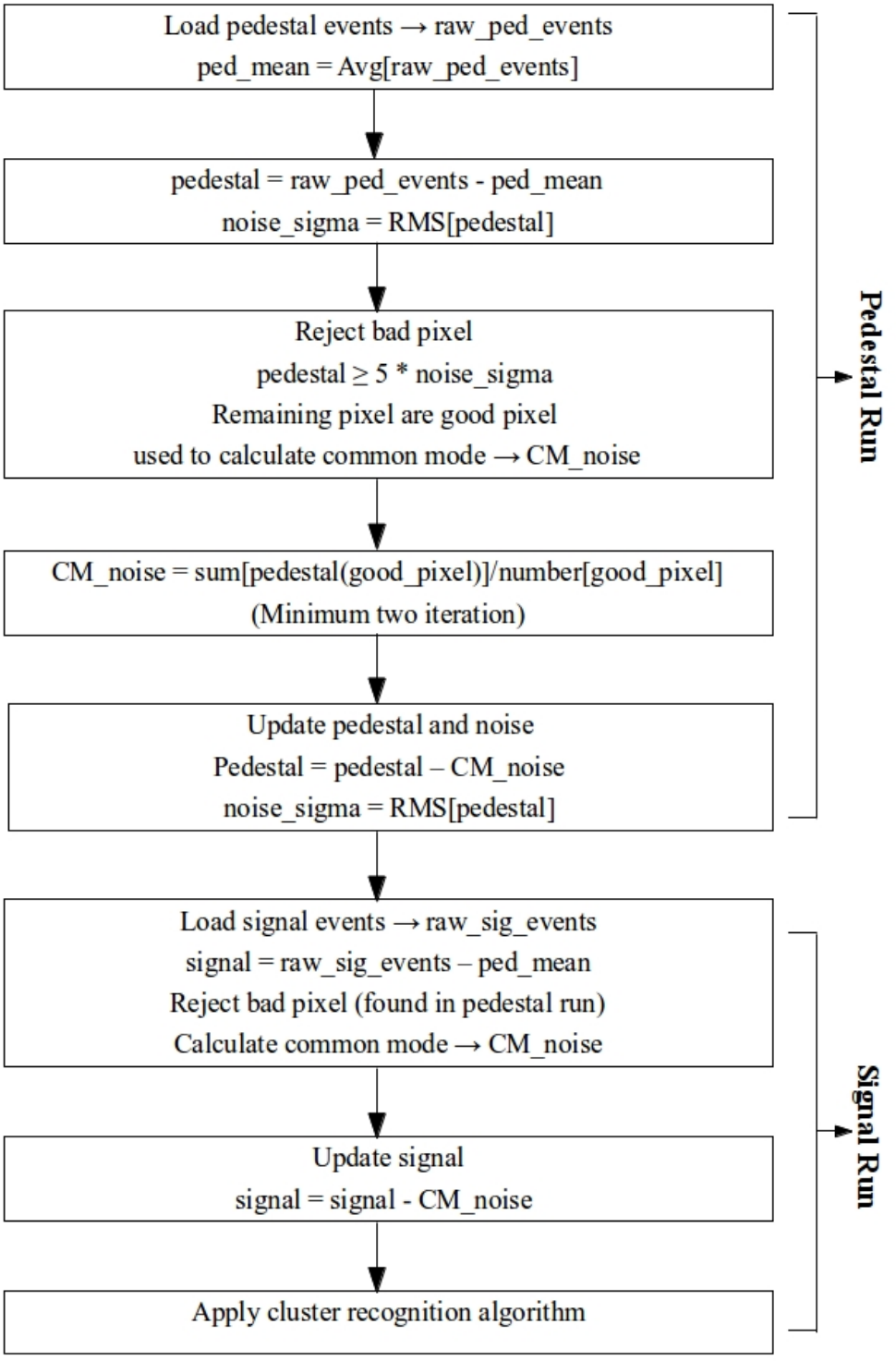

FIGURE 3.4: Flow chart of offline data analysis.

extraction is carried out by rejecting bad pixels (found in pedestal run), saturated pixels, and subtracting the pedestal and CM noise from the raw signal data.

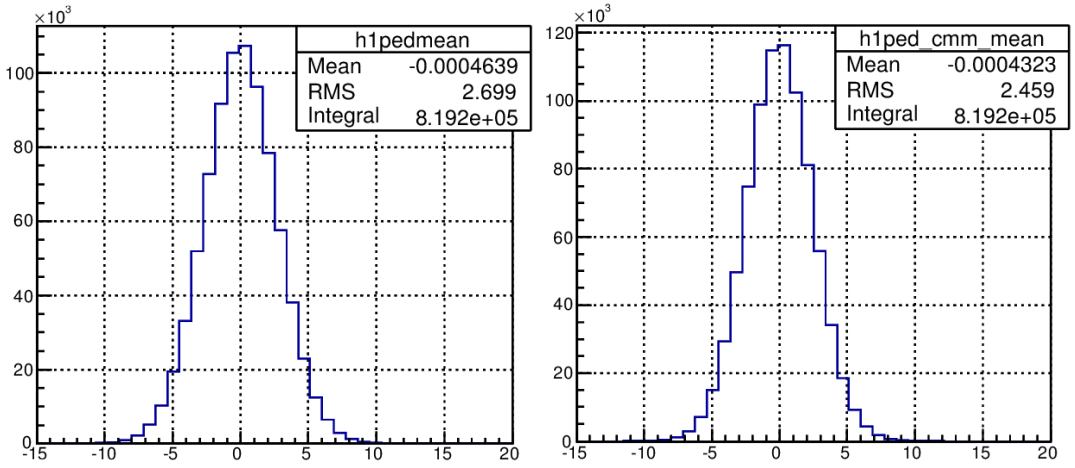

FIGURE 3.5: Histogram of 8^{th} region of INTPIX3a without CM noise (left) and with CM noise (right).

Online method: The flow chart of online data analysis is shown in figure 3.6. In this case no pedestal run, only signal run with the Am-241 source was used for the data analysis. Same as offline analysis, first 50 events are rejected to settle the voltage levels and remaining events are divided into three parts:

1. The average of next 50 events after rejecting first 50 events are used to initialise the pedestal and noise array (initial events)
2. Next 400 events are used to update the pedestal and noise values (Initial events)
3. The rest of events are used for signal calculation and cluster recognition (remaining events)

Equations 3.1 and 3.2 [126] are used to update the pedestal and noise array. The number of events "50" and "400" depends on the level of fluctuations in the pedestal, noise, and the values of pedestal weight (W_p) and signal weight (W_s). The values of weight used in this analysis are $W_p = 0.01$ and $W_s = 0.001$ for not a hit pixel. Similar equations will be used if the pixel is a hit pixel, however with smaller weights ($W_{pmin} \ll W_p$, $W_{smin} \ll W_s$):

$$ped_E(i) = (1 - W_p).ped_{(E-1)}(i) + rawdata_E(i).W_p, \tag{3.1}$$

$$noise^2_E(i) = (1 - W_s).noise^2_{(E-1)}(i) + signal^2_E(i).W_s, \tag{3.2}$$

The pedestal and noise are extracted by using appropriate weighted sums of the recorded values. When the mean value of noise^2 array is stable all bad pixels are removed. In this analysis the noise is calculated dynamically. Finally the cluster recognition algorithm is applied to find all the energies from Am-241 source.

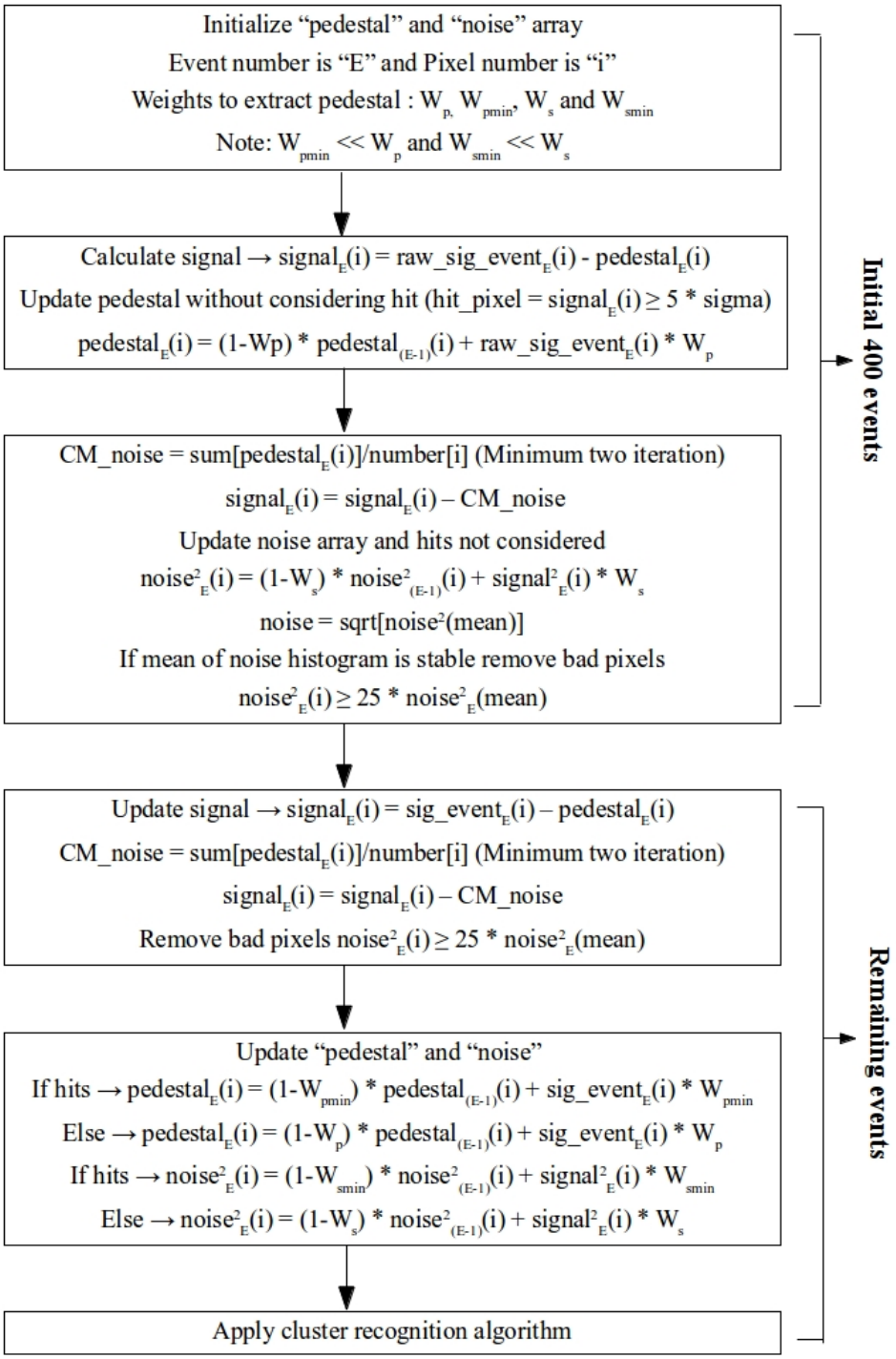

FIGURE 3.6: Flow chart of online data analysis.

3.3 Measurements of test structures

The INTPIX3a was designed with BPW to mitigate the back gate effect in the SOI technology (see subsection 2.4). To evaluate the effect of BPW, the transistor Test Element Group (TEG) was provided in INTPIX3a prototype. Figure 3.7 shows INTPIX3a top layout with the test transistors locations. The transistor Test Element Group (TEG) can be seen at the top and right side of the INTPIX3a layout, with and without BPW. There are 7 NMOS and 6 PMOS test transistors, described briefly in table 3.3. The W/L (ratio of transistor width to the gate length) is constant for all body floating and body tie transistors, whereas the M7 NMOS transistor is the depletion mode IO, with smaller W/L ratio than other transistors. The minimum gate length is 0.20 μm and 0.35 μm. The floating body type transistors are of three (Low, Normal and High) thresholds. In the design the source is common for both NMOS and PMOS transistors, as seen in figure 3.8 and 3.9. The transistors TEGs are added in the layout of INTPIX3a to study the back gate effect and to investigate the effects of radiation induced hole traps. The latter was briefly discussed and presented [127].

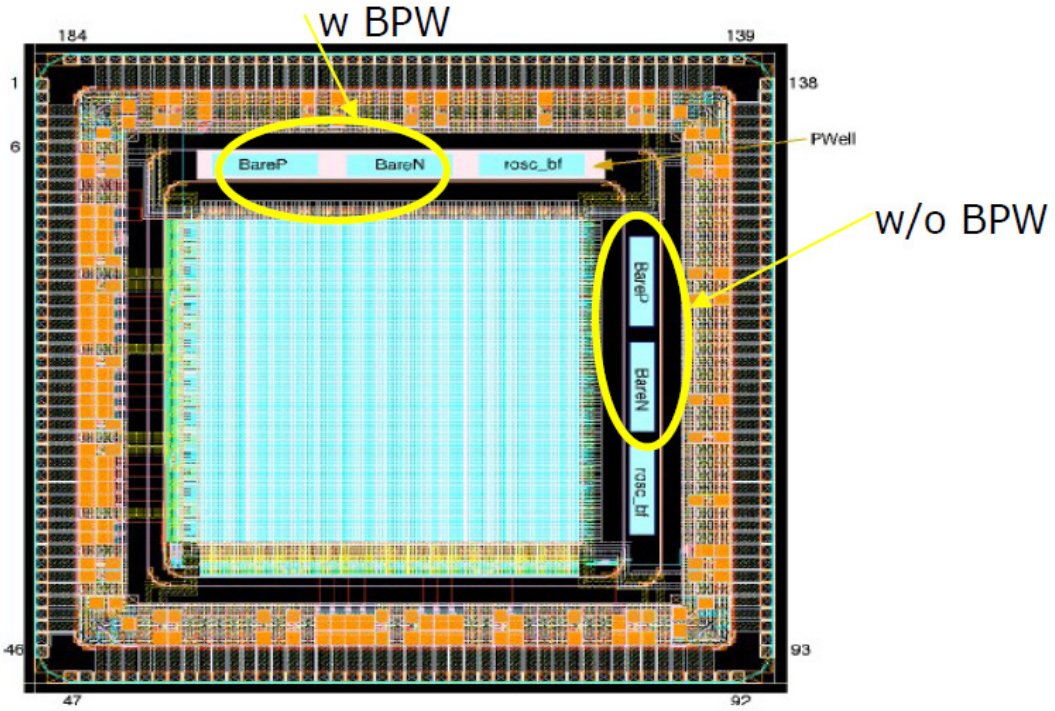

FIGURE 3.7: INTPIX3a layout with transistor location.

For ease of understanding, only the characteristic of M1 (NMOS) is used to visualise the back gate effect. Single transistor is selected by connecting specific gate and drain terminal of the TEG to the semiconductor device parameter analyzer (Agilent B1500A). Figure 3.10 shows the transfer characteristics of NMOS transistor with and without BPW. The back bias voltage is applied to the NMOS transistor and is varied from 0

TABLE 3.3: TEG Transistor parameters.

Transistor	L(μm)	W(μm)	Comment
M1 (NMOS/PMOS)	0.2	100	Normal Vt body floating
M2 (NMOS/PMOS)	0.2	100	Low Vt body floating
M3 (NMOS/PMOS)	0.35	175	High Vt body floating IO
M4 (NMOS/PMOS)	0.35	175	Low Vt body floating IO
M5 (NMOS/PMOS)	1	175	Normal Vt source tie IO
M6 (NMOS/PMOS)	0.2	100	Normal Vt body tie
M7 (NMOS)	10	100	Depletion IO

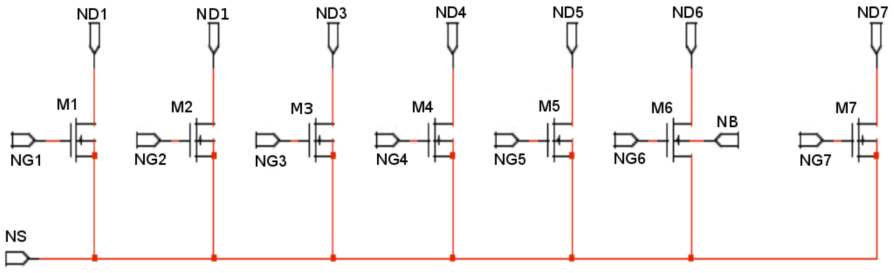

FIGURE 3.8: Circuit diagram of NMOS test transistor.

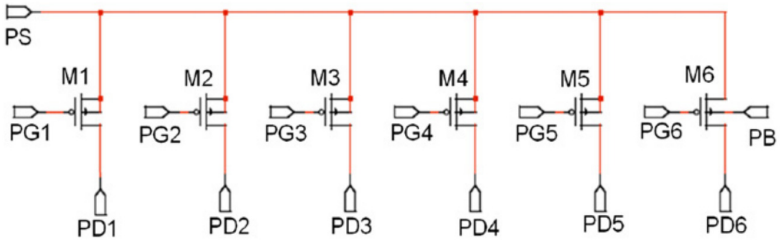

FIGURE 3.9: Circuit diagram of PMOS test transistor.

– 100 V, see figure 3.10. The guard voltages are grounded and a 100 mV of drain to source voltage is applied and kept constant. When the back bias voltage increases the threshold of the NMOS transistor changes and this continues until the transistor stops working properly (see figure 3.10 left). This effect is nothing but back gate effect. Similar measurement was done using PMOS transistor and observe shift in transistor threshold. In case of transistors provided with BPW no change in the characteristics was recorded (see figure 3.10 right). Practically, transistors without BPW are not operational above 30 V of back bias voltage because of back gate effect.

3.4 INTPIX3 detectors

As discussed earlier the INTPIX3 is a detector prototype designed in 2009 by KEK in collaboration with OKI. It was implemented in the 200 nm fully depleted SOI CMOS

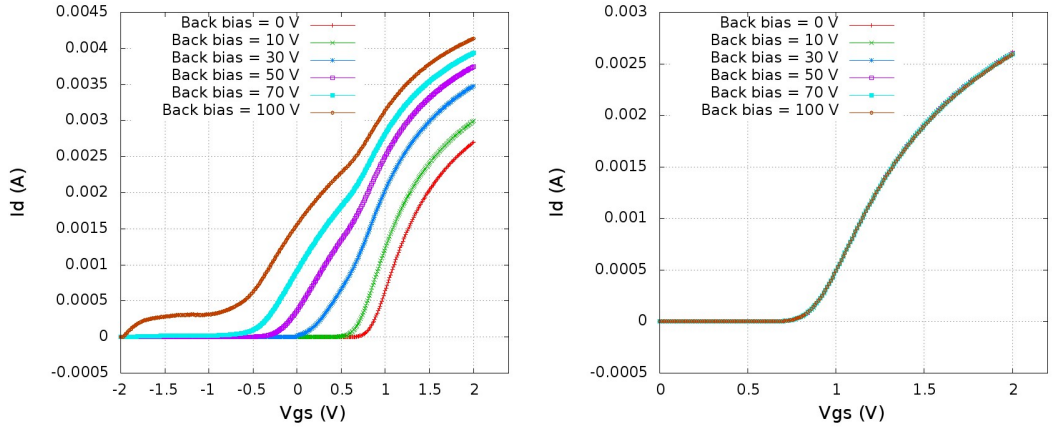

FIGURE 3.10: Transfer characteristic of NMOS transistor without BPW (left) and with BPW (right).

process. Several flavours of INTPIX3 have been designed till to date. In this work only two prototypes (INTPIX3a and INTPIX3b) were studied in detail. The architecture, pixel circuitry and layout of both detectors are explained in this section. Long time stability test, performance using laser, and the noise performance of both detectors were measured using Am-241 source and compared.

3.4.1 Architecture

The INTPIX3a and INTPIX3b are two different detector prototypes with the same architecture and pixel circuitry. The size of the chips is 5 x 5 mm^2. It consist of 128 x 128 pixels on the chip and the pixel size is 20 x 20 μm^2. The CZ-n type wafer is used, which has a resistivity of 700 Ω cm. Figure 3.11 shows the block diagram of INTPIX3a and INTPIX3b. At the periphery a row and a column address decoders, a control logic, and a reference voltage generator (BiasV) are available. The address of the pixel can be specified by selecting the horizontal (RA[6:0]) and vertical (CA[6:0]) addresses. The output is sent to an analogue output buffer and a specified pixel can be readout through the AOut terminal. Each column is provided with column buffer and the output of the selected pixel in that row is transferred to the column buffer. The same operation is repeated till all pixels are readout.

In figure 3.12 the schematic of single pixel circuit is shown. The PMOS (M1) transistor is used as a protection diode and the NMOS (M2) transistor is used as a reset switch. The reverse bias voltage is applied to +Vdet and the reset voltage is applied through the Reset Voltage (RSTV) terminal. When the detector is illuminated with visible laser light, the detected signal is buffered by the source follower (M3). The signal is stored temporarily in the Cstore (100 fF) capacitor and the signal sampling is controlled by the STORE terminal at NMOS (M5) transistor. Finally the signal is amplified by PMOS

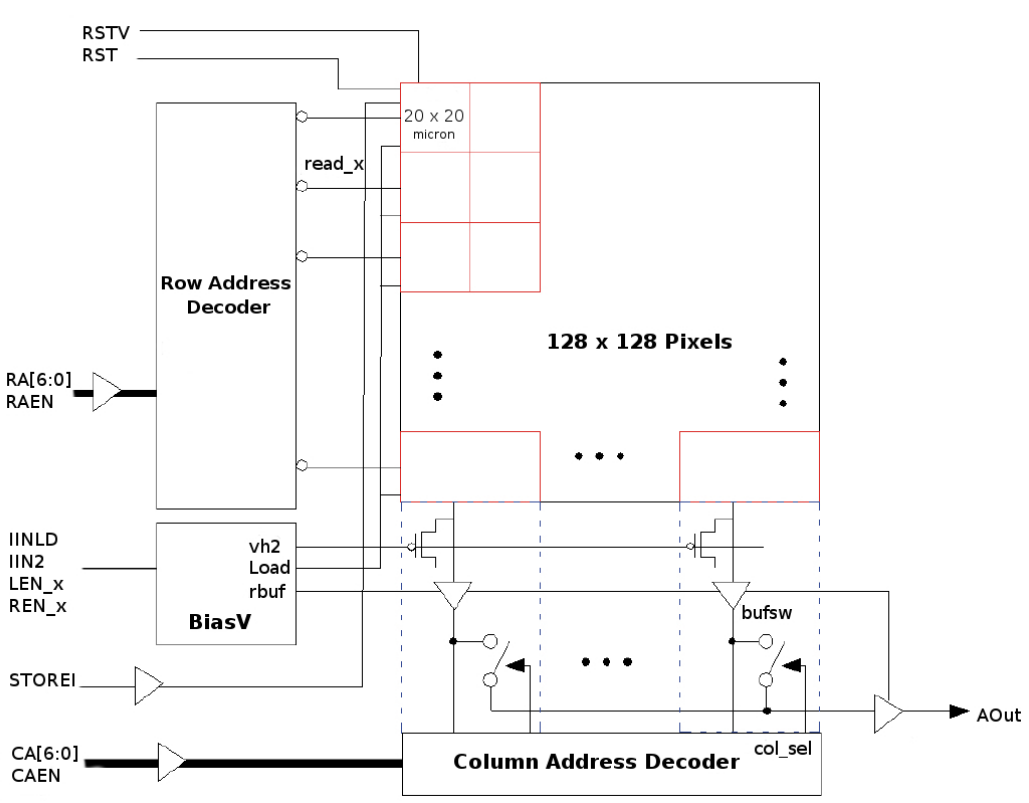

FIGURE 3.11: INTPIX3 block diagram.

transistor (M6) and the digital read signal (read_x) of PMOS (M7) transistor connects the pixel output to the common readout line.

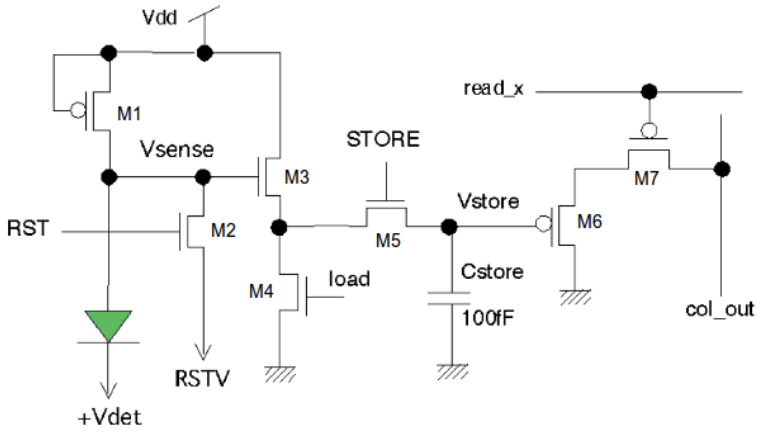

FIGURE 3.12: Single pixel circuit of INTPIX3.

Layouts

The layouts of both INTPIX3 detector prototypes (INTPIX3a and INTPIX3b) are shown in figure 3.13 and 3.14 respectively. In order to test the effect of the BPW, different area and shape of the p+ electrode and BPW were implemented. Two detectors, INTPIX3a

and INTPIX3b, with 16 different pixel type layout topologies were designed. The INTPIX3a is provided with 8 different pixel layouts, out of them the 4^{th} region is similar to INTPIX2 i.e. without BPW. Since the use of BPW in INTPIX3a mitigates the back gate effect (refer to section 3.3), subsequently all designs (including INTPIX3b) are provided with the BPW.

The following are the features and differences between all regions of INTPIX3a and INTPIX3b:

- **Shape of p+ implant:** The shape of p+ implant in INTPIX3a is octagonal and in INTPIX3b it is approximately circular.
- **Number of p+ implant:** The INTPIX3a consists of first four regions with one p+ implant in pixel and next four regions with four p+ implants in pixel (see figure 3.13). All 8 regions of INTPIX3b have only one p+ implant in the pixel centre (see table 3.4).
- **Area of BPW:** The size and shape of BPW and p+ implant varies from one region to the other in both INTPIX3a and INTPIX3b, see figures 3.13 and 3.14.
- **Guard ring:** In INTPIX3a regions 1,2 and 3, and 7^{th} region in INTPIX3b are provided with guard rings, which surround the detector diode to isolate it from the edge of the wafer (mechanical damages at the edge from wafer cutting lead to additional large leakage currents). The guard ring, biassed at the same potential as the detector electrode, captures the edge currents and also forms a well defined electrical boundary for the detector diode.
- **Number of Pixels:** Each region of both INTPIX3a and INTPIX3b contains 32 x 64 pixels.

In subsection 3.4.3 the pixel topologies with guard ring are discussed. The area around transistors and P+ implant in region 1 to 6 of INTPIX3b is provided with BPW and its area and shape is different in each region to optimise the pixel gain. All transistors in the 7^{th} region of INTPIX3b are placed at the corner of the pixel and covered with BPW without covering the P+ implant. Whereas the transistors of 8^{th} region of INTPIX3b are placed close to the P+ implant and both (transistor and P+ implant) are covered with BPW.

3.4.2 Stability test

All 8 regions of detector INTPIX3a and INTPIX3b are measured in dark without any (laser or Am-241) signal and it is found that the output voltage increases with time and

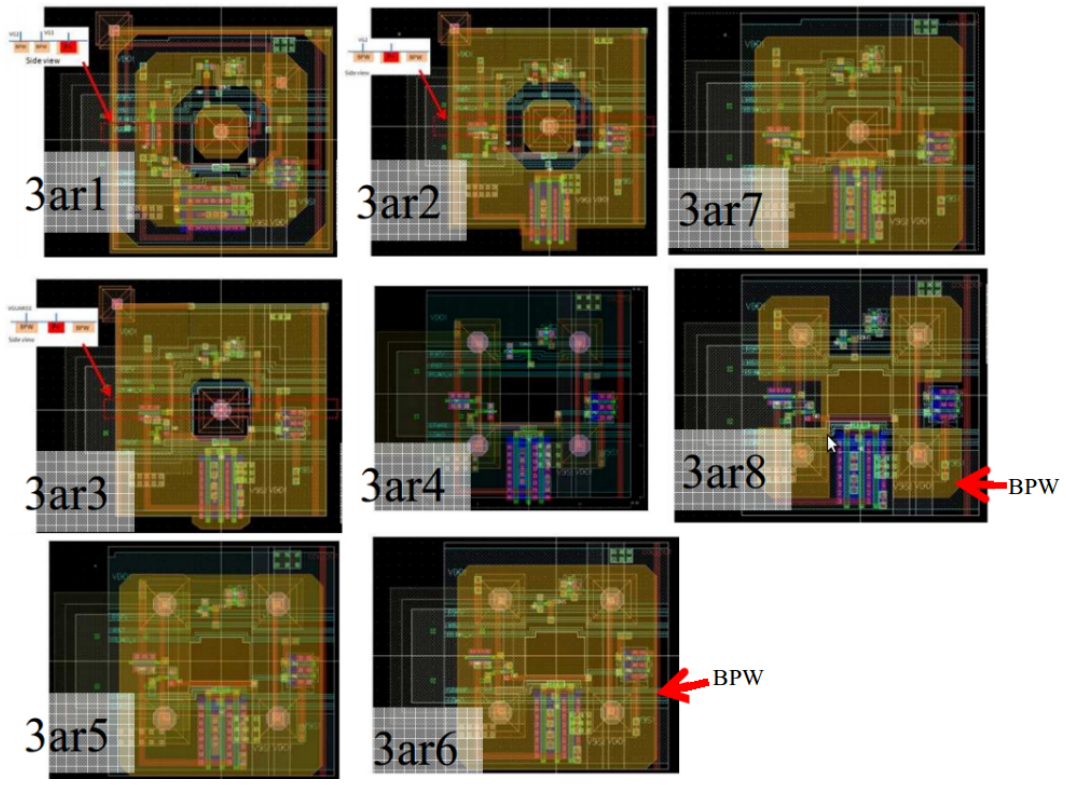

FIGURE 3.13: Pixel layout of INTPIX3a.

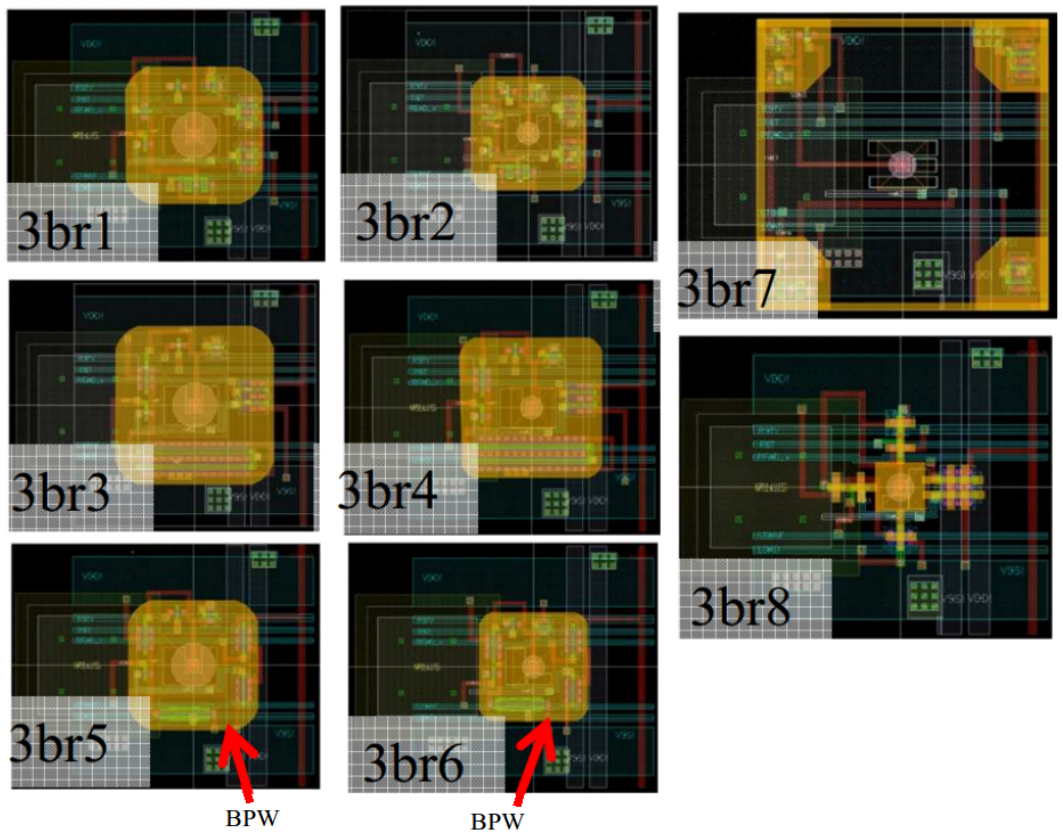

FIGURE 3.14: Pixel layout of INTPIX3b.

TABLE 3.4: Pixel layout topologies.

Pixel type	INTPIX3a	INTPIX3b
Region 1	1p[a] BPW + 2 Ext.[b] BPW	1p[a] BPW
Region 2	1p[a] BPW + 1 Ext.[b] BPW	1p[a] BPW
Region 3	1 Ext.[b] BPW	1p[a] BPW
Region 4	INTPIX2 (4p[a])	1p[a] BPW
Region 5	4p[a] BPW	1p[a] BPW
Region 6	4p[a] BPW	1p[a] BPW
Region 7	1p[a] BPW	1p[a] Tr.[c] covered with BPW
Region 8	4p[a] BPW Tr.[c] are not covered	1p[a] Tr.[c] covered with BPW

[a] P+ implant
[b] External
[c] Transistor

higher slope is observed for larger bias voltages, for example the pixels output behaviour of the 6^{th} region of both detectors is shown in figure 3.15. Figure 3.15 shows the pixel output behaviour with time for both detectors INTPIX3a (left) and INTPIX3b (right). After averaging every 10 frames, the pixel outputs (expressed in ADC counts) are used to show the time stability plot. Data is taken continuously till the detector reaches saturation. Due to the maximum frame limit in the DAQ, 70000 frames per run is possible. The complete measurement last for 90 minutes. For ease of understanding, only two pixels are selected from the 6^{th} region of both detectors to study the long time stability. This shows that these detectors cannot be used for long run, as most of their pixels are going to saturate after approximately 1 hour run. The parameter settings are shown in table 3.5. Except the detector bias voltage all other parameters are the same for both detectors.

TABLE 3.5: Parameter setting of detector INTPIX3a and INTPIX3b for stability test.

Parameters	INTPIX3a(fig:3.15 left)	INTPIX3b(fig:3.15 right)
Environment	Dark	Dark
Signal	No	No
Frames	70000	70000
Back Bias	100V	80V
Integration Time and Scan Time	500μs, 1000 $ns/pixel$	500μs, 1000 $ns/pixel$
RSTV and RST Length	750 mV, 240 ns	750 mV, 240 ns
Readout Frequency	95 Hz	95 Hz

In principle each pixel should reset after every frame and if there is no signal in the detector the raw pixel output (ADC count) should be constant. But it was found that ADC count of both detectors are adding up frame by frame till reaching saturation. It is difficult to give exact reason of this effect but most probably the pixel reset connection is not working properly and/or there is a problem of overheating. To avoid this saturation effect, all following measurements are started after 5 minutes of switching on the set-up

and the measurements do not last for more than 15 minutes. After every 15 minutes of measurements the same steps were followed for the next measurements, and also the measurements were done at constant room temperature.

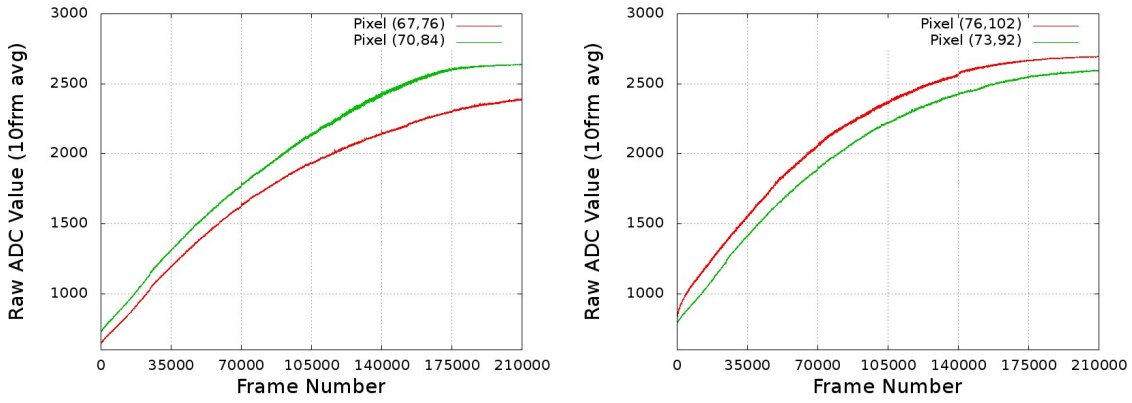

FIGURE 3.15: Raw pixel output (in ADC counts) as a function of time (frame number) for 6^{th} region of detector INTPIX3a (left) and INTPIX3b (right).

3.4.3 Measurements of Pedestal vs Bias voltage

The analysis of the pedestal shift is done in the readout test bench, based on the Soi EvAluation BoArd with Sitcp (SEABAS) [128] readout board. A set of macros in c++ using Root was written to analyse the data.

All eight regions of INTPIX3a were measured to observe the stability of raw pixel output as a function of the detector bias voltage, see figure 3.16. Two tests were done, one with floating guard voltage and other with constant guard voltage. The parameter setting is shown in table 3.6. The back bias voltage is increased with a steps of 5 V and for every measurement, the mean of 500 frames is calculated and recorded for all the regions. Figure 3.16 shows the mean of raw pixel output for all eight regions of INTPIX3a. It is seen that for 4^{th} region without BPW layer the pedestals increase with the increase of the back voltage. No pedestal shift or small shift in other regions, confirms that the back-gate effect is eliminated by the introduction of BPW layer. In figure 3.16 (left) the curves for region 1,2 and 3, measured with floating guard voltage, show slight increase of the pedestal values. This is stabilised by applying a constant guard voltage, as can be seen in figure 3.16 (right).

3.4.4 Detector performance using IR laser

The pixels for vertex detector are generally studied by using a radioactive source or radiation beams from particle accelerators. However, the availability of accelerator and

TABLE 3.6: Parameter setting of INTPIX3a for bias voltage scan to study the pedestal shifts.

Parameters	floating guard voltage	constant guard voltage
Environment	Dark	Dark
Signal	No	No
Frames	500	500
Guard Voltage V_{g1}, V_{g2}	floating	gnd, 1.8 V
Integration Time and Scan Time	500μs, 1000 $ns/pixel$	500μs, 1000 $ns/pixel$
RSTV and RST Length	750 mV, 240 ns	750 mV, 240 ns
Frequency	95 Hz	95 Hz

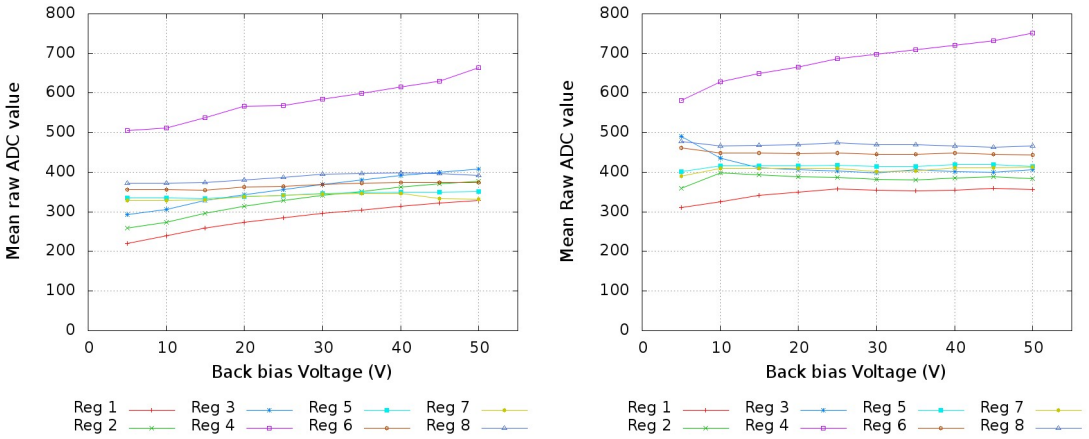

FIGURE 3.16: Mean raw pixel output (in ADC counts) as a function of detector bias voltage of INTPIX3a, floating (left) and constant (right) guard voltage (Pedestal Shift).

its cost are the main issues. Nowadays most of the reported test set-ups of vertex detectors are equipped with pulsed laser system for evaluation of pixel detectors [129, 130, 131, 132]. A laser system is used in the laboratory to have a fully controllable source and high event statistics. Beside these advantages, the cost of these measurements is low and they are readily available. To elucidate the measurements, the estimation of the spot size of the laser at a focal distance from the detector is important. The laser with 660 nm wavelength is used to study the performance of INTPIX3a detector. The 8^{th} region of INTPIX3a is used to study the performance with IR laser, because it has smaller area of BPW what results in higher gain.

Laser spot size and Pixel scan

The optimum distance between the laser and the detector is found by searching for the smallest spot size for the 660 nm laser. The 3-D step motor is used to move the detector towards the laser in the focal plane. Figure 3.2 shows how the set-up look like.

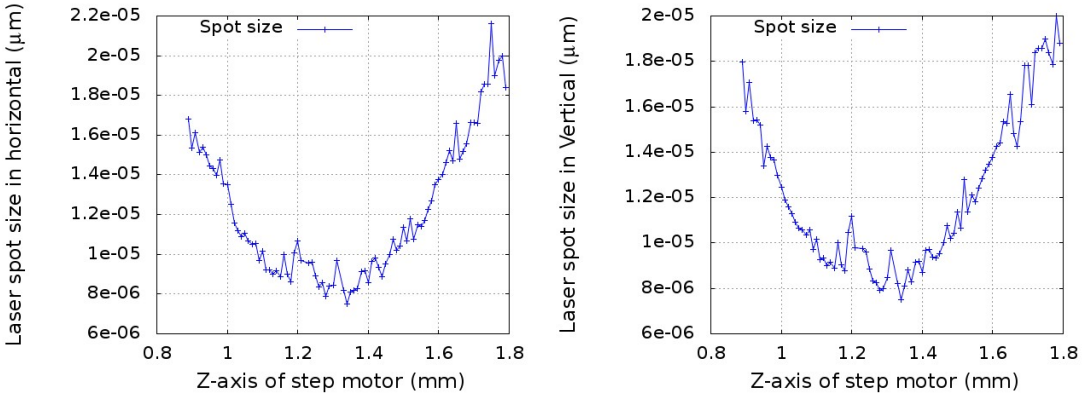

FIGURE 3.17: Spot size of hit pixel (with 660 nm laser) is calculated in Horizontal (left) and Vertical (right) direction with respect to distance between laser and detector for 8^{th} region of INTPIX3a.

The pixels of the detector are illuminated by the laser and the spot size of the laser is estimated. The cluster of hit pixels is found and the weighted mean and weighted sigma of the cluster are calculated in horizontal and vertical direction. The laser spot size is calculated from the weighted cluster sigma and plotted along the distance between the detector and the laser, see figure 3.17. The spot size of the laser is the smallest at focal distance from the detector and if this distance is increased or decreased the spot size increases, as seen in figure 3.17. To obtain the focal distance, the laser is moved towards the detector till a smallest spot size is achieved. A 2-D histogram for single pixel with the smallest spot size is shown in figure 3.18. From figure 3.17, it is clear that the spot size of the laser at a focal distance is about 8 μm in horizontal and vertical direction.

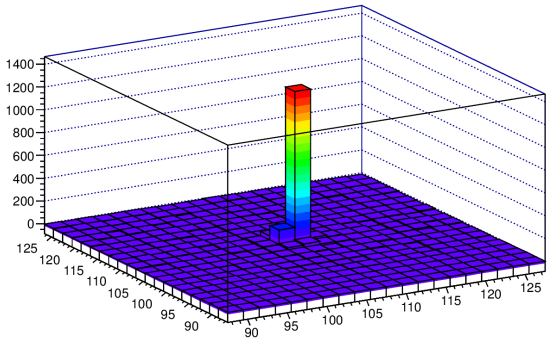

FIGURE 3.18: 2-D laser histogram of single pixel for 8^{th} region of INTPIX3a.

Two pixels each 20 x 20 μm^2 were scanned with a step size of 5 μm along the pixel row and column. Pixel scan is done to see the linearity of the measured laser position in the detector using the laser position on 3-D step motor. The weighted mean and sigma of the hit pixels cluster were calculated. The weighted cluster mean value represents the pixel position and the weighted cluster sigma represents the spread of cluster (laser spot size). Figure 3.19 shows the pixel position scan of INTPIX3a in X (left) and Y (right) direction. It confirms that the laser movement in Y-axis (see figure 3.19 right) is linear

with the measured weighted mean position of the laser on detector Y-axis. In X-axis the measurement result is slightly less liner.

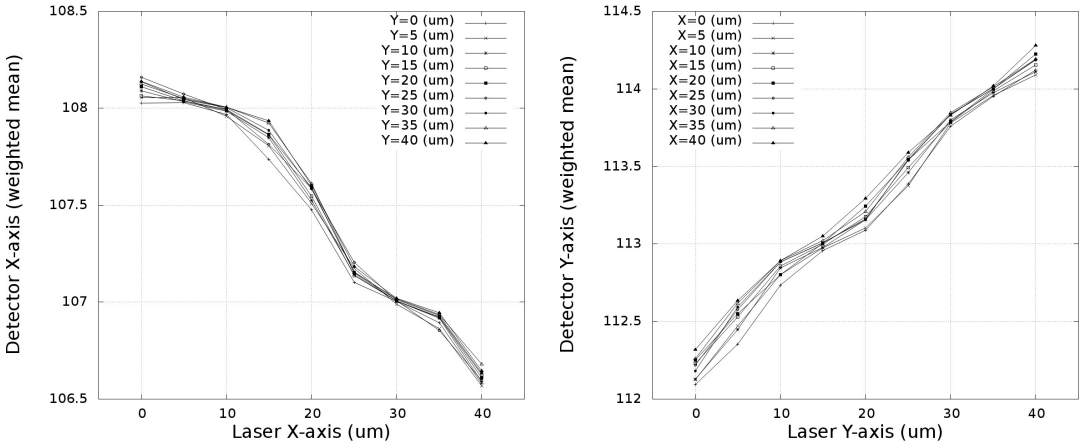

FIGURE 3.19: The weighted mean of the cluster of hit pixel (with laser) is calculated with respect to laser position. The laser is moved by 40 x 40 μm with a step of 5 μm.

3.4.5 Measurements using Am-241 source

The low energy gamma radiation interacts with the detector material and generates number of electron-hole (e-h) pairs in the detector. An active detector volume is created by applying bias voltage and e-h pairs drift towards the electrodes under the influence of electric filed. In this measurement, the Am-241 is used as a gamma radiation source. Both SOI detector prototypes INTPIX3a and INTPIX3b were examined to find the ENC and the gain of the detector. The test set-up and radiation data of Am-241 source was described in section 3.2.1. The measurements and analyses to calculate the ENC is shown for the 6^{th} region as an example. The same analyses were applied to all regions of INTPIX3a and INTPIX3b detector to perform the comparison. The algorithm for cluster finding and data analyses were described in section 3.2.3 and 3.2.4. The offline method was used to analyse the low energy gamma radiation.

The measurements were done using the parameters shown in table 3.7. The detector back bias voltage was 100 V and guard voltages V_{g1} and V_{g2} were set to ground and 1.8 V respectively.

Data cleaning

The data cleaning and analysis was done using offline algorithm. Initial frames are rejected and averages of the pedestals are calculated for each pixel from the pedestal run, and it is subtracted from the raw ADC values. The effect of initial frames can be

TABLE 3.7: Parameter (DAQ-GUI) setting of INTPIX3a and INTPIX3b detectors for Am-241 source measurements.

Intergration time and scan time	500 μs, 1000 ns/pixel
RSTV and RST length	750 mV , 240 ns
Frequency	95 Hz
Run mode	calib and data
Calib run	500 events (In black box without Am-241 source)
Data run (with source)	5000 events (In black box with Am-241 source)

seen in figure 3.20 (left). When considering the initial 50 frames from the pedestal run a left shoulder is visible and this effect is easily removed by rejecting initial frames, see figure 3.20 (right). The CM noise is removed and later the bad pixels are masked by considering the sigma level of each pixel (see section 3.2.4). The final histogram of the pedestals after data cleaning is shown in figure 3.21. As illustrated, the Gaussian shape of the pedestal distribution was restored and the standard deviation of the data was significantly reduced by suppression of the common interference and noise.

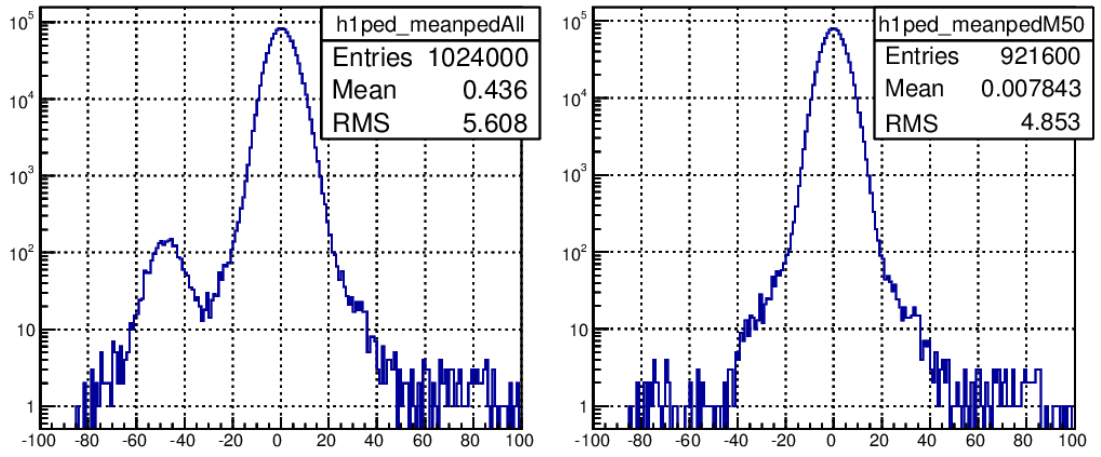

FIGURE 3.20: Effect of Initial Frames before (left) and after (right) initial frame removal (6^{th} region of INTPIX3a).

The same procedure as explained above is applied in the signal run to plot the Am-241 spectrum. An example of measured spectrum with shoulders indicating the presence of gamma lines from Am-241 source can be seen in figure 3.22. Since it is not straightforward to identify all gamma peaks (refer table: 3.1) from the Am-241 hit spectrum pixel distribution, in the next section the distributions of cluster of pixels (corresponding to gamma events) will be produce rather than the distributions of single pixels.

Analysis

The groups of hit pixels were identified using the cluster algorithm described in section 3.2.3 to find the clusters representing X-ray events. Since the alpha's are blocked by a

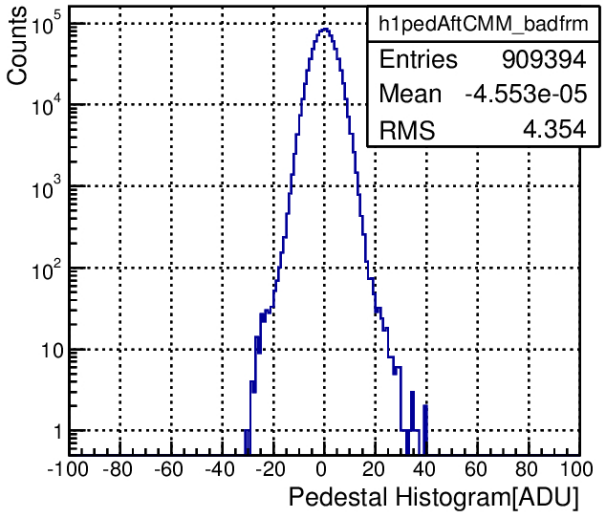

FIGURE 3.21: Histogram of the Pedestal after common mode rejection and masking bad pixel (6^{th} region of INTPIX3a).

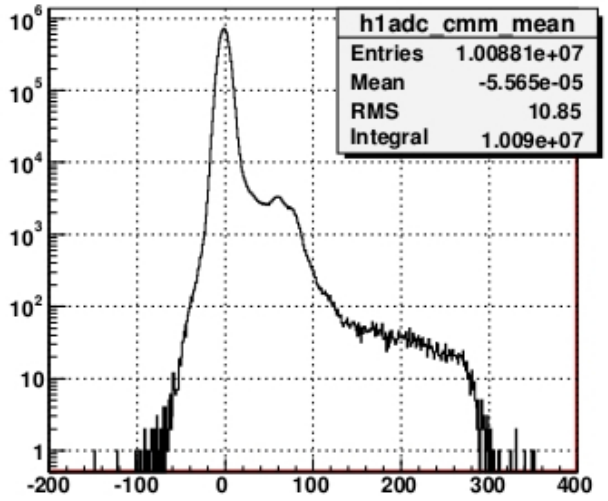

FIGURE 3.22: Histograms of Am-241 hit spectrum pixel distribution with noise peak and the right shoulder indicate the 59.5 keV peak (6^{th} region of INTPIX3a).

mask and only the X-ray lines can generate charge in the pixels. In order to find pixels with the signal above noise, equation 3.3 was used:

$$adc[i][j] >= mean\_adc[i][j] + (5.5 * sigma\_ped), \tag{3.3}$$

$$i,j = pixels\ number$$

If the condition in 3.3 is true then those pixels are supposed to be hit by X-rays of Am-241 source. Number of pixels hit depends on energy and intensity of the X-ray line. In principle each X-ray event may create one, two or more hit pixels and in practise it was enough to study 1, 2, 3, and 4 pixel clusters. Figure 3.23 shows the histogram after

merging 1, 2, 3, and 4 pixel clusters. All the peaks seen in the histogram are fitted and the mean value of each peak represents the energy in ADC count. Three low energy X-ray lines (13.9 keV and 17.7 keV and 26.3 keV) and a more pronounced peak representing 59.5 keV line from Am-241 source at 273 ADC counts are clearly seen.

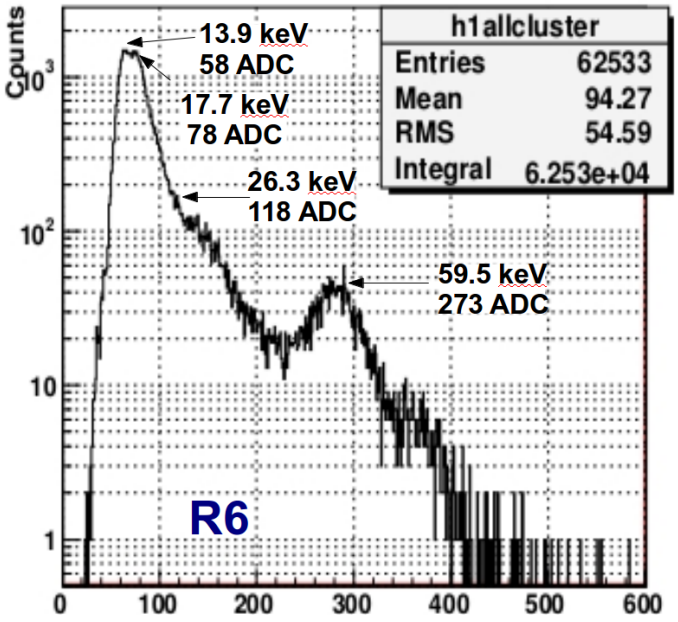

FIGURE 3.23: Histogram after merging all clusters and the peaks indicate the energy of Am-241 in ADC count (6^{th} region of INTPIX3a).

The separate distributions of single, double, triple, and quadruple pixel clusters are shown in figure 3.24. Depending on the photon energy, different clusters are created. It is seen that the 13.9 keV has a highest probability to hit single pixel, corresponding to large number of entries in figure 3.24 (top left). On the other hand the 26.3 keV line is best seen in triple pixel clusters distribution, see figure 3.24 (bottom left), while the 59.5 keV line is seen well in double, triple, and quadruple pixel clusters distributions.

Comparison of INTPIX3a and INTPIX3b

The measurements results of both detectors are compared and discussed. The histograms of hit (and noise) distributions for all regions of both detectors INTPIX3a and INTPIX3b are seen in figures 3.25 and 3.26. First three regions of detector INTPIX3a and 7^{th} region of INTPIX3b are provided with external guard ring. Guard rings are provided in the design to isolate the edge of the wafer. After providing the required guard voltages to these regions there is no good response to Am-241 source, as seen in figure 3.25 and 3.26. The right shoulder of these histograms had a very small number of hits and it is impossible to identify the X-ray lines of Am-241. The 4^{th} region of INTPIX3a has a

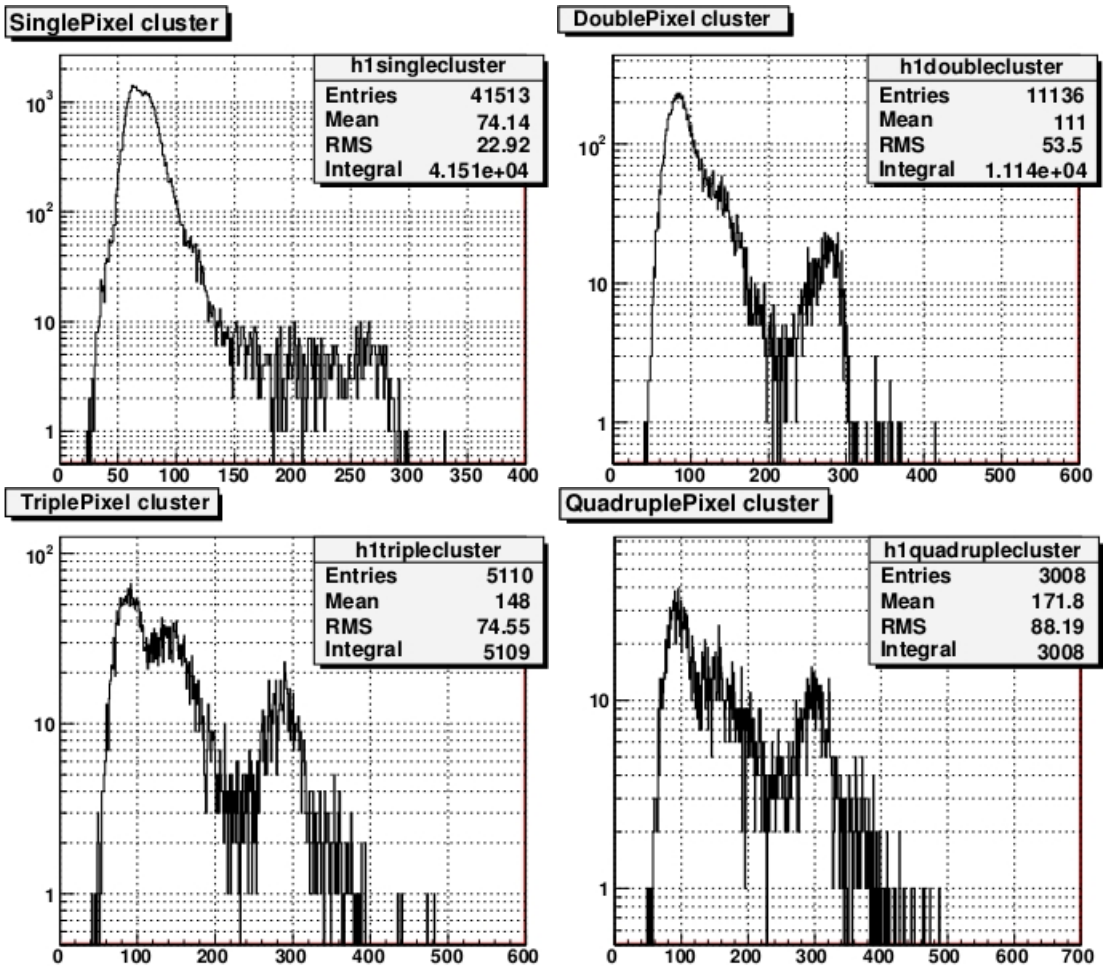

FIGURE 3.24: Histograms of single pixel (top left), double pixel (top right), triple pixel and quadruple pixel clusters are produced after exposing the detector to Am-241 source (6^{th} region of INTPIX3a).

problem of back gate effect[2] and this region of the detector has higher gain. The gain of other regions is smaller compared to 4^{th} region due to the presence of BPW layer. Whereas in 8^{th} region only transistors are covered with BPW and the rest is without BPW (see figure 3.14), this result in higher gain similar as in the 4^{th} region and also mitigates the back gate effect. The performance of 5^{th}-8^{th} regions of INTPIX3a with Am-241 source shown in figure 3.25 is pretty similar to 4^{th} region. Looking a bit closer, a finer lower energy (13.9KeV, 17.7KeV) X-ray peaks structure is seen in 5^{th} - 8^{th} regions. The best region seems to be the 8^{th} region where the peaks are most pronounced. The total gain of the whole readout chain of 8^{th} region of INTPIX3a is 6.6 $\mu V/e^-$ (see figure 3.29).

The INTPIX3b detector produces the results at least the same good compared to INTPIX3a. Particularly, the regions 6^{th} and 8^{th} shown in figure 3.26, apart from having higher gain, show a very good response to monochromatic lines from Am-241 source.

[2]Back gate effect was discussed in section 3.1

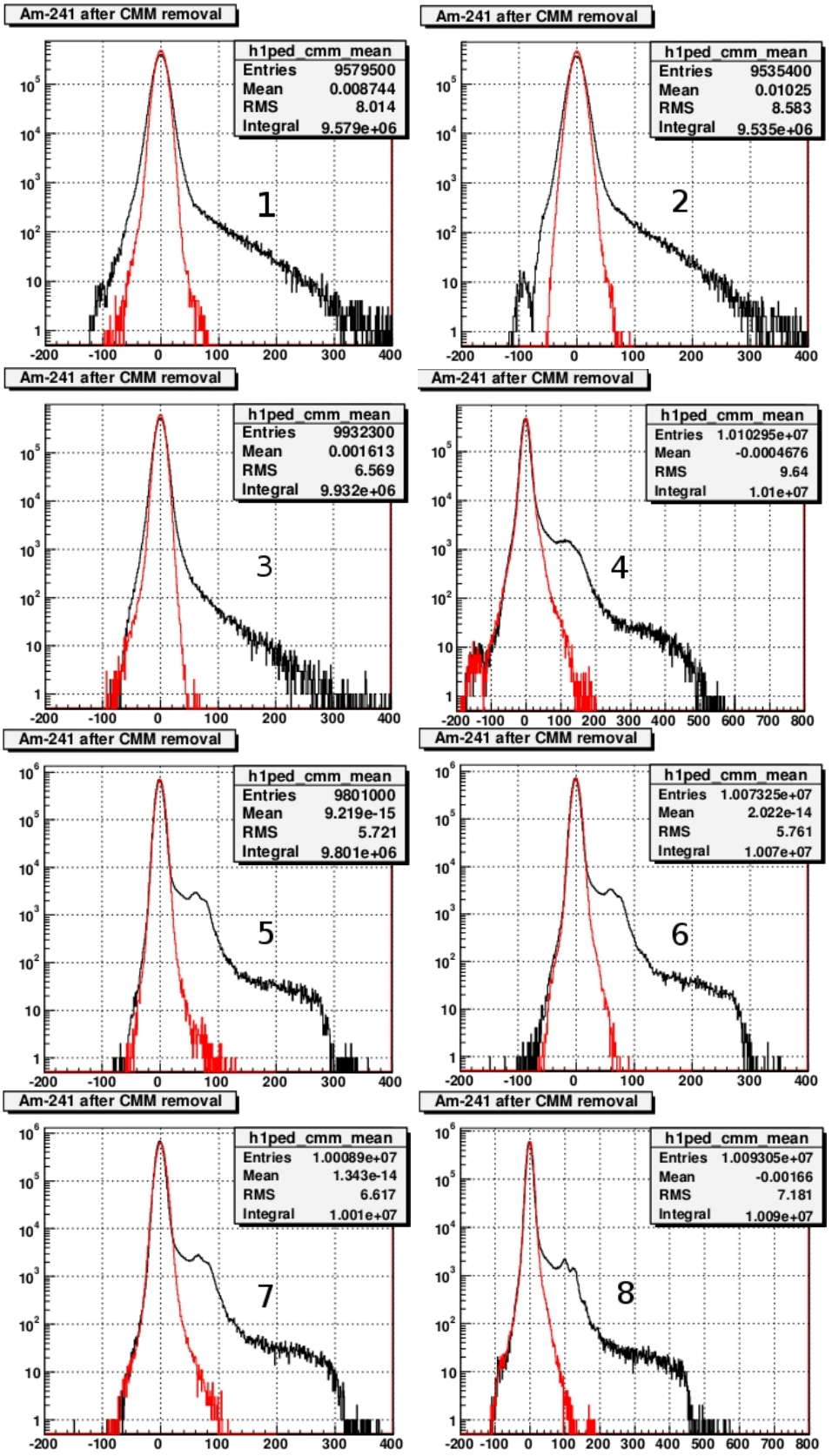

FIGURE 3.25: Histogram of all region in INTPIX3a. The pedestals are represented in red and the signal from Am-241 is represented in (black). (The numbers in the figure indicate the region number of INTPIX3a).

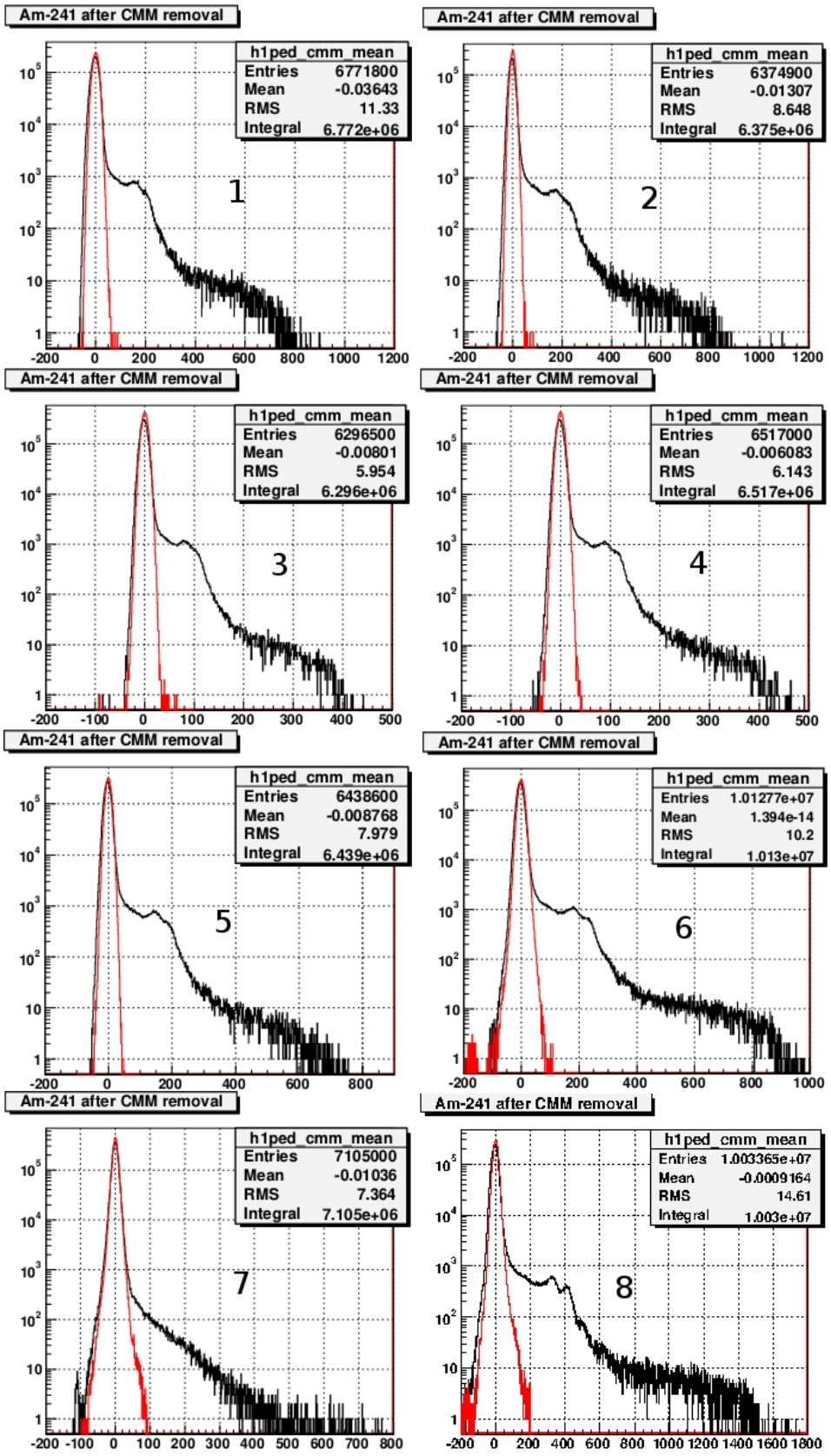

FIGURE 3.26: Histogram of all region in INTPIX3b. The pedestals are represented in red and the signal from Am-241 is represented in (black). (The numbers in the figure indicate the region number of INTPIX3b).

The merged histograms of pixel cluster distributions for all regions of both detectors can be seen in figures 3.27 and 3.28.

TABLE 3.8: Comparison of Noise and ENC of regions of INTPIX3a and INTPIX3b.

INTPIX3a			
Region	Noise σ (ADC)	ENC(e^-)	Mean of 59.5KeV (ADC)
1	9.27	-	-
2	11.06	-	-
3	6.67	-	-
4	8.26	245	549.6
5	4.40	260	276
6	4.35	260	272.7
7	4.92	280	286.2
8	5.06	186	444.4
INTPIX3b			
1	11.98	279	700.7
2	9.82	200	799.8
3	6.50	283	374.8
4	6.80	271	409.4
5	8.8	291	668.3
6	10.20	205	810.3
7	10.13	-	-
8	14.61	168	1422

The table 3.8 shows the noise, ENC and the mean signal for 59.5 keV energy. The ENC was calculated by using the peak position of 59.5 keV and noise sigma. No signal peaks were detected for the regions 1^{st}, 2^{nd} and 3^{rd} of the INTPIX3a and the 7^{th} region of the INTPIX3b. So, for the comparison these regions are not used. The 8^{th} region of INTPIX3a and 8^{th} region of INTPIX3b detector have the best ENC (see table: 3.8) since these two regions have smaller area of BPW in the pixel.

As a confirmation that the 8^{th} region of INTPIX3b is the best with the lowest ENC, one can see that apart from the discussed earlier Am-241 lines, a 8.01 keV copper line is seen as well in the 8^{th} region, see figure 3.28. The total gain of the whole readout chain of INTPIX3b is calculated using the linear fit of all the energies detected from Am-241. Figure 3.30 shows the output gain of the 8^{th} region of INTPIX3b. It is clear that due to small area of BPW (in case of INTPIX3b see figure 3.14) in the pixel, a large gain is observed.

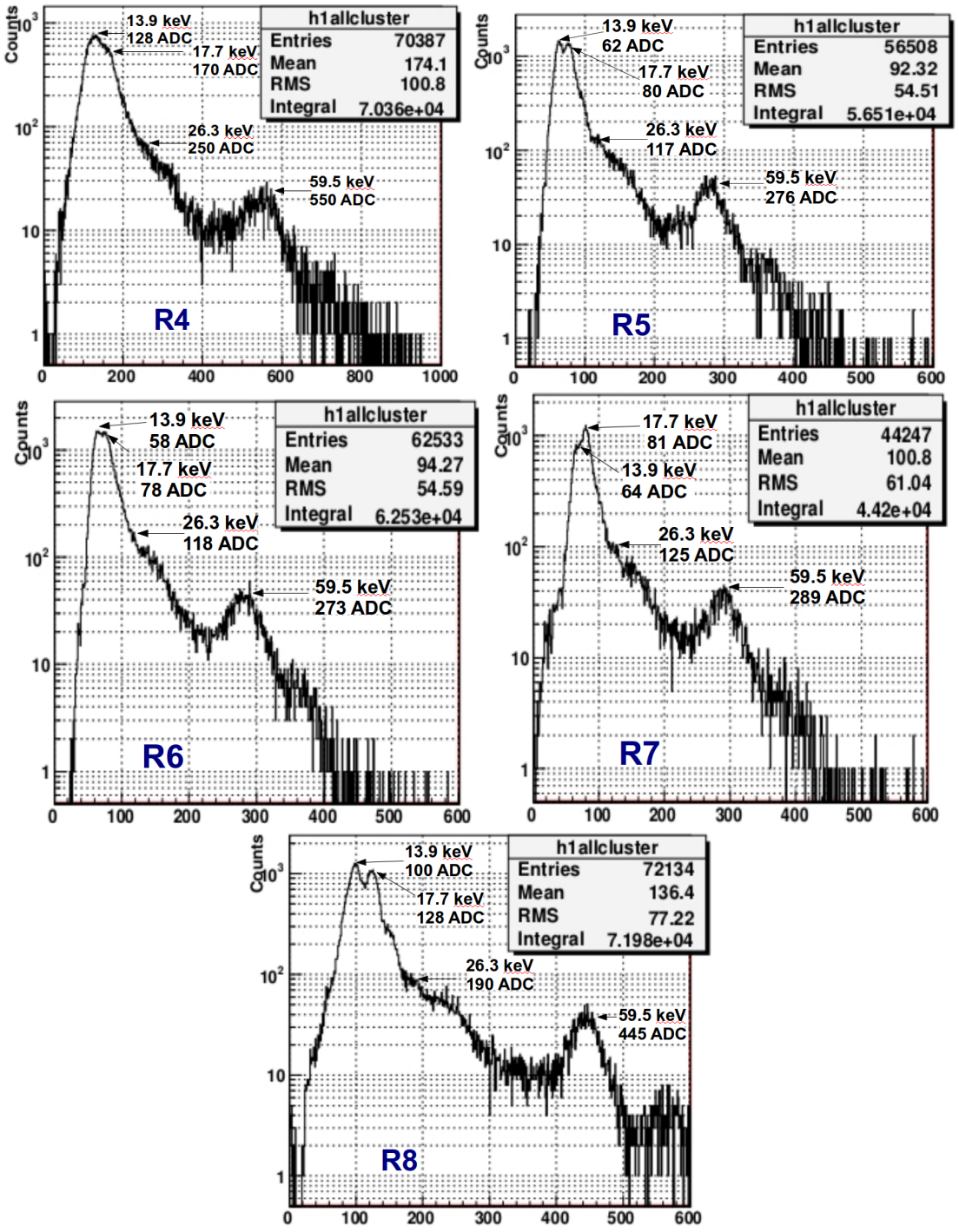

FIGURE 3.27: Histogram after merging all cluster of detector INTPIX3a.

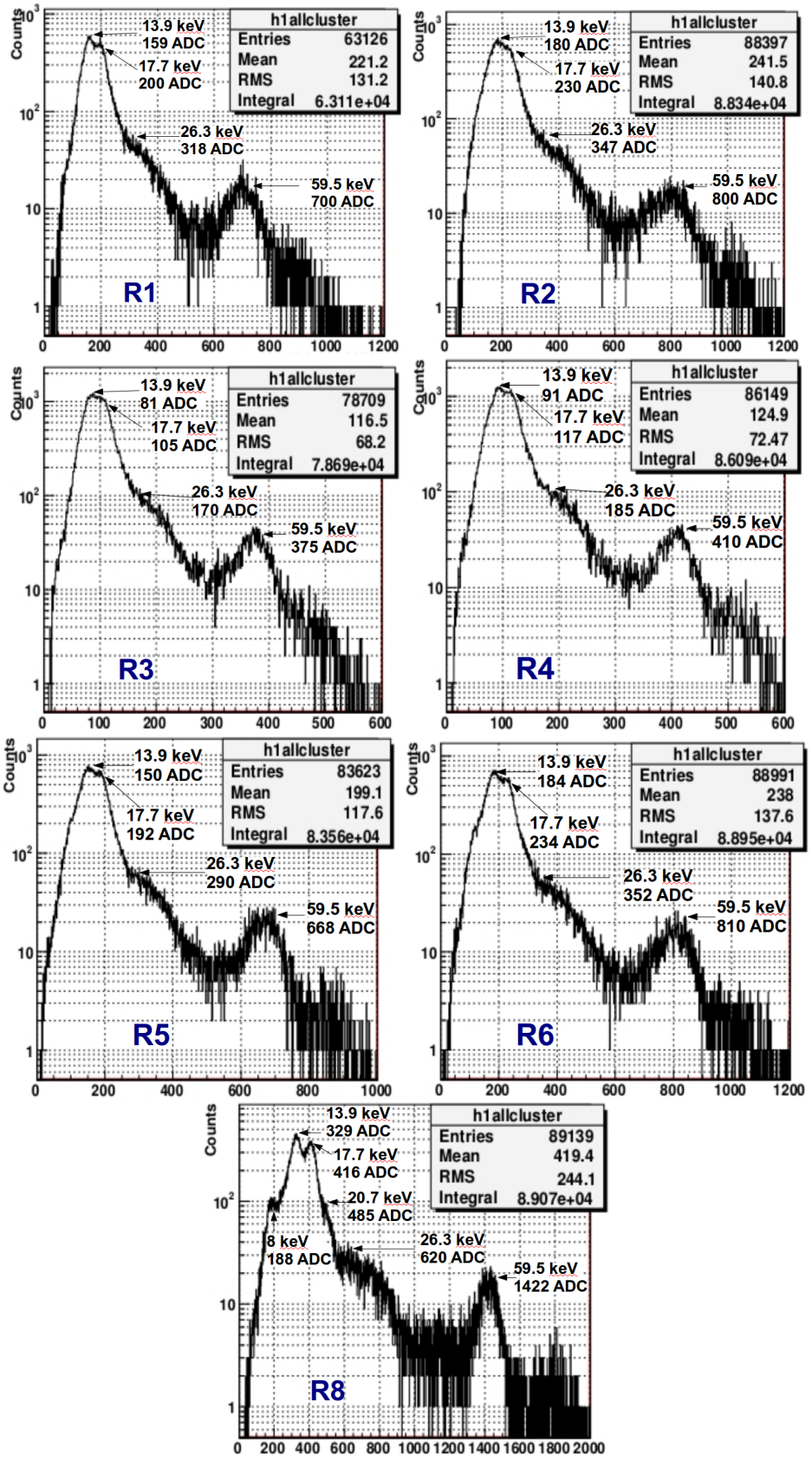

FIGURE 3.28: Histogram after merging all cluster of detector INTPIX3b.

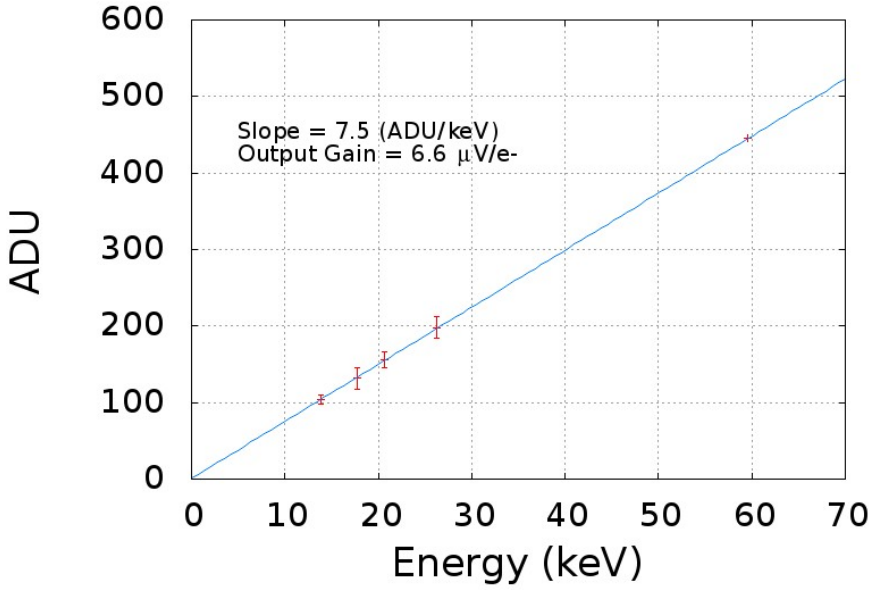

FIGURE 3.29: Output gain of 8^{th} region of INTPIX3a calculated using the linear fit of Am-241 spectrum.

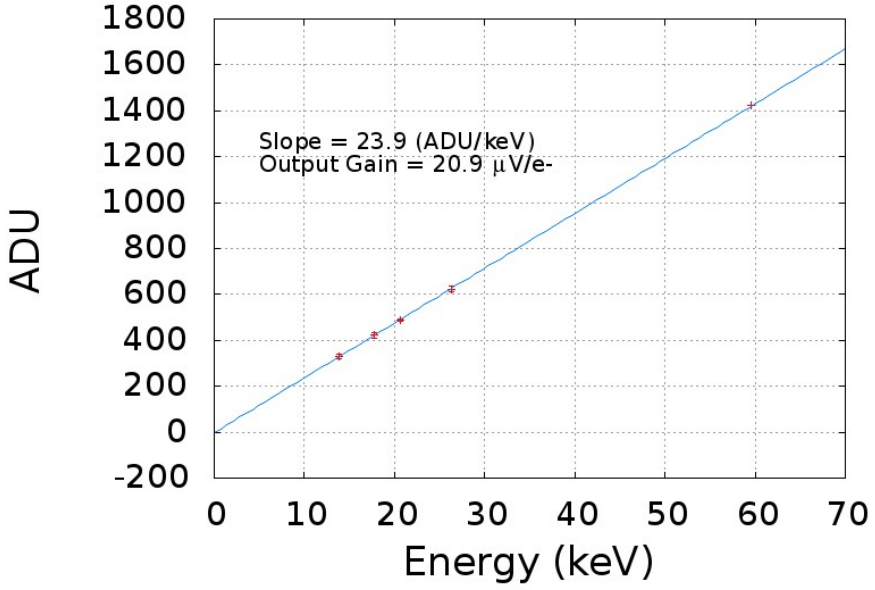

FIGURE 3.30: Output gain of 8^{th} region of INTPIX3b calculated using the linear fit of Am-241 spectrum.

Chapter 4

DIPIX2 detectors

After successfully mitigated the back gate effect discovered in INTPIX2, KEK has designed several new detectors including the family of DIPIX detectors. These detectors were designed as a next step towards particle detection with good performance in radiation environments. They are fabricated in the Lapis semiconductor co., Ltd. (previous name OKI semiconductor) with 200 nm CMOS fully depleted SOI process. These detectors resemble INTPIX but have some additional features, see section 3.1. The pixel circuitry of DIPIX detectors are designed to work with both n-type and p-type wafer. These wafers are produce on the same reticle mask by swapping ion beams [133]. The SOI process allows to fabricate detector using not only a lower resistivity wafer obtained with CZ-n method, but also high resistivity FZ-n and FZ-p wafers. The measurements results and comparison of all these wafers will be discussed in the following sections.

Table 4.1 lists the studied detectors and their parameters in DIPIX family. Two versions of DIPIX detectors are available (DIPIX1 and DIPIX2). The DIPIX1 detector consist of 256 x 256 pixels block, where each pixel size is 14 x 14 μm^2. These detectors were designed with the same pixel circuitry, pixel pitch and chip area. Three different wafers were used with different resistivity. DIPIX2 comprises two pixel layout topologies (2 x 256 x 128 pixels) out of which one (i.e. first half 256 x 128 pixels) is the same as DIPIX1. The measurements results of DIPIX1 detectors are not shown in this dissertation, since the results obtained using laser and Am-241 source for both DIPIX1 and the first region of DIPIX2 are the same. In this work all three DIPIX2 (CZ-n, FZ-n and FZ-p) detectors are measured and compared.

TABLE 4.1: DIPIX Family.

detector parameters	DIPIX1	DIPIX2
CZ-n resistivity (kΩ-cm)	0.7	0.7
FZ-n resistivity (kΩ-cm)	2	2
FZ-p resistivity (kΩ-cm)	7	7
Pixel types per chip	1	2
Pixel size (μm^2)	14	14
No. of pixels	256x256	128x256x2
Chip area (mm^2)	5x5	5x5
Effective area (mm^2)	3.584x3.584	3.584x3.584
Internal ADC	Yes	Yes
CDS in Pixel	yes	yes

4.1 Architecture

Figure 4.1 shows the block diagram of DIPIX. The architecture and pixel circuitry are same for DIPIX1 and DIPIX2 detectors. The serial readout of the pixel array is possible both in analogue and digital modes. The installed on-chip ramp-compare type ADC allows us to readout in digital mode. At the periphery row and column shift registers, a control logic, a reference voltage generator (Bias) and a ramp generator are seen. The analogue readout part is similar to INTPIX3 as described in section 3.4.1. The address decoders in INTPIX3 were replaced with shift registers in DIPIX and this results in sequential addressing. The digital readout is possible using a Wilinson type 10-bit ADC provided for each column. The AOUT1 and AOUT2 are the analogue outputs while the digital output is DO[10:0].

The schematic of the DIPIX2 pixel is shown in figure 4.2. The pixel circuit of DIPIX2 detector is a standard active pixel type with a storage capacitor. The circuit is prepared to work both with the N-type and P-type detectors, biassed with reverse voltage +Vdet or -Vdet. The PMOS (M1) and NMOS (M2) transistors are used as the reset switch and the protection diode respectively for the P-type detector and vice versa for the N-type detector. The input source follower (M3) provides current amplification of the detected signal, charging the storage capacitor (Cstore) of about 100 fF, made with the DMOS transistor. The digital STORE (S1) switch controls the signal sampling while the LOAD source follower bias determines the time constant of the Cstore discharging. The pixels are equipped with the CDS circuit, supposed to reduce the DC level shift of the signal and the kTC noise caused by the reset switch. The initial CDS signal sample is stored on the 82 fF MIM capacitor (C_{cds}). The SKIP (S2) switch is used to enable or disable the CDS operation. The M5 PMOS works as an output amplifier in the source follower configuration. The digital READ signal on PMOS (M6) transistor connects the pixel output to the common readout line. The serial readout of the pixel array is possible both

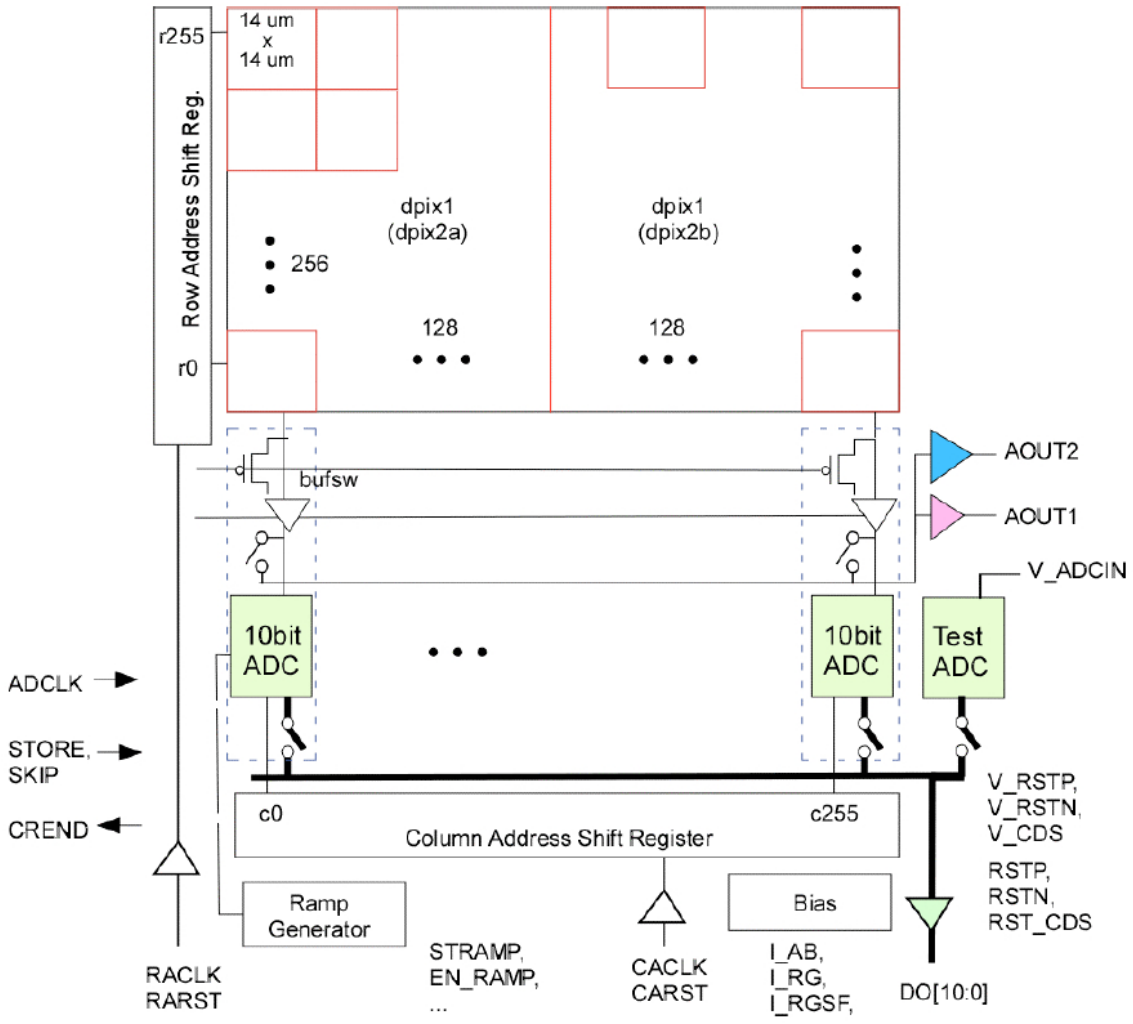

FIGURE 4.1: DIPIX2 block diagram.

in analogue and digital modes, the latter available thanks to the installed on-chip ramp-compare type ADC. An open window area, without the metal coverage, was provided for optical illumination in the centre part of each pixel.

4.1.1 Layouts

The chip layout of DIPIX2 is shown in figure 4.3. The IO pads are placed on two sides of the chip. The DIPIX2 detector consist of two pixel layout topologies and their cross sectional views are shown in figure 4.4. The example layouts shown in the figure are for n-type wafer, for p-type wafer inverse implants are used. Figure 4.4 (top) shows half pixels (region 1) which were processed by adding BPW at p+ implant for n-type wafer and vice versa for p-type wafer. The remaining half pixels (region 2) were processed by adding both Buried N-Well (BNW) and BPW together, see figure 4.4 (bottom). The overlaid electrode BNW (BPW) behaves like n-stop for n-type wafer (p-stop for p-type

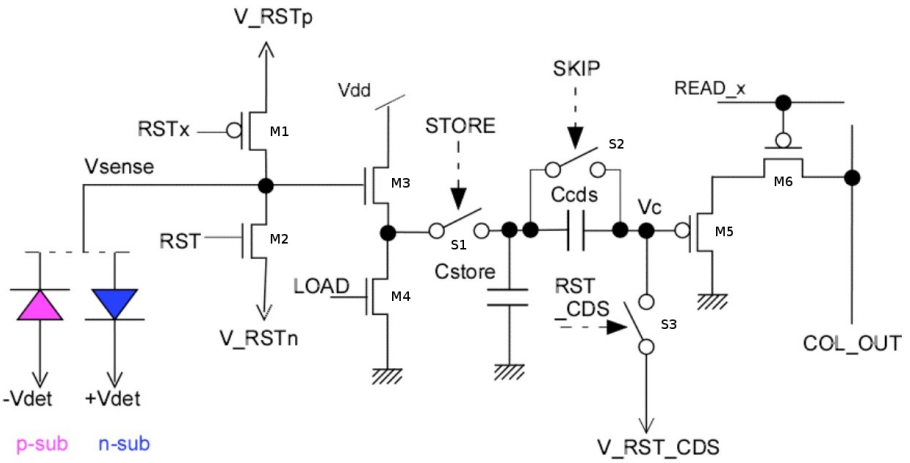

FIGURE 4.2: Single pixel circuit of DIPIX2.

wafer) and it is used to reduce the inter-pixel coupling. However the results obtained from the 2^{nd} region of n-type wafers are not obvious [14]. All measurements presented in the next sections are for the 1^{st} region of n-type wafer and the 2^{nd} region of p-type wafer. The shape of BPW is octagonal and its width is 10 μm (see table 4.2). The p+ implant is almost circular with a size of 1.4 μm at the centre of the pixel. HV ring (Vdet terminal) has been arranged on the outer periphery of the chip and the bias voltage to the detector can be applied at Vdet terminal.

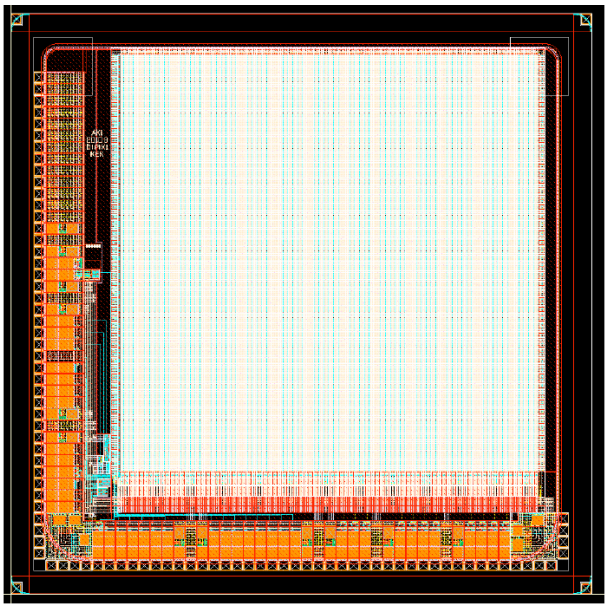

FIGURE 4.3: Chip layout of DIPIX2.

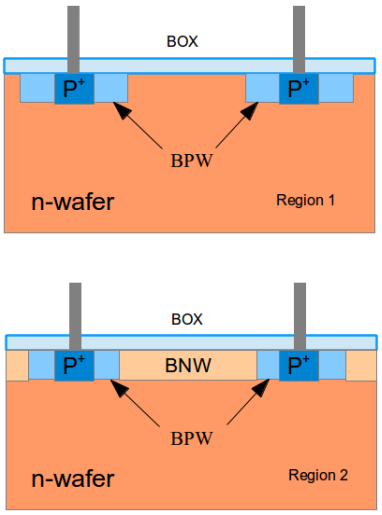

FIGURE 4.4: DIPIX2 N-type pixel layout topology (top: pixel type one and bottom: pixel type two).

TABLE 4.2: DIPIX2 Pixel type topology.

Pixel type	DIPIX2 N-type	DIPIX2 P-type
Region 1	1p BPW(10μm)	1p BNW(10μm)
Region 2	1p BPW(10μm) and BNW[a]	1p BNW(10μm) and BPW[b]

[a]BNW between pixels work as n-stop
[b]BPW between pixels work as p-stop

4.2 Stability test

Stability test done for DIPIX2 is the same as for INTPIX3 (refer to section 3.4.2). The pixels responses are analysed in the dark without any signal. The behaviour of DIPIX2 CZ-n and FZ-n detectors are studied as a function of time. The parameter setting of both detectors are listed in table 4.3. All settings are the same except the back bias voltage, since a Halo effect is seen in FZ-n detector (refer 4.2.1) when the applied detector bias voltage is above 80 V. The outputs after ADC conversion (average of 10 frames) are plotted over time in figure 4.5. Two pixels are selected, each from different region, to study the stability. The measurement is taken continuously for 1 hour and the behaviour is studied skipping by the CDS option. In the figure 4.5 (left) the systematic changes in ADC counts before saturation are probably due to self heating. If constant temperature is maintained for a long run of measurement, this probably can be reduced. As compared to CZ-n detector, the initial change in ADC count for FZ-n is much smaller, see figure 4.5 (right). In case of FZ-p (not shown in the plot) a small change of about 5% in the raw ADC count is observed in the measured data.

TABLE 4.3: Parameter setting of DIPIX2 CZ-n and FZ-n detectors for stability test.

Parameters	CZ-n type	FZ-n type
Environment	Dark	Dark
Signal	No	No
Frames	40000	40000
Back Bias	100	70
Integration time and scan time	500 μs, 640 ns/pixel	500 μs, 640 ns/pixel
RSTV and RST length	750 mV, 2040 ns	750 mV, 2040 ns

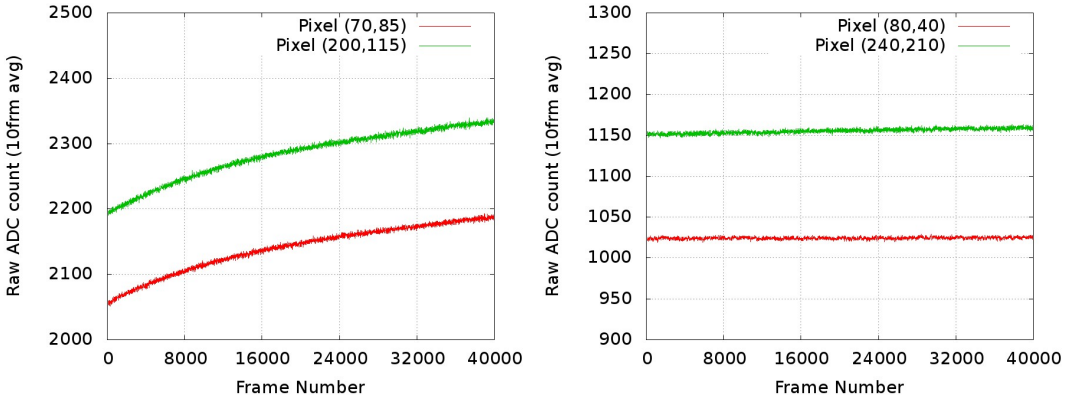

FIGURE 4.5: Long time stability test of DIPIX2 CZ-n (left) and FZ-n (right) detectors, pixel behaviour of two pixels, one from the 1^{st} region and another from the 2^{nd} region, is shown. It may be concluded that the DIPIX2 detector does not have the problem seen in INTPIX3 chip.

4.2.1 Halo in FZ-n detector

Figure 4.6 (left) shows the Halo effect which appears in FZ-n detector [134]. If detector bias voltage is increased above 80 V, the increase in leakage current saturates the detector. At 100 V the whole detector is covered with hits and this is independent of the laser spot. The effect is also observed in other chips for the same detector fabricated in one Multi Project Wafer (MPW) run. Since the detector cannot biassed above 80 V due to Halo effect, it restrict us to fully deplete the FZ-n detector. No such effect is observed in CZ-n and FZ-p detectors. The 2-D plot in figure 4.7 shows the pixel leakage current at 100 V detector bias voltage for the 1^{st} region of FZ-n detector. Each pixel leakage current was calculated by measuring the pixel DC level (pedestal) at different integration times (refer to section 4.4.2). It is found that the pixels with Halo effect have leakage current 20 times larger than the normal pixel. On the other hand beside Halo effect, a cluster of hot pixel at low voltages (i.e. below 10 V) are seen. The size of hot pixel cluster increases when the detector bias voltage reduces to 0 V, see figure 4.6 (right). This behaviour is also independent of the laser signal.

The Halo effect is also observed when the detector is illuminated with laser signal. A bunch of pixels around the hit pixel having 12 to 15 % of hit pixel count is seen in the

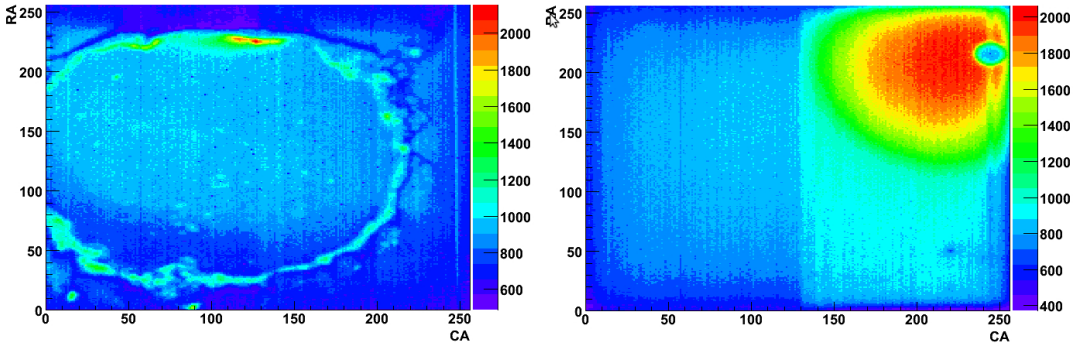

FIGURE 4.6: 2-D plot of DIPIX2 FZ-n detector represents ADC counts as a function of pixel matrix. Halo effect at high detector bias voltage (left: 100 V) and a cluster of hot pixels at low detector bias voltage (right: 0V).

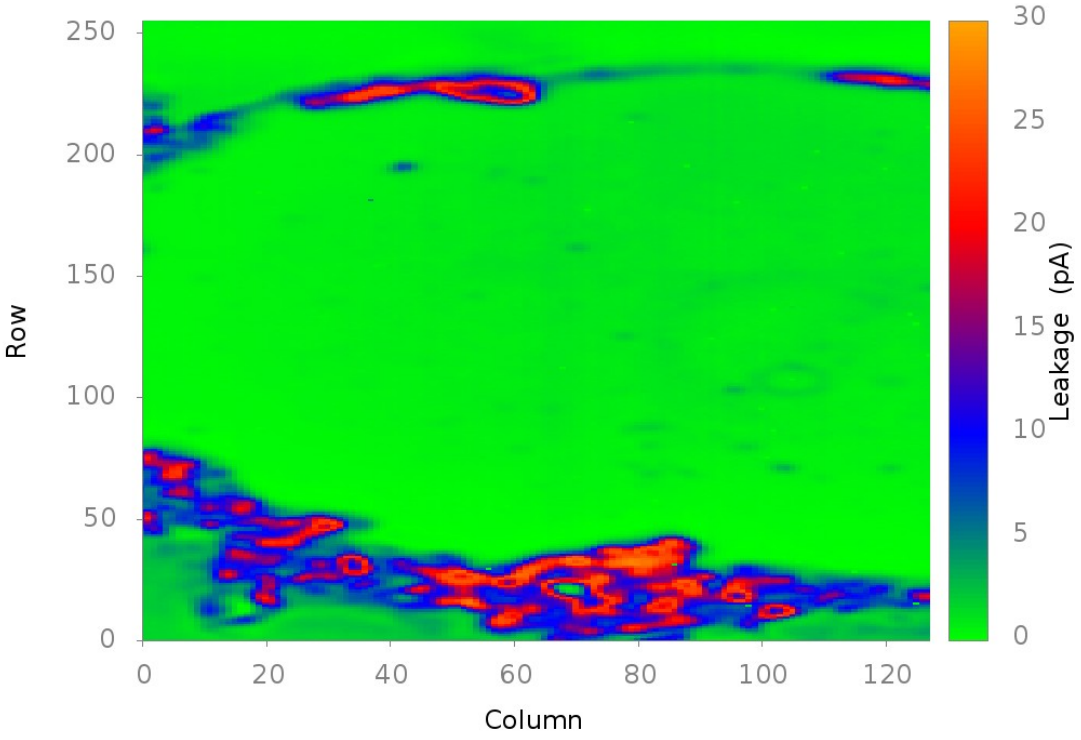

FIGURE 4.7: 2-D plot of 1^{st} region of FZ-n detector at 100 V detector bias voltage. Leakage current as a function of pixel position in matrix.

figure 4.8 (left). In order to reduce the Halo, the scans of detector back bias voltage, integration time, and laser intensity were performed. These scans resulted in reducing the Halo and its spot size. The Halo depends mostly on laser intensity, increasing for higher intensity. Figure 4.8 shows the laser signal in pixel matrix. The optimal setting for DIPIX2 FZ-n detector are 80 V detector back bias voltage and 100 μm of integration time. Figure 4.8 (right) shows the laser spot after optimisation.

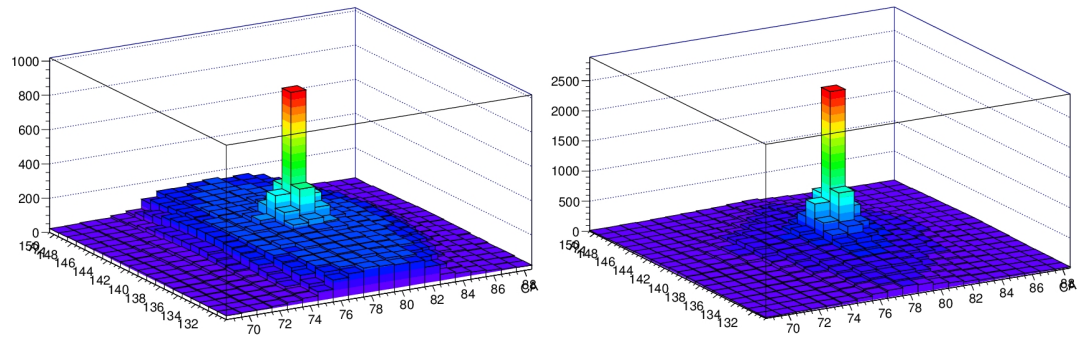

FIGURE 4.8: 2-D plot of DIPIX2 FZ-n detector before (left) and after (right) optimisation of the laser spot.

4.2.2 Periodic noisy peaks

Noisy peaks are found in the process of data readout after every 22 or 23 frames. This noisy peaks are related to timing of the readout. Since the readout buffer is not completely empty before the arrival of next event, this results in overlapping of events. The raw ADC values (average of all pixels) are plotted as a function of frame number for different integration times in figure 4.9. Figure 4.9 shows the presence of a noisy peak at every 22 or 23 frames. Regardless of change in integration time no change in peak position is observed. These peaks are found in both readouts, with CDS and without CDS. Since the position of these peaks are constant and periodic, it can be easily remove in the process of data cleaning.

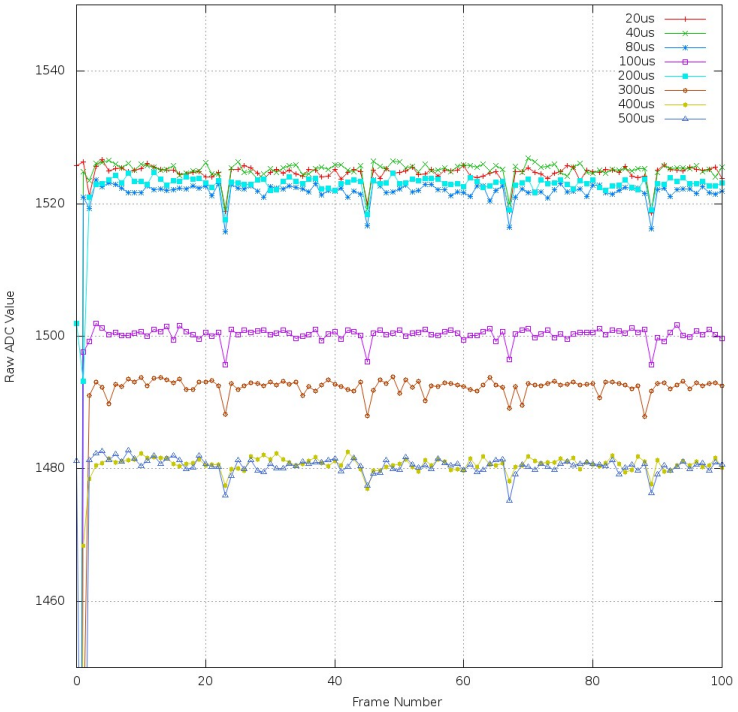

FIGURE 4.9: Periodic noisy peaks in CZ-n detector without CDS. The raw ADC values are a function of frame number for different integration times.

4.3 Detector performance using IR laser

The performance study of DIPIX2 detector is done using the 660 nm and 1060 nm laser wavelengths. The laser set-up as described in section 3.2.2 is used. The optimisation of laser intensity, integration time, and bias voltage is done to find the smallest spot size of the laser. The operation mode for the laser in this section is a pulsed mode with external trigger. After the laser set-up is prepared in pulsed mode, the optimised settings are applied and different characteristics of DIPIX CZ-n, FZ-n and FZ-p detectors are studied. The depletion study is also done on all three wafers and compared.

4.3.1 Pixel scan

The DIPIX2 CZ-n detector was scanned through 100 x 100 μm with a step of 2.5 μm in both X and Y axis of the detector. Since the pixel size is 14 μm, seven pixels are included in this scan. This scan helps in determining the accuracy of pixel size with respect to movable 3-D step motor. The laser was fixed, the detector was attached to 3-D step motor and the smallest laser spot was achieved, see figure 3.2. The weighted mean and weighted sigma of the cluster of hit pixels are calculated. The calculated weighted cluster mean represents the position of the laser on the detector. The top two plots in figure 4.10 show the results for 660 nm laser and the bottom two plots in figure 4.10 show the results for 1060 nm laser. In these plots the left figures show the results obtained from the scan performed in X-direction of 3-D step motor and the right figures represent the Y-direction scan. After fitting of the measured data, the slope is equal to the pixel size, i.e. 14 μm, see figure 4.10. This confirms that the accuracy of the pixel size is reliable.

4.3.2 Study of depletion voltage and signal with IR laser

The depletion region of the detector was studied using the picosecond pulsed IR diode laser (PDL 800-D) as radiation source, for the characteristics of the laser see table 3.2. The laser head was placed at a distance of 7 mm from the detector using 3-D XYZ stage to achieve the smallest spot size. The integration time of the front-end was set to 100 μs. The measured signal was expected to occupy mostly a single pixel, since the laser spot size is smaller than the size of a single pixel of DIPIX2, i.e. 14 x 14 μm^2. The 2-D profiles obtained from the detector biassed at 100 V (partially depleted), illuminating from the top side (junction side) of the detector with the 660 nm and 1060 nm lasers are shown in figure 4.11. The laser intensity was chosen to get realistic signal amplitudes corresponding to ionisation of a MIP, which gives about 850 ADC counts.

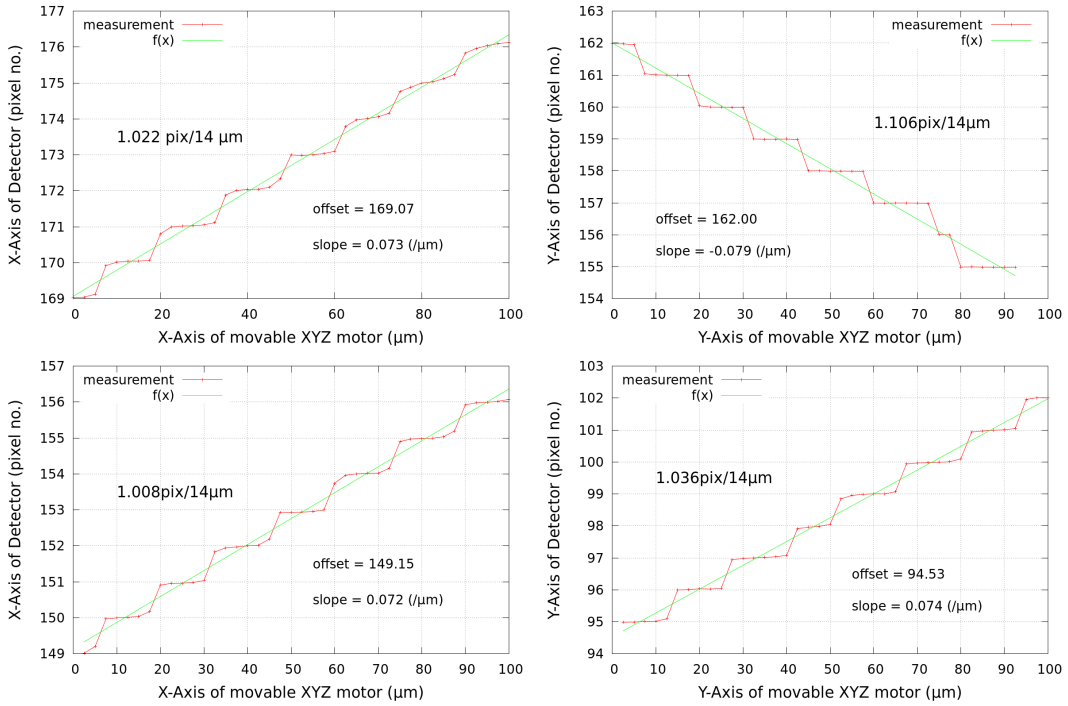

FIGURE 4.10: Pixel scan using 660 nm (top) and 1060 nm (bottom).

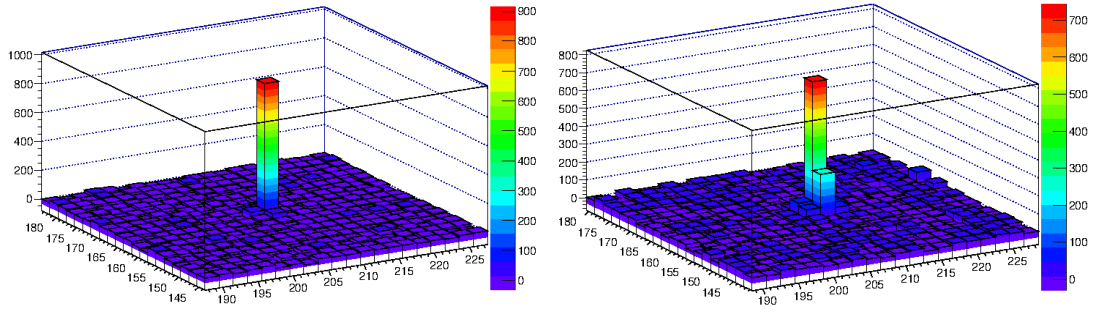

FIGURE 4.11: Examples of laser events of DIPIX2 CZ-n detector illuminated with 660 nm (left) and 1060 nm (right) laser wavelength.

To study the development of depletion layer the signal amplitude (sum of pixels amplitudes in a cluster) was measured as a function of detector bias voltage at different integration times. The 660 nm and 1060 nm lasers were used and their intensities, larger than in previous measurements, were kept approximately constant. Only one laser pulse was sent to the detector during a single integration time, since the laser was synchronised to the readout.

Three wafers with different thickness and resistivity (refer Table 4.1) were studied. For the 660 nm laser wavelength, having less than 10 μm range in silicon (according to [135] the penetration depth is 3.9 μm), a surface charge deposition is expected. Since the depth of the built-in depletion region is already above 10 μm, the signal should saturate at the lowest detector bias voltages. This is seen on figure 4.12 (left) looking at signal

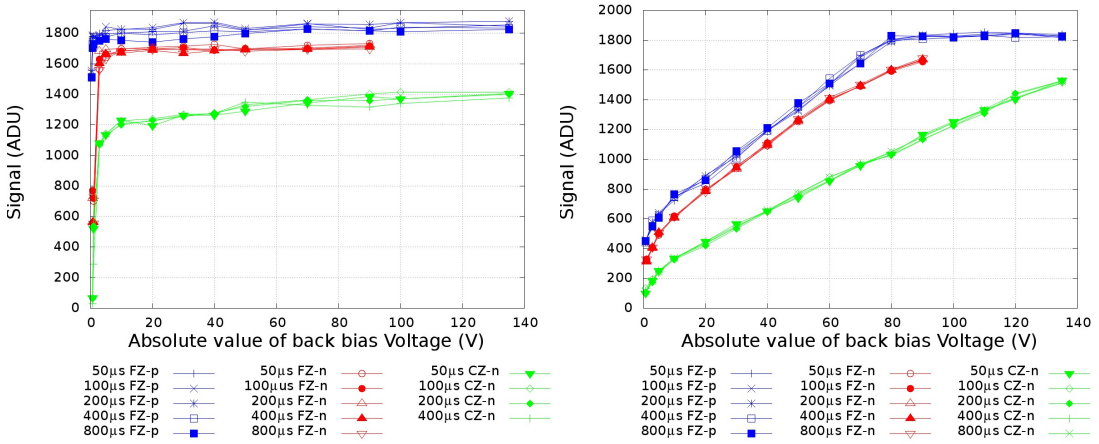

FIGURE 4.12: Signal amplitude as a function of detector bias voltage obtained at different integration times with 660 nm laser (left) and 1060 nm laser (right) for DIPIX2 CZ-n, FZ-n and FZ-p.

amplitude. On the contrary, for the 1060 nm laser, having the range in silicon higher than the detector thickness (penetration depth 890 μm [135]) one can expect the signal to increase until the full depletion is achieved. Indeed such increase is observed until the highest bias voltage applied for the CZ-n wafer, showing that the full depletion voltage for the CZ-n wafer is higher than the maximum applied bias. The measurements were done with the detector bias voltage limited to 130 V for caution because only two prototypes were available. This is in good agreement with the CZ-n detector specification since for 260 μm thick detector with resistivity about 700 Ω cm the depletion voltage should be about 240 V. According to the detector specifications, the full depletion voltage for detector with the FZ-n and the FZ-p wafers are calculated as 110 V and -80 V respectively. Figure 4.12 (right) shows that for the FZ-p wafer the signal saturates above -80 V detector bias voltage and this confirms that the full depletion is obtained. The detector with the FZ-n wafer is not biassed above 90 V due to the existence of large leakage current in the pixel matrix. For this reason the full signal saturation could not be achieved. Note that no change in signal amplitude for different integration times is seen because the laser is synchronised to the readout.

Figure 4.13 shows the measured (without laser) RMS of pixel noise at different integration times, which for the CZ-n wafer is continuously increasing, starting from the lowest detector bias. The pixel noise RMS is taken from the pedestal histogram. These histograms are produced for each detector bias voltage and the noise values are recorded. For the FZ-n and the FZ-p wafers much less noise increase is observed. An increase of noise with integration time shows that the effect of increasing leakage current (which increases pixel noise) dominates the effect of decreasing pixel capacitance (which tends to decrease pixel noise). It is seen well for the CZ-n for which the curves recorded at large integration times (higher current noise) have significantly higher noise. From the above

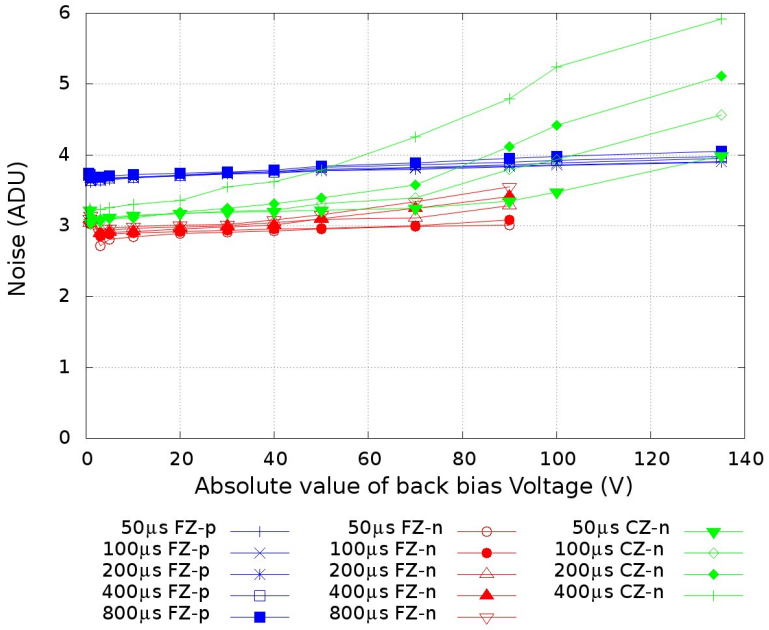

FIGURE 4.13: Noise as a function of detector bias voltage obtained at different integration times with DIPIX2 CZ-n, FZ-n and FZ-p.

data the SNR was calculated as a function of the detector bias voltage, for both laser sources. The results are shown in figure 4.14 for the 660 nm (left) and 1060 nm (right) laser wavelengths. For small detector bias voltages the SNR is growing rapidly because of increasing charge collection depth. For the 660 nm laser the SNR reaches maximum at very low bias voltage because of charge collection saturation. In case of the CZ-n wafer, after reaching saturation the SNR starts to decrease slowly because of continuous noise increase. For the 1060 nm laser and all wafer types the SNR grows up and then saturates. For the CZ-n wafer this saturation effect does not result from the full detector depletion but shows that the increase of signal amplitude is balanced by the noise increase. In the FZ-p wafer the saturation is achieved at -80 V when the full depletion is obtained and the SNR stays constant, since the increase in noise is very small for this detector. In the FZ-n wafer the presence of Halo and large leakage current restricts us from achieving the full depletion (refer to section 4.2.1). Because of malfunctioning of the FZ-n detector at higher detector bias it will not be included in the further studies.

4.4 Measurements using Am-241 source

Detectors with different wafer resistivity were measured using Am-241 source to calculate the energy resolution and the ENC of the detector. The pixel leakage current and noise performance was also studied as a function of detector bias voltage at constant temperature. The method for data cleaning and analysis is the same as described in

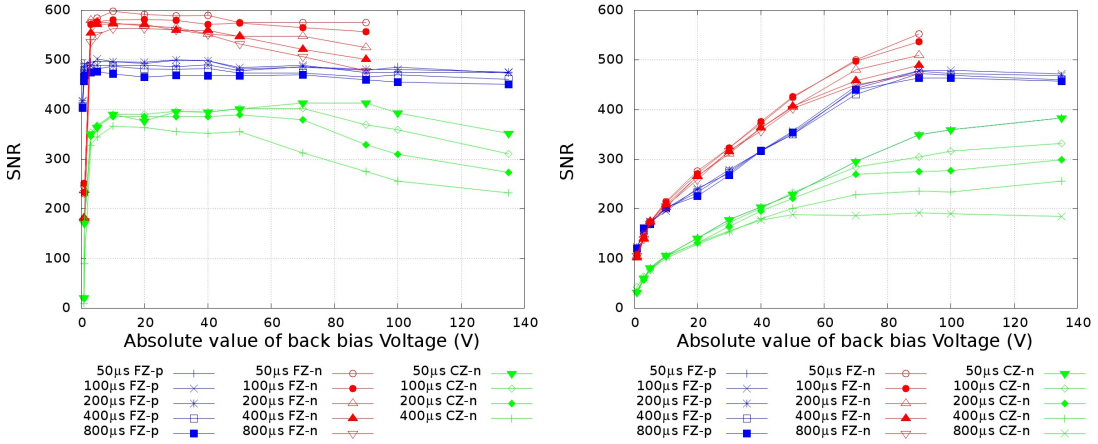

FIGURE 4.14: Signal to noise ratio as a function of detector bias voltage obtained at different integration times with 660 nm laser (left) and 1060 nm laser (right) for DIPIX2 CZ-n, FZ-n and FZ-p.

section 3.4.5. Depending on the type of measurement both offline and online analysis methods (see section 3.2.4) were used.

4.4.1 Measurements of ENC and Gain using DIPIX2 (CZ-n and FZ-p) detector

The Am-241 source is used to measure the noise and gain at three different temperatures. The temperatures used for these measurements are room temperature ($+20^oC$[1]), $+5^oC$, and -20^oC[2]. Since these detectors are susceptible to a small change in temperature, the monitoring of the total leakage current is also important. A drop voltage corresponding to the leakage current is measured across a resistor (200 kΩ) connected in series with detector bias terminal, since the total leakage current of the detector is of the order of nA. The temperature inside the fridge was measured by using a temperature sensor (PT100). Both the leakage current and temperature were monitored automatically using a lab-view program. Figure 4.15 shows an example of how the leakage current depends on small temperature changes of the fridge. Since a general purpose fridges were used for the measurement, the temperature of these fridges were not exactly as described, rather periodically varying by $\pm 2^oC$. To avoid the wrong ENC and gain calculation, the data taking with Am-241 source is initiated when the leakage current is stable. In figure 4.15 the measurements were done between 45 and 60 minutes.

When the measurement set-up is switched on the leakage current is not stable. The leakage current is monitored continuously until it stabilizes. Figure 4.16 shows the leakage current as a function of time for the CZ-n, FZ-n and FZ-p detectors. The back bias

[1]The room temperature is controlled using air conditioner
[2]Two fridges were used for $+5^oC$ and -20^oC

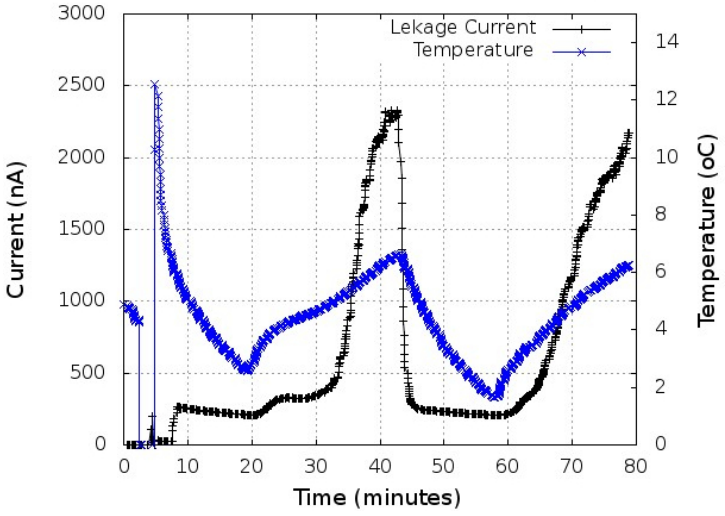

FIGURE 4.15: The FZ-p detector is used to study the dependence of leakage current on temperature with time.

voltage for the CZ-n, FZ-n and FZ-p detectors were 80 V, 80 V and -80 V respectively. From the figure it is seen that after 20 min the total leakage current is stabilized for the CZ-n and it is about 410 nA. In case of the FZ-p detector, it takes about one hour to stabilize the leakage current and it is about 2.7 μA. A large value of leakage is measured for the FZ-p compared to the CZ-n (low resistivity wafer). Since the FZ-p has resistivity 10 times larger than the CZ-n, a smaller value of leakage current is expected. This unexpected result can be explained by the presence of undesired current leaks at the chip edges and not in the pixels. On the other hand, the leakage current of the FZ-n detector is smaller compared to the CZ-n but it grows with time continuously and reaches values close to the CZ-n detector. The FZ-n detector will not be included in further studies, since the observed performance is worse, such as the Halo effect and continuous increase in leakage.

The DIPIX2 was irradiated using the Am-241 source to calculate the energy resolution and the ENC of the detector. For the set-up of this measurement refer to section 3.2.1. The detector was biassed at 80 V and placed at room temperature (20 ^{o}C). The study of noise and output gain with the Am-241 source is shown for the CZ-n and FZ-p detector. Figure 4.17 shows a single, a double, a triple and a quadruple pixel cluster histograms for the CZ-n detector and figure 4.18 shows the merged clusters histogram for the CZ-n detector. To obtain the spectrum of X-ray lines from Am-241 source the online method of analysis was utilised, refer to section 3.2.4. All monochromatic lines are well seen as peaks in the merged histogram. The low energy peaks corresponding to 8.01 keV, 13.9 keV, 17.7 keV, 20.7 keV and 26.3 keV are clearly seen in the single pixel cluster distribution and higher energy peak at 59.5 keV is seen in larger pixel clusters. The cluster histogram and merged clusters histogram of the Am-241 source obtained for the

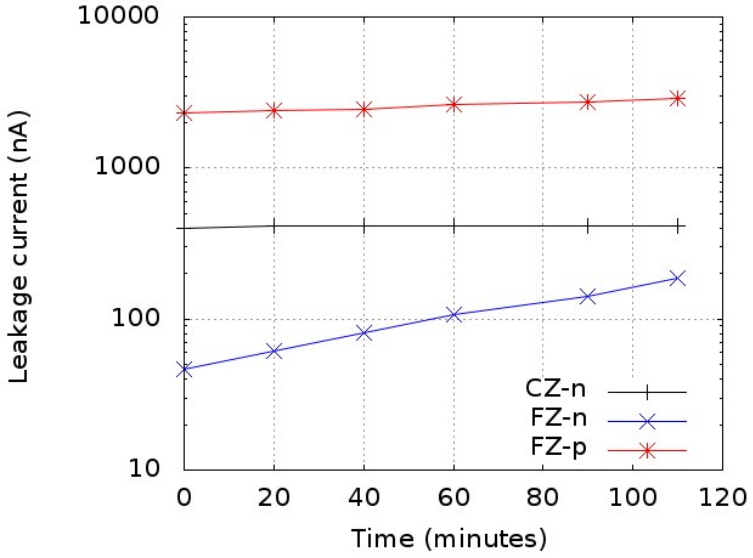

FIGURE 4.16: Leakage current at room temperature as a function of time.

FZ-p detector are shown in figure 4.19 and 4.20 respectively. The ENC is $\simeq$ 110 e^- for the CZ-n and $\simeq$ 93 e^- for the FZ-p detector, calculated from the 59.5 keV peak position.

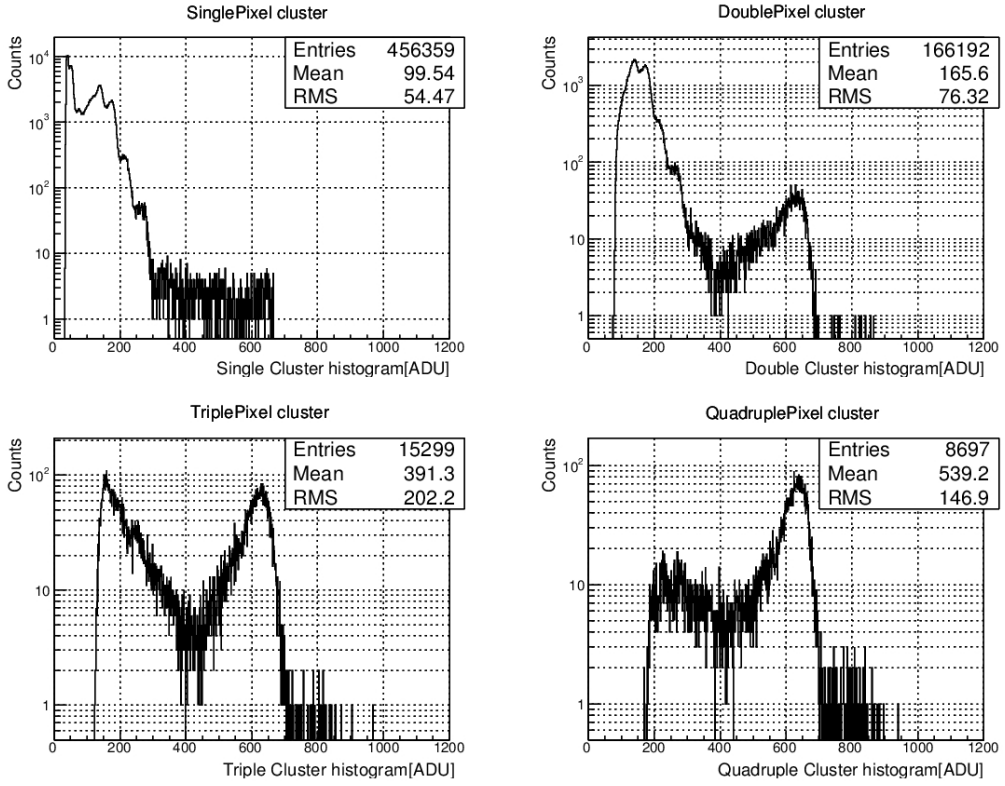

FIGURE 4.17: Distributions of amplitudes generated in DIPIX2 CZ-n by Am-241 X-ray source for different cluster size.

Figure 4.21 left and right show the linear fit of energies measured from the Am-241 source for the CZ-n and FZ-p detector respectively. The gain of the whole readout for the CZ-n

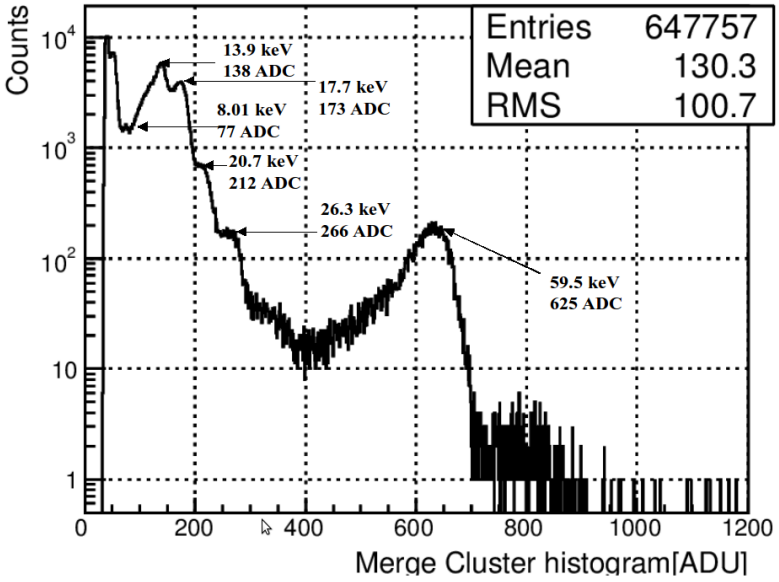

FIGURE 4.18: Energy spectra of X-ray (Am-241) obtained after merging all clusters from DIPIX2 CZ-n.

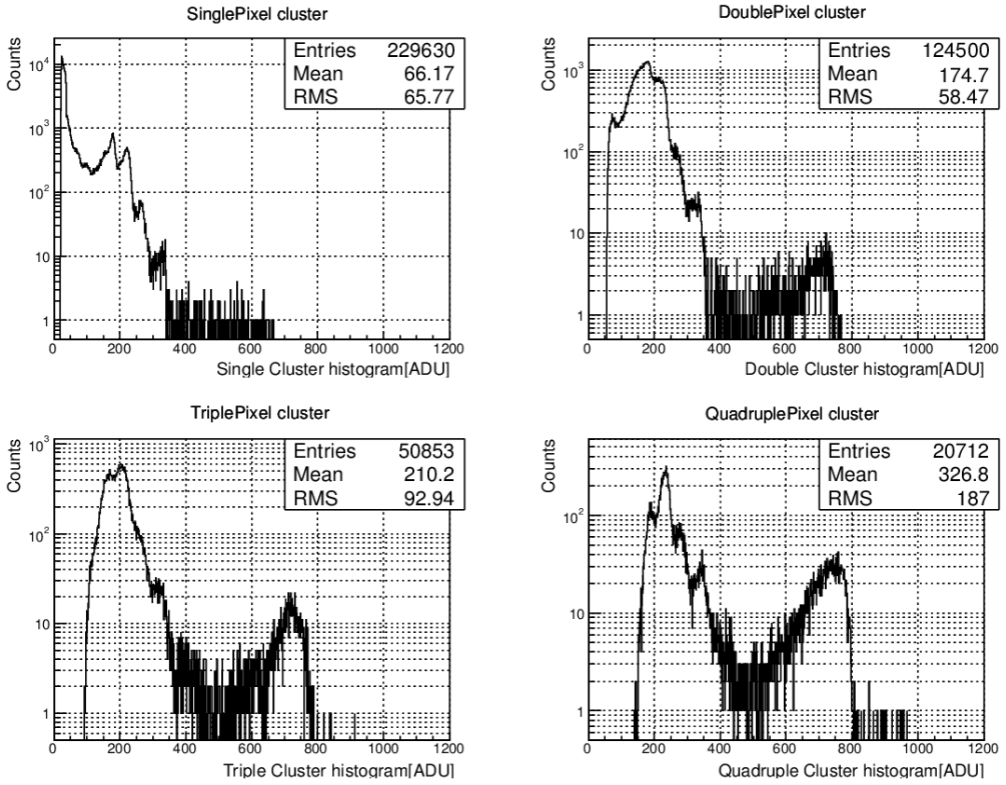

FIGURE 4.19: Distributions of amplitudes generated in DIPIX2 FZ-p by Am-241 X-ray source for different cluster size.

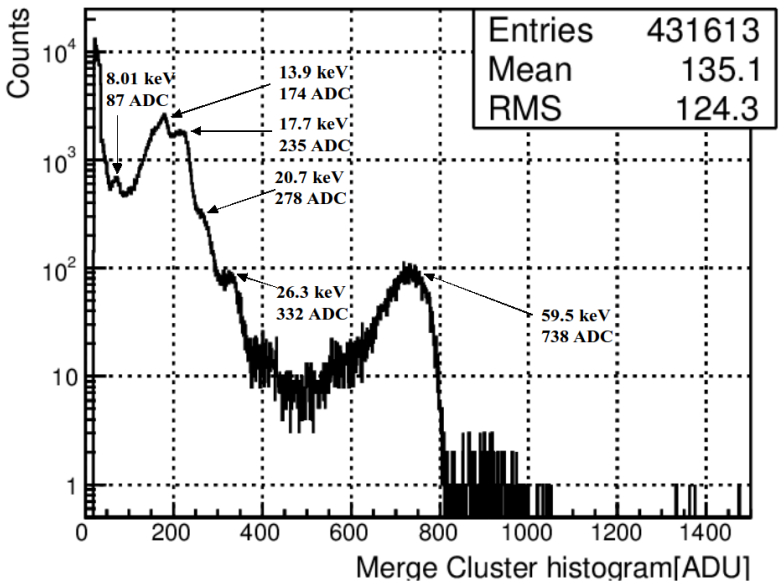

FIGURE 4.20: Energy spectra of X-ray (Am-241) obtained after merging all clusters from DIPIX2 FZ-p.

detector is 9.2 $\mu V/e^-$ and for the FZ-p 10.9 $\mu V/e^-$, calculated from the best fit between the Am-241 energies and the measured ADC count.

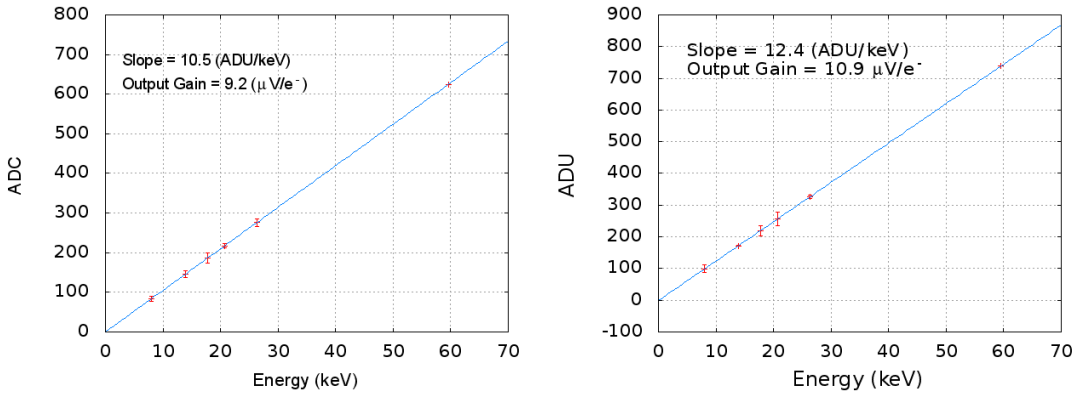

FIGURE 4.21: ADC count as a function of the energy spectrum from Am-241 for CZ-n (left) and FZ-p (right).

The DIPIX2 CZ-n and FZ-p leakage current and noise performance were also studied as a function of detector bias voltage at different temperatures, as shown in figure 4.22 and 4.23. For this study the measurements were done at ambient temperature and at two lower temperatures for DIPIX2 placed in the fridge. The DIPIX2 leakage current was measured continuously. The exact chip temperature was not known and the temperatures seen on the legends of figure 4.22 and 4.23 show only external temperature settings, which could differ from the chip temperature. For this reason these measurement are meant to show only qualitative behaviour. The total leakage current was measured at the high voltage terminal. Figure 4.22 (left) shows an expected very large change of

leakage current of the DIPIX2 CZ-n between the measurements performed at different temperatures. For each temperature a steady grow of leakage current with detector bias voltage is also observed. The ENC, shown in figure 4.22 (right), grows with temperature, as one could qualitatively expect. But the increase of ENC vs temperature is very small, meaning that the main source of noise is not the leakage current noise as one could expect but it comes from other sources (refer to section 4.4.2). Figure 4.23 show the leakage current and ENC as a function of detector bias for the DIPIX2 FZ-p. As discussed earlier in this section the leakage current is not consistent with the wafer resistivities. The observed leakage current in FZ-p detector is possibly due to undesired current leaks at the chip edges. On the other hand, as expected, the ENC is slightly smaller than in case of the CZ-n wafer.

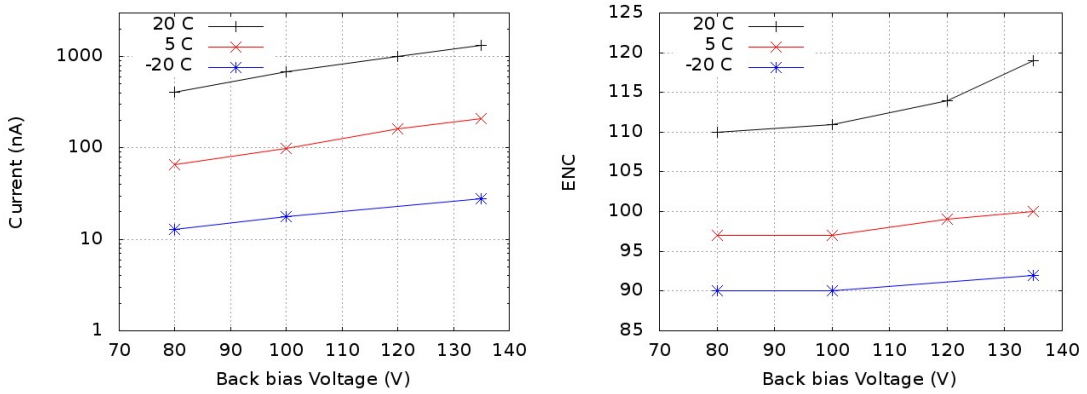

FIGURE 4.22: The CZ-n detector is measured to plot the leakage current (left) and ENC (right) as a function of detector bias voltage at three different temperatures.

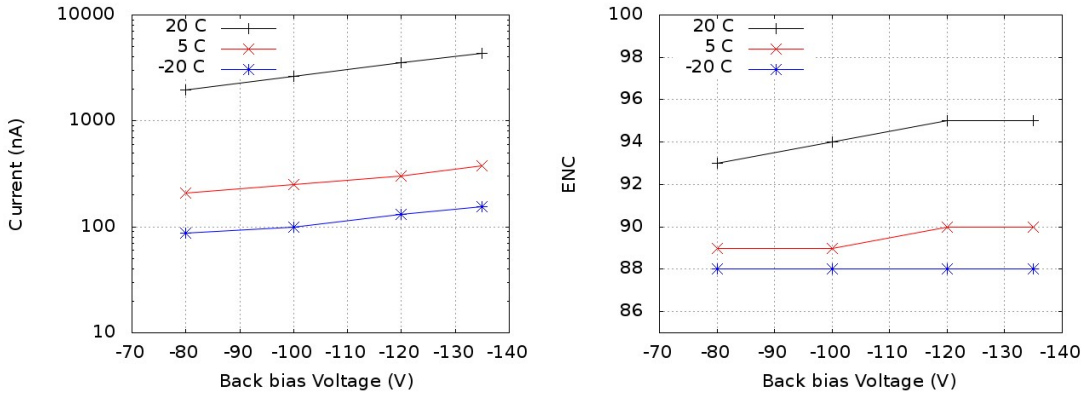

FIGURE 4.23: The FZ-p detector is measured to plot the leakage current (left) and ENC (right) as a function of detector bias voltage at three different temperatures.

4.4.2 Study of pixel current and noise

Measurements of the pixel DC level (pedestal) at different integration times can be used to obtain the value of pixel current. The pixel current, except of pure leakage

TABLE 4.4: Parameters of the DIPIX2 chips.

Wafer	Resistivity (kΩ cm)	Thickness (μm)	Capacitance (fF/pix)	Pixel Leak (pA/pixel)	Total Leak (μA)
CZ-n	0.7	250	16.5	4.95	0.38
FZ-p	7	500	13.8	2.21	2.7

current of p-n junction, may contain also other components, like the SOI transistor body charging/discharging currents, the gate tunnelling current, currents resulting from surface effects etc. This total pixel current can be found as the slope of the measured pedestals versus integration time (assuming linear dependency), multiplied by the pixel capacitance [84]. The latter is known from the Am-241 59.5 keV peak position, see figure 4.18 and 4.20. Note, that since the voltage gain of the whole readout chain, including the DIPIX2 and the external ADC board (SEABAS [73]) is very close to one and the values of the pedestals are known. Figure 4.24 shows the mean pedestals of all pixels at different integration times for the CZ-n and FZ-p detectors and were biassed at 100 V and -100 V, respectively. Table 4.4 shows the parameters of the two wafers, including resistivity, thickness, pixel capacitance, the calculated average pixel current, and the total detector current.

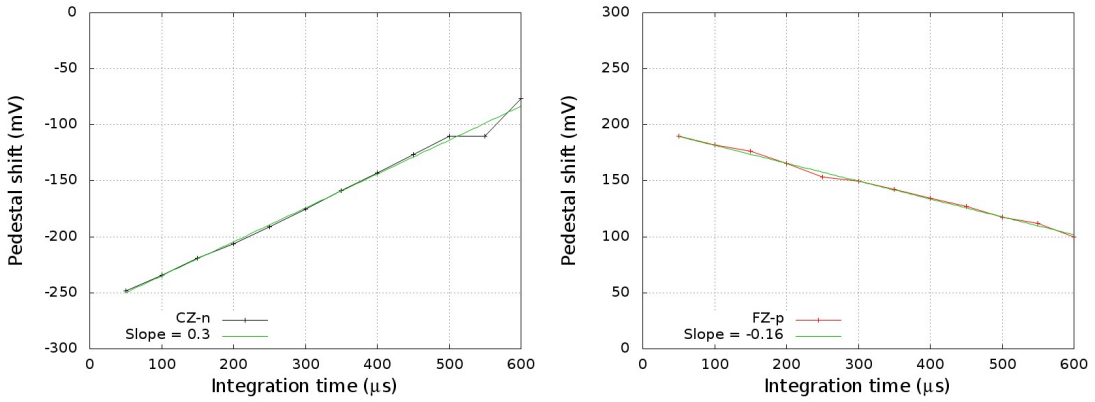

FIGURE 4.24: To calculate the pixel current, mean pedestal shift is plotted as a function of integration time, CZ-n (left) and FZ-p (right).

Plots shown in figure 4.25 present the pixel currents as a function of position in matrix of 128 x 256 pixels (top); and 3-D plot of a small fraction of the same matrix (bottom). The pixel current was calculated from the pedestal data collected in 400 frames, separately for each pixel. The pixel current can be also estimated assuming a linear dependency of the squared ENC on integration time; the relevant slope, resulting from the shot noise, linearly depends on the current and the voltage-to-charge gain, known already from the Am-241 measurements. Such study was performed for FZ-p detector. To assure a good linearity in the ENC measurements, it was necessary to perform a two dimensional scan of the pixel reset (RST) and CDS reset (RST CDS) voltages with

respect to integration times (see figure 4.26). For each measurement the peak difference is calculated by determining the position of 59.5 keV peak for each integration time and the difference of the peak position at higher integration time to the lower integration time. The region where the minimum peak difference is measured will be used as the optimal value for pixel current study, see figure 4.26. The optimal value of RST of 800 mV and RST CDS of 450 mV were used in all following measurements.

Figure 4.27 (left) shows the pixel current versus sensor bias voltage obtained for both the pedestal shift and the ENC methods. The curves saturate above the -80 V bias voltage because the full depletion is achieved (see also figure 4.12). A flatness of the ENC curves versus detector bias voltage visible in figure 4.28 confirms good quality of the FZ-p detector. A weak dependency of the pixel capacitance on detector bias is presented in figure 4.27 (right).

The DIPIX2 FZ-p noise measurements at different integration times made possible to estimate the pixels currents of around 2 pA, which means that the relevant parallel noise components of the ENC at the typical integration time of 100 μs can be around 40 e^- only. Thus a question arises about remaining noise components, included in the obtained values of the total ENC above 110 e^-, see figure 4.28.

Two special versions of the SEABAS board firmware were used to investigate the electronic noise of the system. First, the output noise with the CDS switch S3 permanently closed (figure 4.2), was found to be around 1.0 adc units ($\simeq$ 25 e^-) and almost independent on the integration times. It includes all noises originating in the DIPIX2 readout chain, i.e. the chip column and output amplifiers followed by the SEABAS electronics. Another measurements, with the RESET switch permanently closed (transistor M1, see figure 4.2) were performed in order to estimate a total electronic noise, including the pixel Source Follower (transistor M3). This total electronic noise has monotonously varied from 3.5 to 4.0 adc units (75 to 86 e-) for integration times from 320 ns to 600 μs, respectively. From the latter result, taking into account the kTC noise of the CDS and formerly measured electronic noise of the readout chain, one can deduce that the pixel Source Follower noise, processed by the CDS, dominates, adding between 65 to 80 e^- to ENC. Here it should be noted that the CDS increases white noise by the factor of "$\sqrt{2}$".

Thus the relatively large noise originating in Source Follower can be explained by the high level of the flicker noise produced in input transistor; its small dimensions (W=630 nm, L = 200 nm) are not optimal in terms of the flicker noise minimization. Flicker noise presence is clearly indicated by the observed noise versus integration time dependency.

Still, the mentioned above, estimated noise components (40 e^- - parallel noise, and 75-86 e^- - Source Follower, CDS, and readout) don't sum up to the observed noise level (figure

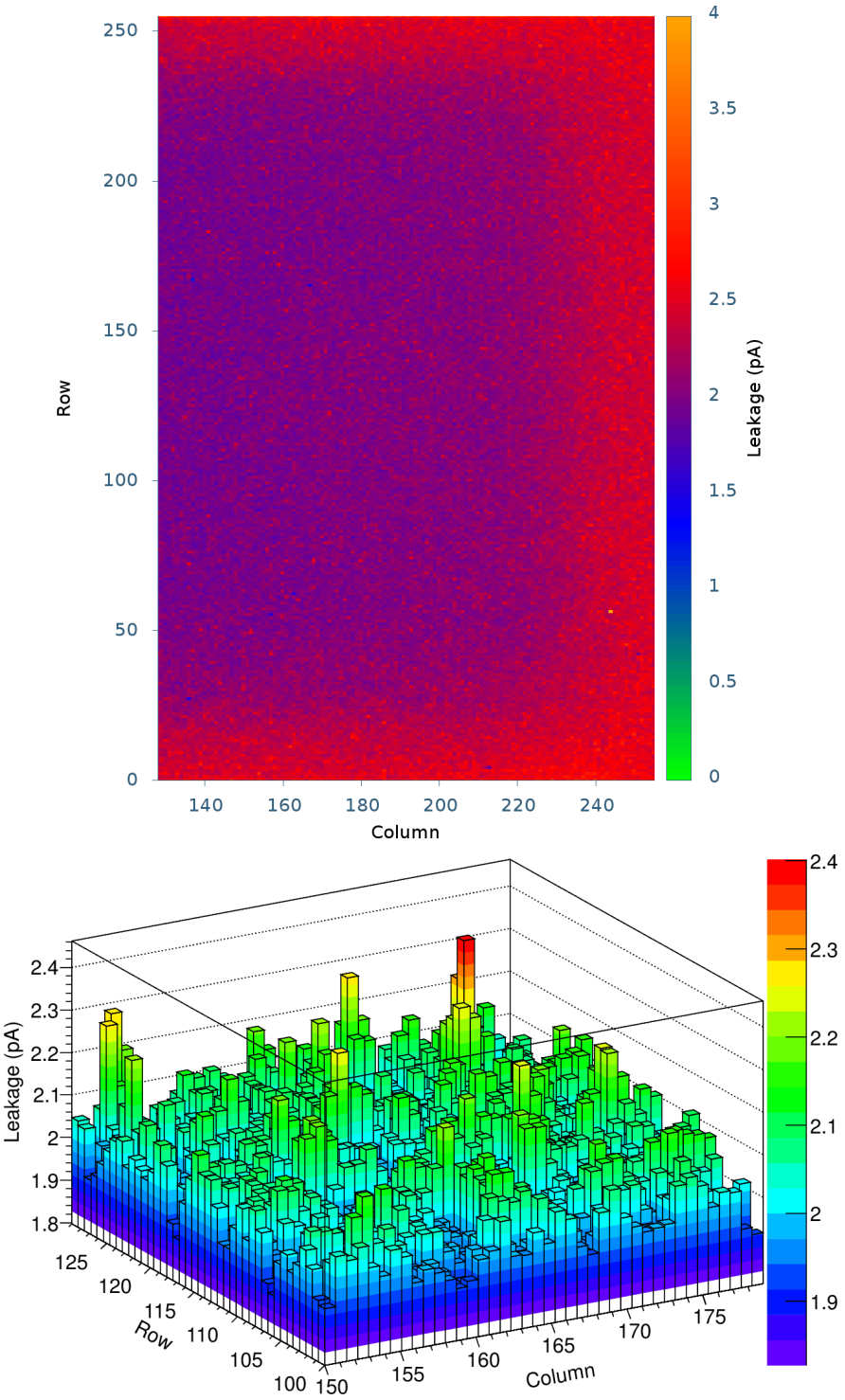

FIGURE 4.25: The pixel currents of the DIPIX2 FZ-p biassed to -80 V as a function of the pixel position. Top picture shows currents of 128 x 256 pixel area (half of the sensor) and the bottom one is a zoomed 3D graph of the 30 x 30 pixels area.

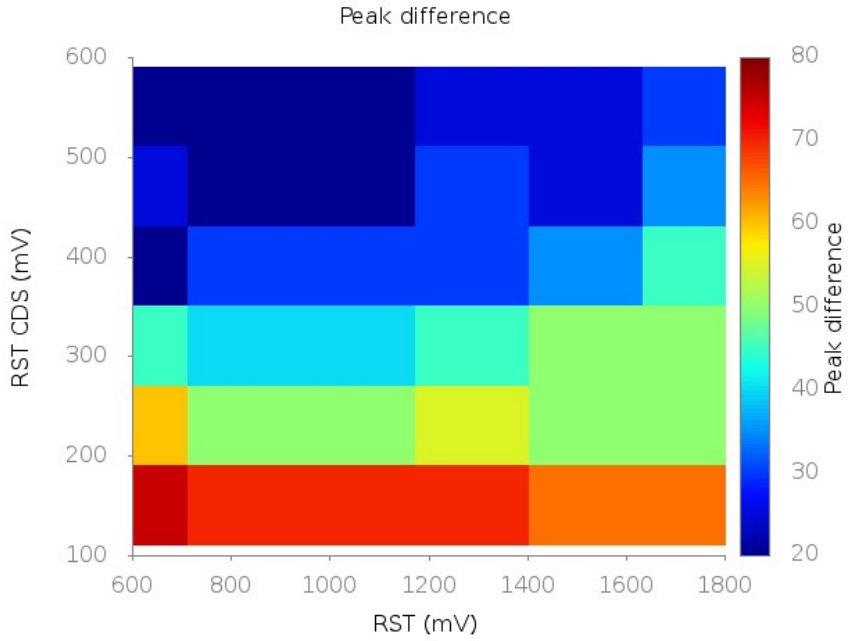

FIGURE 4.26: 2D plot, the peak difference as a function of RST and RST_CDS.

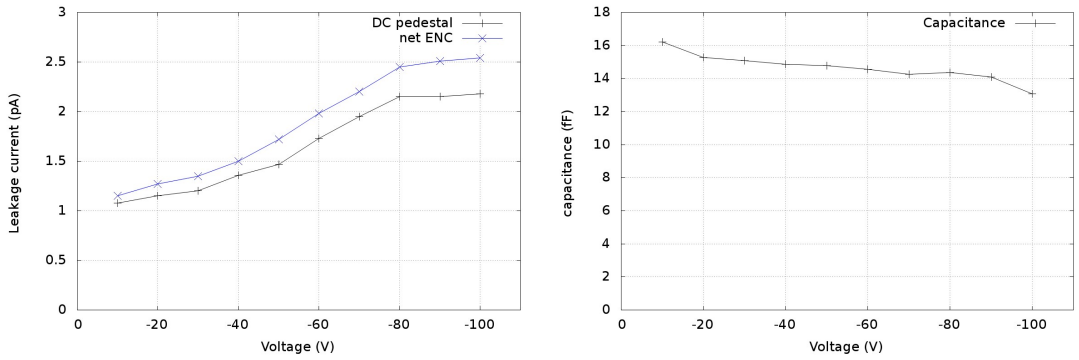

FIGURE 4.27: The FZ-p pixel current (left) and the pixel capacitance vs detector bias voltage.

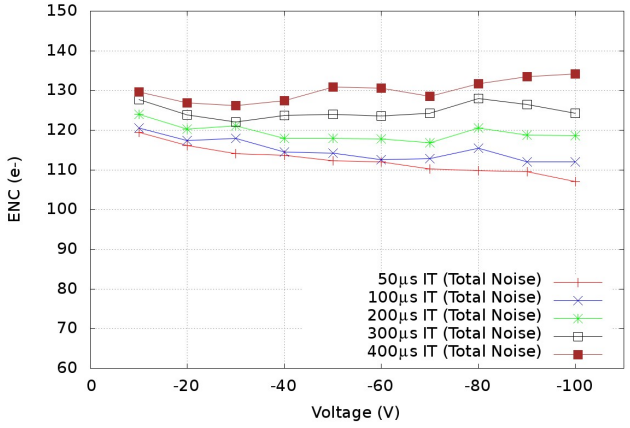

FIGURE 4.28: The ENC noise as a function of the sensor bias voltage for FZ-p detector.

4.28). These missing parts must be attributed to the readout operation (for example digital cross-talks, noisy DC biases) and also to the thermal and unknown effects in the sensor.

Summary and Conclusions

The progress in the development and improvements of SOI technology has attracted various international institutions [136]. The interest in SOI technology has grown outside the HEP applications and it attracts researchers from astronomy, medicine and photon science. The maturity level achieved by this technology will be beneficial for the design of future radiation detectors.

The main objective of this dissertation was the characterisation and studies of the detector performance of different pixel prototype circuits designed and developed at KEK Tsukuba, Japan. The author performed the measurements and data analysis of INTPIX3 and DIPIX2 detectors. As discussed earlier, both detectors are integration type pixel detectors. All INTPIX3 detectors were designed using CZ-n type wafer with resistivity of 0.7 kΩ cm, whereas DIPIX2 detectors were designed using three different wafers for which the resistivity varies from 0.7 kΩ cm to 7 kΩ cm.

The effect of large detector bias voltage on transistors was reproduced using ENEXSS simulation software [137] and the transistor characteristics from ENEXSS were compared with cadence and found to be similar (chapter 2.4). The test set-up and procedure for detector measurements were prepared for the measurements with the laser and radiation source (chapter 3.2). Two INTPIX3 detectors, INTPIX3a and INTPIX3b, each with 8 different regions, were characterised. The solution to the back gate effect was introduced in INTPIX3a by implanting an extra BPW layer just below the oxide layer. The characteristic of the TEG transistor and the stability measurement of raw pixel output with detector bias voltage confirm that the back gate effect is mitigated (chapter 3.3 and 3.4.3). The solution to the back gate effect results in an increase of pixel capacitance and reduces the gain of the detector. This effect can be reduced by optimising the area of BPW in the pixel.

All 16 regions of INTPIX were measured with a radiation source (Am-241) to find the optimal area of BPW layer. The measurement results confirm that the region with a smaller area of BPW perfectly mitigates the back gate effect and also has higher gain and better ENC (see table 3.8) [138]. The ENC of the 8^{th} region of INTPIX3a and INTPIX3b

is about 186 e^- and 168 e^- respectively. The gain of the 8^{th} region of INTPIX3b is 20.9 $\mu V/e^-$ which is higher than the gain of the 8^{th} region of INTPIX3a (6.6 $\mu V/e^-$). From these results it is confirmed that the 8^{th} region of INTPIX3b provided with smaller BPW area results in better gain and ENC.

The laser with a wavelength of 660 nm was used for the SOI detector study and its spot size was optimised by varying the distance between the laser and the detector. The measured spot size was about 8 μm, and since the pixel size of INTPIX3 is 20 μm, most of the charge deposited by the laser is seen in a single pixel. Several pixels of the INTPIX3a detector were scanned by moving the laser in the X and Y directions. The measured position of the laser on the detector was linear with the real position on the 3-D step motor (chapter 3.4.4). The stability test of the detector indicates that these detectors cannot be used for long time measurements because of increasing pixel ADC count with time (chapter 3.4.2). One of the possible reason for this effect is due to an increase in detector temperature. The position of the sub-board (consisting of an INTPIX3 socket) is exactly above the main readout board, see left figure 4.29. This arrangement possibly increases the detector temperature and results in increasing pixel ADC count.

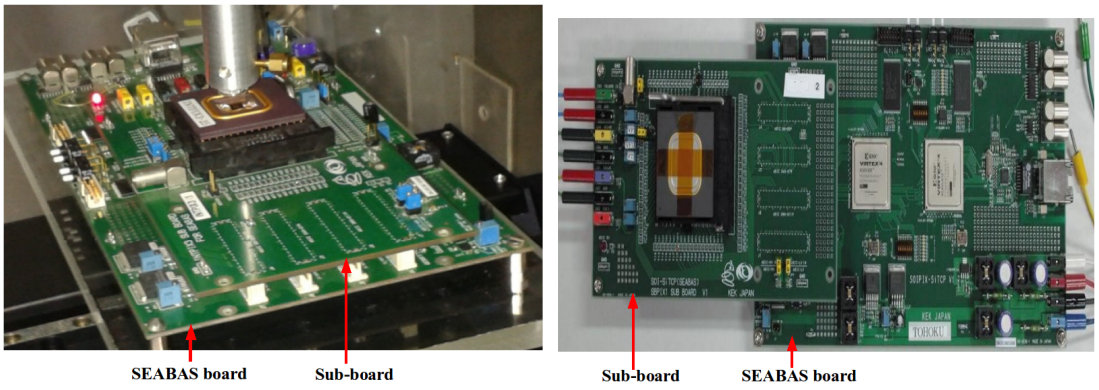

FIGURE 4.29: INTPIX3 (left) and DIPIX2 (right) seabas and sub-board.

Three detectors of the DIPIX2 family (CZ-n, FZ-n and FZ-p) were studied. The long time stability problem was successfully mitigated in DIPIX2, maybe by changing the position of the sub-board on the main readout board (see right figure 4.29). The pixels were scanned through 100 x 100 μm using both 660 nm and 1060 nm lasers. The obtained results confirm that the measured position is linear with the known position of the laser and the slope is in agreement with the pixel size, indicating the accuracy of the detector [139]. Both lasers were used to study the full depletion voltage. The measurement with the 660 nm laser shows saturation at low detector bias voltage for all three wafer resistivities, indicating the penetration depth of the 660 nm laser of about a few μm. On the other hand for the 1060 nm laser, a continuous increase in the laser signal is observed until a full depletion is obtained. The measured results confirmed the calculated full depletion voltage of the FZ-p detector of about -80 V (chapter 4.3.2) [140],

allowing for a reduction of detector thickness, which is of concern for particle physics experiments.

The performance of DIPIX2 detectors was also verified using an Am-241 radiation source. The ENC of the CZ-n and FZ-p detector is measured to be about 110 e^- and 93 e^- respectively at ambient temperature (20 ^{o}C). Due to halo effect and worse ENC in the FZ-n detector, it was not used to study the pixel current and ENC at lower temperatures. The measured ENC of the FZ-p detector at lower temperature (-20 ^{o}C) is reduced to 88 e^-. The detector leakage current was also measured at both temperatures (20 ^{o}C and -20 ^{o}C), showing a decrease by two orders of magnitude, as expected. However, the high drop of leakage currents did not result in a similar decrease of the noise ENC. To understand the inconsistency of ENC with the leakage current, the pixel current and noise were measured (chapter 4.4) [140]. In a first attempt it was verified that the pixel current obtained from the measurements of DC potential, for different integration time, is in good agreement with the one calculated from the measured ENC of noise. The leakage current for each pixel in the sensor is measured and the flatness of the ENC versus detector bias voltage (chapter 4.4.2) confirms a good quality of the FZ-p detector.

The developed SOI pixel prototypes were investigated for the application in particle physics. The key technological improvements such as the use of high resistivity FZ-n wafers and thinning the devices to 50 μm have been successfully realised [139]. The radiation tolerance for SOI pixel detectors should be the main future improvement. Due to the non-availability of infrastructure the radiation tests were not performed in this work, which could be a future activity. However the radiation tolerance study on INTPIX3 was done by the KEK group in Japan and the results are promising at 10 kGy of radiation [14]. Thanks to the D-SOI technique up to 100 kGy tolerable radiation level can be achieved [83].

Symbols

a	distance
P	power
σ	Standard deviation
p_T	Transverse momentum
B	Magnetic field
L	Distance between planes
s	sagitta
R	Curvature radius
Λ	Baryons
D, B	Mesons
σ_{d0}	Impact parameter resolution
$r1$, $r2$	radii of the layers
σ_1, σ_2	Intrinsic measurement error
p	Momentum
x/X_0	Radiation length
$c\tau$	Mean decay length
i	Instantaneous induced current
q	Charge
$\vec{v}$	velocity
$\vec{E_Q}$	Electric field
V	Voltage
C	Capacitance
E_g	Band gap energy
E_c	Conduction band energy
E_v	Valence band energy
$n(E)$	Distribution of electrons in conduction band
$p(E)$	Distribution of holes in valence band
$g_c(E)$	Density of quantum states in conduction band
$g_v(E)$	Density of quantum states in valence band

$f_F(E)$	Fermi-dirac probability function
n	Electron concentration
p	Hole concentration
n_0	Electron concentration in thermal equilibrium
p_0	Hole concentration in thermal equilibrium
N_c	Effective density in the conduction band (for silicon 2.8 x $10^{19} cm^{-3}$)
N_v	Effective density in the valence band (for silicon 1.04 x $10^{19} cm^{-3}$)
k_B	Boltzmann constant
T	Absolute temperature
n_i	Intrinsic carrier concentration (for silicon n_i is the order of $10^{10} cm^{-3}$)
ρ	Density
τ	Mean free time
υ_d	Drift velocity
J_{ndrf}	Electron drift current density
J_{pdrf}	Hole drift current density
μ_n	Electron mobility
μ_p	Hole mobility
D_n, D_p	Diffusion constants
$\frac{dn}{dx}$	Gradient of electron carrier concentration
$\frac{dp}{dx}$	Gradient of hole carrier concentration
J_n	Total electron current density
J_p	Total hole current density
ψ	Electrostatic potential
ε	Isotropic dielectric permittivity
N_D	doping concentration of donors
N_A	doping concentration of acceptors
U_n, U_p	Net recombination rates
U_{SRH}, U_{Auger}	Shockley-Read-Hall and Auger recombination
n_{ieff}	Effective intrinsic concentration
τ_n, τ_p	Lifetime of electron and hole
n_{1ieff}, p_{1ieff}	Densities close to effective intrinsics level
c_n, c_p	Specified constant depends on the material
$\mu_{can}(E)$	Mobility of Canali model
υ_{sat}	Saturation velocity
β	Relative particle speed
$N(x)$	Doping distribution
N_{peak}	Doping concentration at the peak
x_{peak}	Position of peak at location x
N_{ref}	Referential concentration

x_{ref}	Referential position at location x
W	Width
L	Length
V_d	Drain voltage
V_g	Gate voltage
I_d	Drain current
V_{gs}	Gate to source voltage

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