AKADEMIA GÓRNICZO-HUTNICZA IM. STANISŁAWA STASZICA W KRAKOWIE

WYDZIAŁ FIZYKI I INFORMATYKI STOSOWANEJ

Projekt dyplomowy

Qualification tests of FLAXE - a dedicated front-end ASIC for the readout of semiconductor detectors

Testy kwalifikacyjne dedykowanego układu scalonego FLAXE, do odczytu sygnałów z detektorów półprzewodnikowych

Autor: *Maciej Uliasz*
Kierunek studiów: *Fizyka Techniczna*
Opiekun pracy: *prof. dr hab. inż. Marek Idzik*

Kraków, 2025

I would like to express thanks to my family and friends for supporting me throughout the studies, and to my supervisor for actively overseeing my progress on this thesis.

Contents

Introduction

The FLAXE application specific integrated circuit (ASIC) is a chip designed for handling the readout of the calorimeter in the LUXE experiment at DESY in Hamburg. The objective of the experiment is to study interactions of 16.5 GeV electrons with a 40 TW laser. Such conditions result in the strong-field interaction vaccumm becoming polarized, and in positron-electron pairs being produced. By observing the rates of this production in the function of laser intensity, LUXE aims to better explore the QED theory and it's processes, especially weak coupling in non-linear Compton scattering.

The goal of this thesis was to perform qualification tests on the first batch of 142 FLAXE chips. This is vital for singling out faulty chips, estimating the yield of the production, and grading the chips. The chips with a higher grade are to be used in the more important, pivotal points of the used detector. After the initial tests, data about certain qualities of the chips is to be aggregated, in order to get a better idea of any possible errors in design or during production.

Chapter 1 of this dissertation mentions the basic principles of semiconductor detectors, and basic circuit elements utilized in readout electronics. The next chapter describes the FLAXE ASIC: it's construction and parameters. Chapter 3 includes the bulk of the analysis and results from the qualification testing.

1. Principles of readout electronics

1.1. Semiconductor detectors

Readout electronics go hand in hand with the detectors they get their signal from. A particularly popular type of detector in the field of particle detection is the semiconductor detector. The most often used material for their construction is silicon, simply because of it's abundance in the Earth's crust. The basis for the intrinsic inner workings of that type of detector are the energy bands of semiconductor materials. A passing photon lifts electrons from the valence band to the conduction band, which leaves behind holes in the valence band. Electrons and holes are both free charge carriers, and they can be registered on electrodes, provided that voltage is applied. The main advantages of using a silicon detector are:

- The density of a silicon detector is much greater than that of a gaseous detector. This, on the basis of the Bloch formula, makes it so that far less volume is needed to deposit the same amount of energy from a particle.
- In addition to absorbing energy of particles more effectively, the energy necessary to create an electron-hole pair is a few times smaller than the energy required to create an electron-ion par, which results in a higher output signal.
- Superior spatial resolution.
- Small leakage currents.
- Fast signal

The active part of the detector is realized by a junction of p and n doped regions. There exist two variations on this construction: the PIN and PN type detectors. PIN detectors have three layers; two outer most ones are heavily doped with acceptors and donors each, meanwhile the middle layer is an intrinsic one, with the same concentration of both holes and electrons. This inner layer is the actual part of the detection system, in which radiation is absorbed. Such a construction produces a uniform electric field within the intrinsic layer.

PN type detectors have only two layers, and in contrast to the PIN type, they are highly antisymmetric in geometry. Usually the p layer is thin, and merely acts as a a window for the radiation, meanwhile the

n layers is the active part. Such an arrangement of layers makes it so that the electric field intensity decreases linearly within the electron doped region [1].

1.2. Charge amplifiers

As with most electronic equipment, an amplifier is necessary to provide us with a stable and high enough signal, and this is no different in particle detectors. This is doubly true for semiconductor detectors, since they, unlike gaseous detectors, have no natural ways of amplifying their signal. The native signal from a semiconductor detector usually is in the range of nanoamperes [2]. That is why, before any signal processing or digitisation gets done, an amplifier is placed as the second element in the signal chain, right after the detector itself. Because of this, it's often called the preamplifier. The construction of an amplifier itself is realized by transistors. Many different designs are possible, ranging from simple inverters, to amplifiers with multiple cascode stages.

Preamplifiers work on the principle of operational amplifiers, that is, their characteristic depends on other components present in the circuit that makes up the amplifier. Usually these components are present in the feedback loop and they consist of impedances and capacitances; capacitance in order to put up voltage at the output of the amplifier proportional to the amount integrated charge. The impedance is used for discharging the capacitor, since with more and more charges flowing into it, the output of the amplifier will eventually saturate.

1.3. Signal shaping

The third part of the signal chain is the signal shaper. Initially, our signal comes out of the detector as semi dirac deltas of current, and the preamplifier transforms them into step functions of voltage piled up on each other. This is an undesirable effect, because it disallows us from completely separating individual signals from each other, and it makes the analysis of the information difficult. To prevent the oncoming impulses from the detector piling up, a high-pass filter can be implemented to separate them. After that, a low-pass filter can be used to give our impulses of voltage a more or less Gaussian shape. Since high and low-pass filters can be realized in the simplest way by RC and CR modules, the resulting shaper is often called the $CRRC$ shaper (Figure 1.1). The time after which the shaped signal reaches it's maximum is called the peaking time. Higher orders of filters can also be used to control the peaking time and the tail of the signal. More often than not however, only the low pass filters are designed in higher orders, which would be denoted as $CRRC^M$ shapers, where M is the order of the low pass filter.

Other than separating oncoming impulses and shaping them for optimal analysis, the shaping system also serves a purpose of reducing noise. However, acquiring better signal to noise ratios (SNR) compromises the the level of the signal tail, by making it higher. As it usually goes in electronics, everything needs to be optimized to our needs.

In real shapers, some undershoots of the signal might occur (voltage impulses going into negative values). To combat this, a technique called pole-zero cancellation is used. It's name comes from the fact that it cancels out the pole present in the transfer function of the preamplifier in the s domain. This is usually done by connecting a resistor in parallel to the capacitor of the high pass filter in the shaper [3].

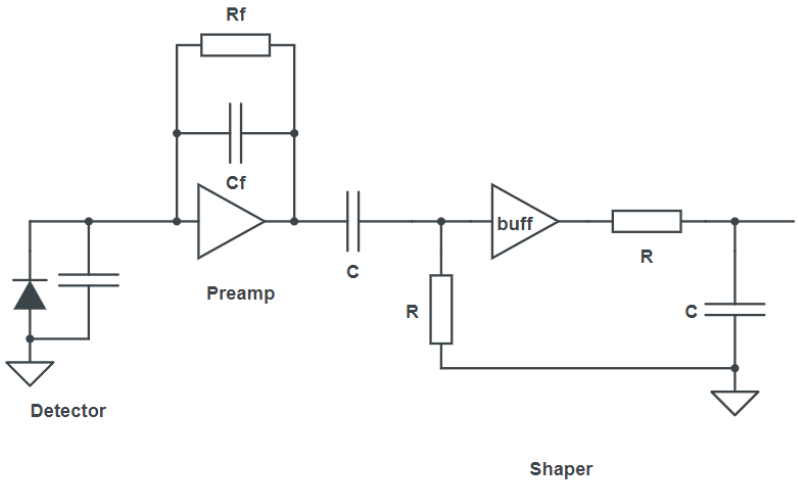

Fig. 1.1. The three first stages of a signal chain: the detector simulated by a diode and capacitor, the preamplifier and shaper processing blocks. The R_f and C_f components connected in the feedback loop to the preamplifier control the time response of the discharging capacitor. The buffer interjecting the high and low-pass filters is an amplifier with an amplification of unity, and it's purpose is to separate the two filters so that they don't supply a load on one another.

1.4. Noise

Fluctuations in our readout might result from a plethora of things. The main types of noise in detectors are: statistical fluctuations of the radiation itself, temperature changes and noise originating from the imperfections of circuit elements. Statistical fluctuations arise from factors intrinsic to the physical processes undergoing in the detector, such as the energies of photons, and energy transport in the crystal lattice. These kinds of noise can be quantified by the so called Fano factor. By definition, the Fano factor is a measure of how much the variance of generated charge carriers in the detector differs from the expected value of variance given by a Poisson distribution. Fano factors differ between detectors and material types, and semiconductor detectors tend to be on the lower end of the spectrum, which means the number of generated carriers in them is consistent.

As for electrical noise, it can be further broken down into: 1/f noise, usually stemming from properties of the material such as the fluctuations of defects or magnetic domains [4][5] [6]; shot noise which occurs when charge carriers travel through a barrier of potential such as the energy gap in semiconductors; thermal noise, originating from different speeds of charge carriers based on their thermal energy.

2. FLAXE application-specific integrated circuit

2.1. General overview

FLAXE is an application-specific integrated circuit designed to be the readout for the electromagnetic calorimeter in the LUXE experiment. LUXE is an ongoing collaboration with DESY in Hamburg, which purpose is to study the strong field regime of the QED theory. The goal is to observe interaction between electrons of energies 16.5 GeV with laser photons, and quantify the rates of interaction in a function of the laser intensity. FLAXE chips will be etched into a sandwich type calorimeter consisting of alternating absorber plates of tungsten and silicon detectors. In the 1mm gaps between the plates, silicon pad detectors are mounted. There are 6 detectors per layer, with 256 pads each, and the dimensions of a pad are 5x5 mm^2. Our chips are responsible for the readout from these pads, and that equals to 1536 channels to read, so 48 ASIC's per layer of the calorimiter. This gives us in total within 768 to 960 chips in order to handle the readout from the entire calorimeter. The better the functionality of the ASIC, the closer it shall be placed to the center of the interaction point of the experiment, so as not to lose valuable data points to readout errors. This is the main motivation for performing qualification tests: grading the chips in order to create a hierarchy of which chips should handle more important areas of silicon pad detectors.

The simplified diagram of the chip can be seen in figure 2.1. It has 32 channels, and is constructed in the CMOS 130nm technology. Each channel has it's own front-end and a 10 bit ADC, both of which will be described more thoroughly in the following sections. After digitalizing the data, it is sent to the internal Data Acquisition System, where the signal is sampled and coded, and sent to the Serial Peripheral Interface.

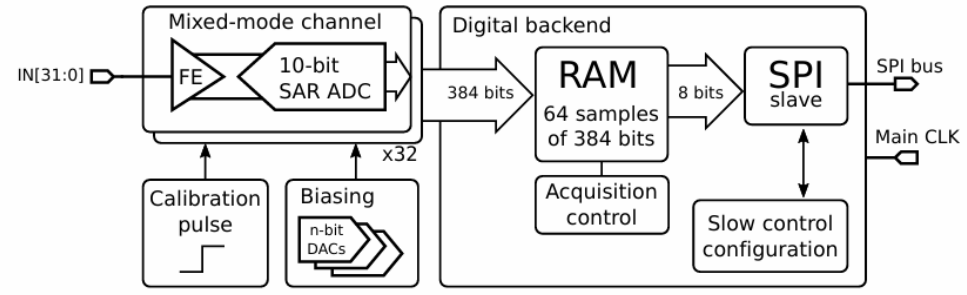

Fig. 2.1. Simplified block diagram of the FLAXE ASIC.

2.2. Analogue front-end

The front-end (Figure 2.2) comprises of a preamplifier, which has two possible gains, interchangeable via switches. One of these gains is adjusted so that the circuit can accept input charges from the entire range of possible charge depositions occurring during the experiment, all the while maintaining an acceptable Signal to Noise Ratio. A Krummenacher feedback is also in place in order to compensate leakage currents from the detector and to set the expected output baseline value [7]. Next is the CRRC shaper, equipped with pole-zero cancellation, to combat undershoots of the signal. It is also fully differential, since the ADC accepts a differential signal as well. The shaper also possesses a trim DAC, which adjusts it's baseline output.

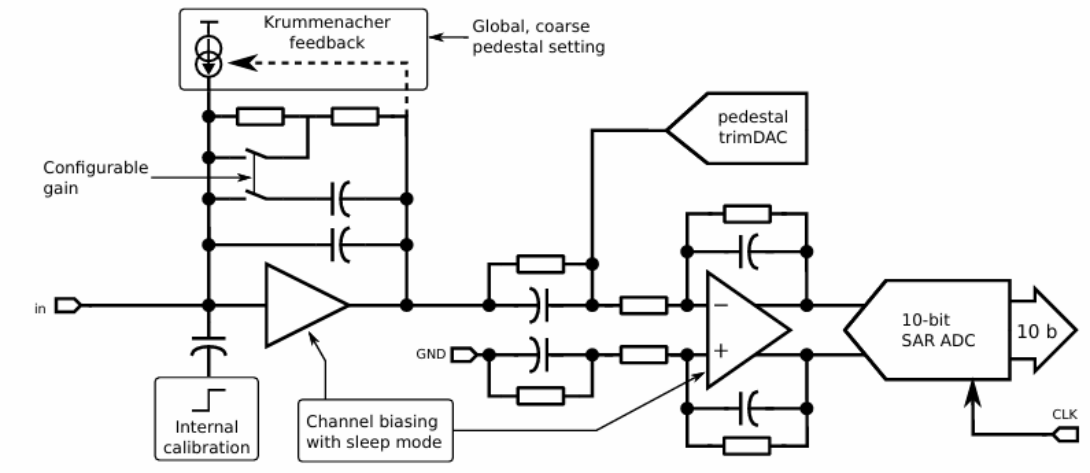

Fig. 2.2. Block diagram of the front-end and ADC. Image source: [8].

2.3. ADC

The ADC (Figure 2.3) present in the FLAXE chip has 10 bits and is of the SAR architecture. SAR stands for Successive Approximation ADC, a technique which adjusts the digital output signal so that it matches the analog input using binary search. In short, the most significant bit is set to 1, and if after going through a DAC, the value of the voltage is higher than the input, the bit is reset, if not, it stays as 1. This process is repeated for the next bits, and in turn we get a digitalized value of the input voltage, as close as possible to the input value. The SAR design was chosen because of it's intrinsic low power consumption, which is always an important factor in readout electronics [9]. Additionally, to reduce power consumption further, a Merged Capacitor Switching scheme is used, along with a split DAC. All bits of the ADC except the least significant one can have their delay before cycling to the next bit changed. This is handled by one of the registers in the Slow Control, described in the Digital back-end sub chapter.

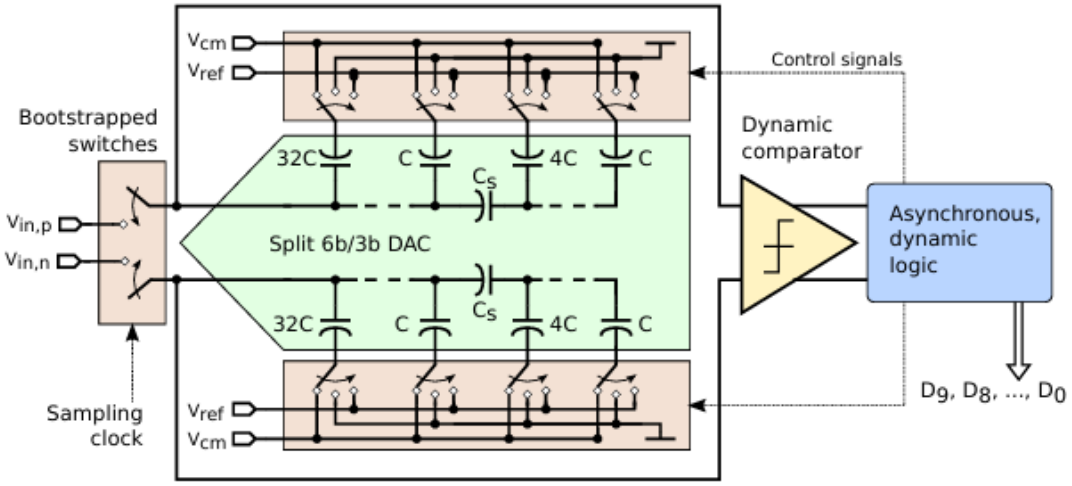

Fig. 2.3. Diagram of the ADC. Image source: [8].

2.4. Digital back-end

The 384 bits outputted from the ADC are sampled by the internal RAM memory of the digital back-end. From there, 8 bits of the samples are sent to the serial peripheral interface (SPI). The SPI protocol involves communication of a master device with a sub device. The desired sub device can be selected by pulling the chip selection input low, and then communication can begin. Data transmission occurs simultaneously, sub and master devices exchange bits at the same time, on the rising edge of the clock originating from the master device. First, the most significant bits are transferred, and they arrive as the least significant to their respective devices. After the next bits arrive, the older bits are moved using shift registers to a more significant position. The final result is that the sub and master device exchanged their bit information exactly.

The digital backened also encompasses the so called slow control. The slow control is a system running on it's own clock, responsible for controlling and checking many parameters of the ASIC. This data is stored in registers, which can be accessed by commands, and it includes information such as DAC values for the preamplifier and Krumenacher feedback, or front-end gain selection. It is also capable of calibrating the impulse voltage, or the delay of ADC bits.

3. FLAXE measurements

Testing of the FLAXE ASICs was carried out in two phases: general qualification tests, and characterization of short circuit currents. The aim of the qualifications tests was to measure the yield of the production, give a general rating of each of the chips, and to single out chips suitable for more thorough testing of their characteristics. The second phase aimed to statistically analyze the nature of short circuits in ASICs that had them.

3.1. Measurement setup

The setup in which the first portion of tests was conducted is shown in Figure 3.1. The setup com-

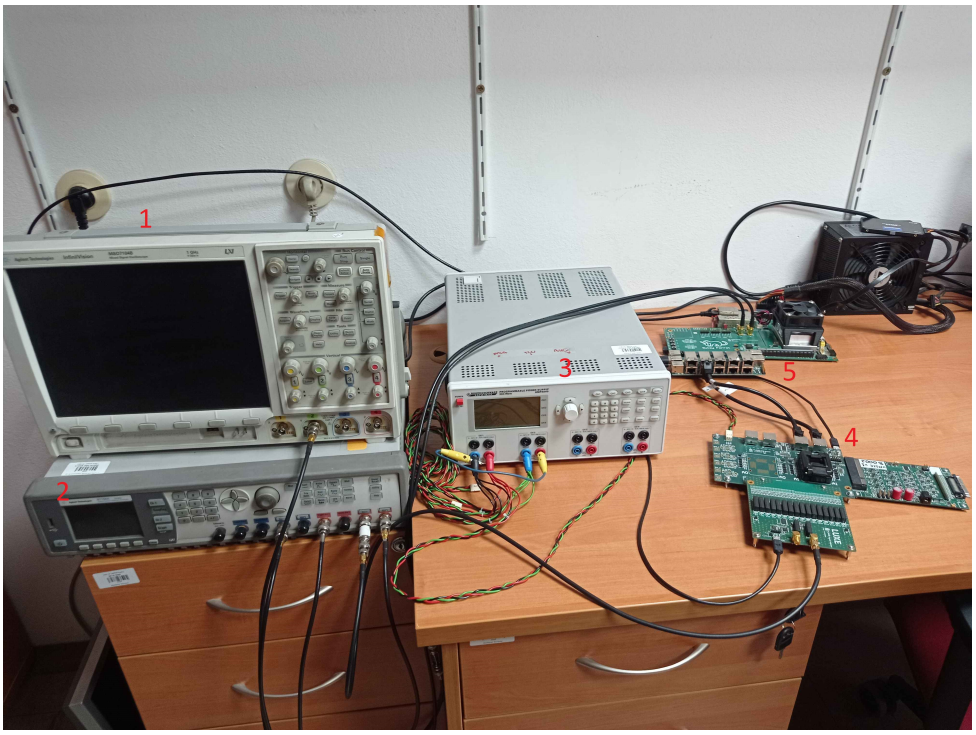

Fig. 3.1. FLAXE qualification measurement setup.

prises of:

– an oscilloscope, labeled as 1

– waveform generator, labeled as 2

– power supply, labeled as 3

– a PCB board with a mechanical interlock where we insert the chip to be tested, labeled as 4

– a PCB board with a field programmable gate array, labeled as 5, which processes and sends data to the computer to the right, out of frame.

The signal generator, oscilloscope and power supply are programmable which is utilized by the programme meant to perform qualification tests, which will be elaborated on in the upcoming section.

3.2. First phase: Qualification tests

A total of 142 ASIC's were tested in the first phase. The chips were lifted from the tray they arrived in via a suction cup, so as not to damage their wiring. Then, they were placed in the mechanical interlock that, when snapped into place, lightly pressed on them to ensure good contacts. A physical contact method of connecting the ASIC to the measurement setup was chosen, because other solutions, such as soldering, would've been inconvenient when performing measurements on a large number of chips.

Qualification measurements are handled by a python programme provided by PhD Jakub Moroń. The software initializes the programmable laboratory equipment and tests the currently embedded chip from various angles. Based on the results, a grade is given to each chip. If a parameter being tested deviates completely or does not work at all, the measurement ends prematurely. Possible grade are: Good, Acceptable, Bad, Failed. The parameters being tested are as follows:

3.2.1. Sequential supply shorts

A simple test for weeding out chips with shortages in them. Each of the power domains in chips were powered on for a brief moment, and if any large voltages (over 1350 mV) were measured, the test was terminated, and the chip considered unsafe for further measurements. Additionally, if any of the domains possessed currents over 600 mA, or voltages below 1050 mV, then the domain's power consumption is rated as Failed, to save some time in the next test, which is more thorough.

3.2.2. Power consumption in sleep and always on modes

These two tests measured the ASIC's power consumption in either their powered on, or powered off states. The specific criteria as to how each of the power domains are graded in accordance to their current is shown in table 3.1. If none of the conditions are fullfilled, the grade is Good.

Table 3.1. Current criteria for grading each of the power domains in power consumption tests.

Rating	FE on	FE off	ADC on	ADC off	Digital
Fail	>160mA	>16mA	>80mA	>8mA	>200mA
Bad	>80mA or <20mA	>8mA	>40mA or <5mA	>4mA	>100mA
Acceptable	>40mA	>4mA	>20mA	>2mA	>40mA

3.2.3. SPI SC register default read and write

First the board is reset, and then 3 attempts are made to read out the default value out of the 62 SPI registers. ASIC's with all correct reads are given a grade of Good, meanwhile all incorrect values result in the Failed grade. Less than 10 errors give a grade of Acceptable, and any other values result in the Bad grade.

Similarly, in the latter half of the test, 3 attempts are made to write a value from a range from 0 to 256, into registers which accept a number (60). The rules for grading are analogous.

3.2.4. Datapath RAM errors and sample input

Four tests regarding the RAM memory were conducted: Datapath RAM output pattern yield, Datapath RAM output virtual address, Datapath RAM error map using input active counter, Datapath RAM input sample counter. Out of those, the two former tests always passed with full success on all chips, so they will be less interesting for us. The active counter test consists of comparing the acquired packaged data to the expected sequence, and calculates the difference between acquired and expected bit word values. The comparison process is repeated for different ADC delay values. The bits with an incorrect value are recorded on a map of all possible 24576 bits (64 samples, 32 channels per sample, 12 bit words per channel). If more than 75% of all 2048 RAM cells have errors, the rating of the ASIC is Failed, more than 50% - Bad. If none of the RAM cells are erroneous, then the ASIC is Good. Any other configuration is given a rating of Acceptable.

The input sample counter test checks whether there are any additional errors in the RAM datapath, unrelated with the known erroneous bits. The unrelated errors can be of wrong bit value, or wrong bit position. Above 100 errors unrelated to the previous input active counter tests gives a rating of Failed, between 10 to 100 - Bad, between 1 to 10 - Acceptable, no errors is a rating of Good.

3.2.5. Biasing DAC's

The biasing DAC test sweeps over all possible DAC values, and measures the appearing analog voltage. Then, it fits a linear funtion to the collected voltages, and computes INL, DNL, Least Significant Bit step voltage (referred to as LSB going forward), and counts the number of missing DAC codes (defined as whenever the DNL of a given DAC assumes a value of -1). Each of the different DAC's is

rated separately, and the tests move to the next stage if at least one of them recieves a grade of Good. The tested DAC's, their range of codes and expected LSB values are as follows: Preamplifier (128 range, 3.4mV LSB), Shaper (128 range, 2.5mV LSB), Krummenacher (32 range, 4.4mV LSB), Calibration (64 range, 9.3mV LSB), Pedestal (128 range, 13.8mV LSB). A single DAC has a grade equal to the worst grade across it's LSB, missing code and DNL grades. When grading LSB, the grade recieved is Failed, Bad, Acceptable when the LSB is below 10%, outside of 50%, and outside of 20% of the expected value, respectively. If the LSB is within 20% of the expected value, the grade is Good. As for DNL, if the maximum value of DNL is above 10, 4, or 2, the corresponding ratings are Failed, Bad, or Acceptable, otherwise the rating is Good. When rating the missing codes, if their amount is larger than 20% or 10% of the maximum code range, then the corresponding grades are Failed or Bad. If the DAC has less than 10% of missing codes but more than 0, then the rating is Acceptable, otherwise the rating is Good.

3.2.6. Channel data readability

Using the RAM error map from datapath RAM error testing (64 samples for 32 channels each), the longest usable (free of errors) ranges in each channel are found. The ranges are sorted by length, channels are paired (channel 0 with 8, 1 with 9, etc.), and the grade is given based on the length of the longest usable range in a channel. Channels with 10 or more consecutive samples without errors are given a grade of Good, and channels with 4 such consecutive samples are given a rating of Acceptable. Lower than 4 is a Bad grade, and 0 is Failed. As for grading the entire chip, if the number of usable channels is equal to 32, the grade is Good, above 16 is Acceptable, and below 16 and 0 are Bad and Failed respectively. A channel is considered "usable" if it was graded Good or Acceptable.

3.2.7. Channel trimDAC's

First, the ASIC acquires sample data for each channel, by sweeping across all possible trimDAC values, and then the signal baseline (Figure 3.62), noise and collected sample count are calculated. After that, the INL, DNL and missing codes of the trimDAC are tested, much like for biasing DAC's. The rating criteria for channels takes into account amount of missing codes, DNL, and LSB. When the amount of missing codes is above 32 or 8: the grade is Failed or Bad. 0 missing codes results in a grade of Good, and anything inbetween 0 and 8 is Acceptable. The full range of trimDAC's is 256 codes. If the maximum DNL is greater than 10, 6, or 3, the grade is Failed, Bad, Acceptable, otherwise it's Good. As for the LSB, if it's below 0.2, the rating is Failed. If the LSB is outside of ranges 0.25-0.65 or 0.35-0.55, the rating is Bad or Acceptable, otherwise it's Good.

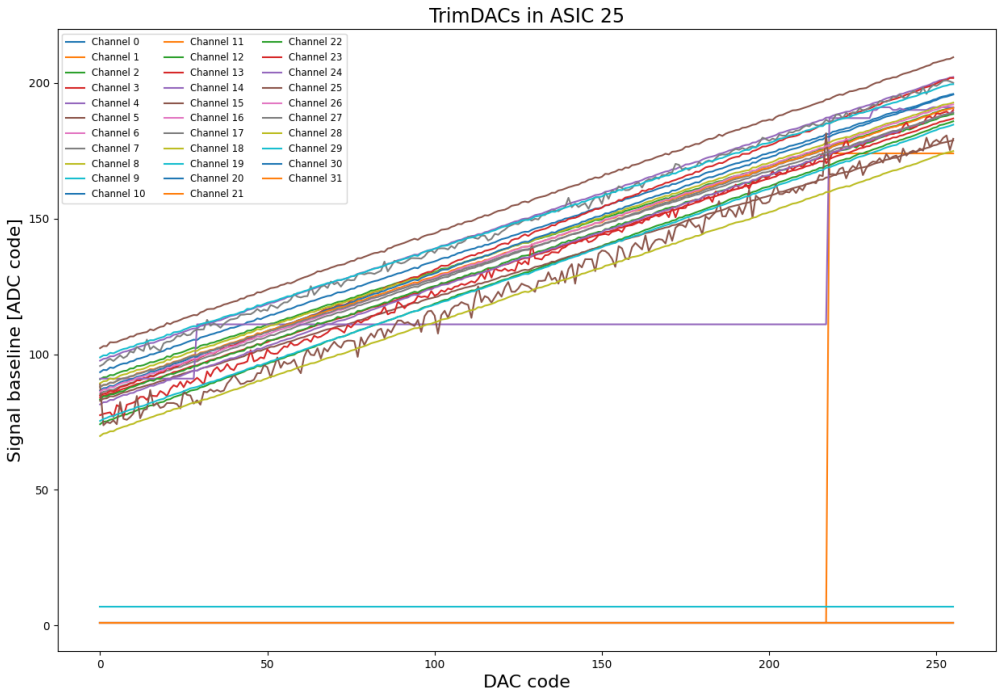

Fig. 3.2. Pedestals of trimDAC's of all channels in ASIC number 25.

3.2.8. Front-end's response, pulse shape, and it's gain

This test injects a test pulse into the ASIC, and measures the delay of the ASIC's response by sending 1000 test packages. The measurements and their statistics come from an oscilloscope. Then, the spread of maximum and minimum delay values is computed, and if it exceeeds 20 ns, then a rating of Failed is given.

After this initial pulse delay is measured, analog tests of whether the front-end's response is of the correct shape and gain, begin. The parameters by which we quantify whether the response shape is that of the theoretical CRRC shape are: amplitude, peaking time and tail level. These parameters, and the gain of the signal, are graded on the basis whether they are within 5, 10 or 25% of the expected values. Then, the measurement is repeated for all channels, and each channel is given a rating based on all 3 aforementioned metrics, which later sums up into the overall rating of the entire chip. On Figure 3.3 is an example plot showing the pulse shapes of all channels in ASIC number 25, which has 19 functioning channels in total. As seen on the Figure, the non functioning channels are either completely dead, have large amounts of noise, or don't come close to the theoretical CRRC shape. The gain plot for the same chip can be seen on Figure 3.4.

After the initial results from the first phase of the measurements, it seemed that the yield of the ASIC's is rather terrible; Only 11 out of 142 were usable at all, and even then they left much to be desired. The main filters for our chips seem to be tests of supply shorts, power consumption in sleep

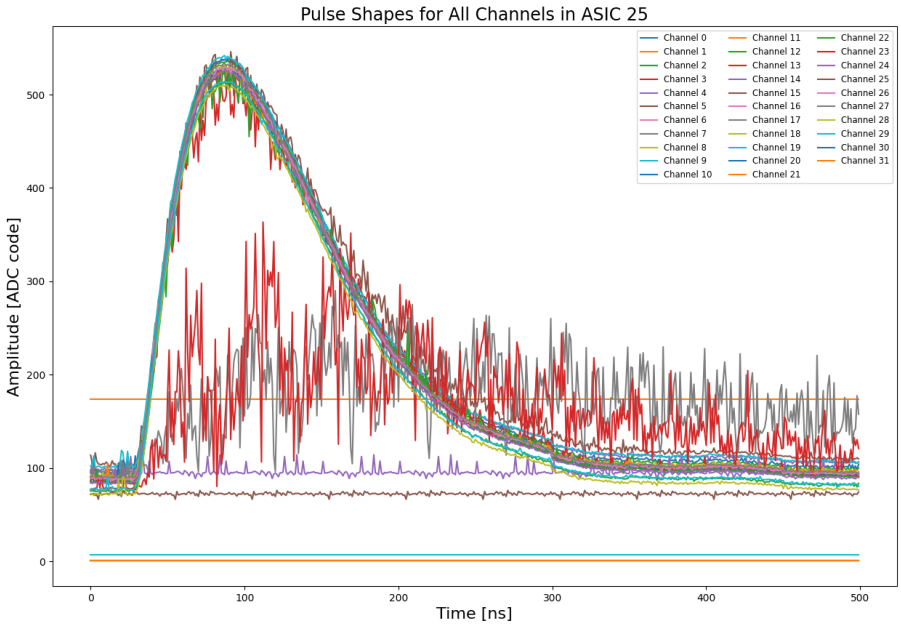

Fig. 3.3. Pulse shapes of all channels in ASIC number 25.

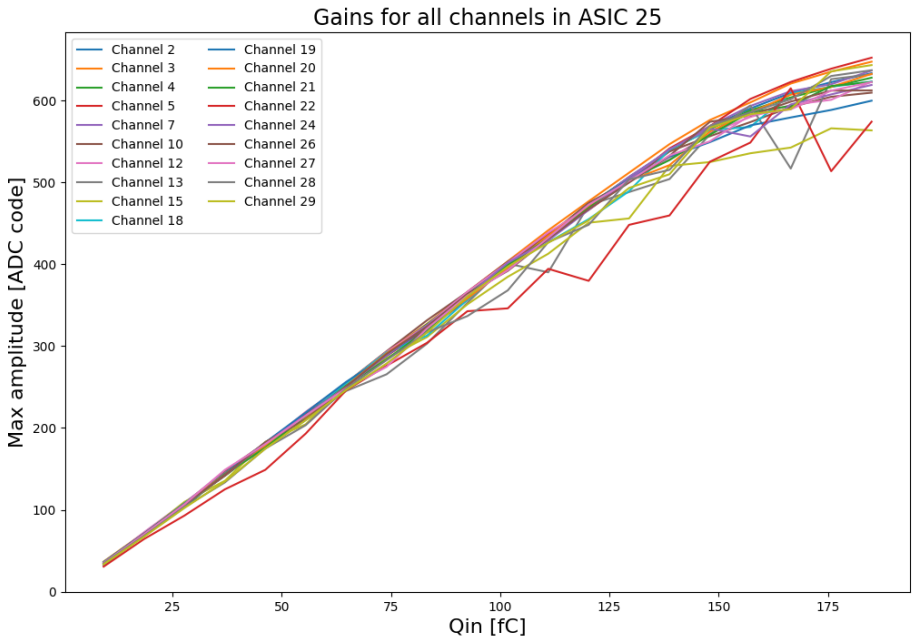

Fig. 3.4. Gains for all channels in ASIC number 25.

mode, SPI register write, datapath RAM errors and channel data readability. These results gave all the

more reason to investigate supply shorts further, as this was a major problem, but relatively easy to investigate.

3.3. Second phase: Supply shorts

The objective of the second part of measurements was to examine and statistically present the nature of shorts in all ASIC's that had them, of which there were 50. The setup comprised of the same mechanical interlock as used before, a power supply, and an ammeter. The measurement process consisted of changing the voltage supplied to each of the domains of the ASIC (front-end, ADC, and digital back-end), from 100 to 1200 millivolts in steps of 100 mV, and measuring the flowing currents, all of which was done manually. Results were initially recorded in a spreadsheet, but a Python programme was later written that converted the spreadsheet data into vectors for easier manipulation. After taking all measurements, the programme which imported data from excel to python vectors was further developed to recognize whether the resistance in each of the domains has an ohmic or di ohmic character; As in whether the current dependence as a function of voltage is a single straight line or whether the linearity coefficient changes at some point. The software does this by calculating and comparing finite differences between two points. If the difference is greater than a given threshold, the software takes this point as the inflection point of the curve and starts comparing again with a new finite difference. Later, it calculates the ohmic resistance of one or two slopes and draws histograms with collective information, such as the resistance for one or two slopes for each domain and the voltage at which the linear factor for each domain changes.

Some of the more prominent results are shown in Figures 3.5, 3.6 and 3.7, meanwhile the rest is included in the appendix (Figures 3.15 to 3.39).

The behavior of supply short currents in chip number 123 (Figure 3.5) is an example of single ohmic behavior. All domains show a more or less linear dependancy of current to voltage, which suggests that the nature of the shortages is like that of an ohmic resistor.

Naturally, there were also chips which showed the opposite, di ohmic behavior. Chip number 31 (Figure 3.6) is the prime example of when the domains of the chip exhibit di ohmic characteristics. A very distinct breach of the curve can be seen at around 500 millivolts in all of the domains, which naturally correlates to the resistance of the shortages changing from one value to another after this point is exceeded.

Most commonly, however, not all domains had the same characteristics. As seen on the example of ASIC number 101 (Figure 3.7), the digital and ADC domains exhibit a single ohmic nature, meanwhile the front-end's current is di ohmic in nature. Many permutations are present in data, but this particular combination proved to be the most common when summary data was visualized.

During this stage of measurements, one unexpected event took place as well. Chips 1 and 2, which originally had failed the supply short test, showed currents below 100 milliamperes in the second phase of the measurements across all domains. Initial qualification tests were repeated, and both chips received

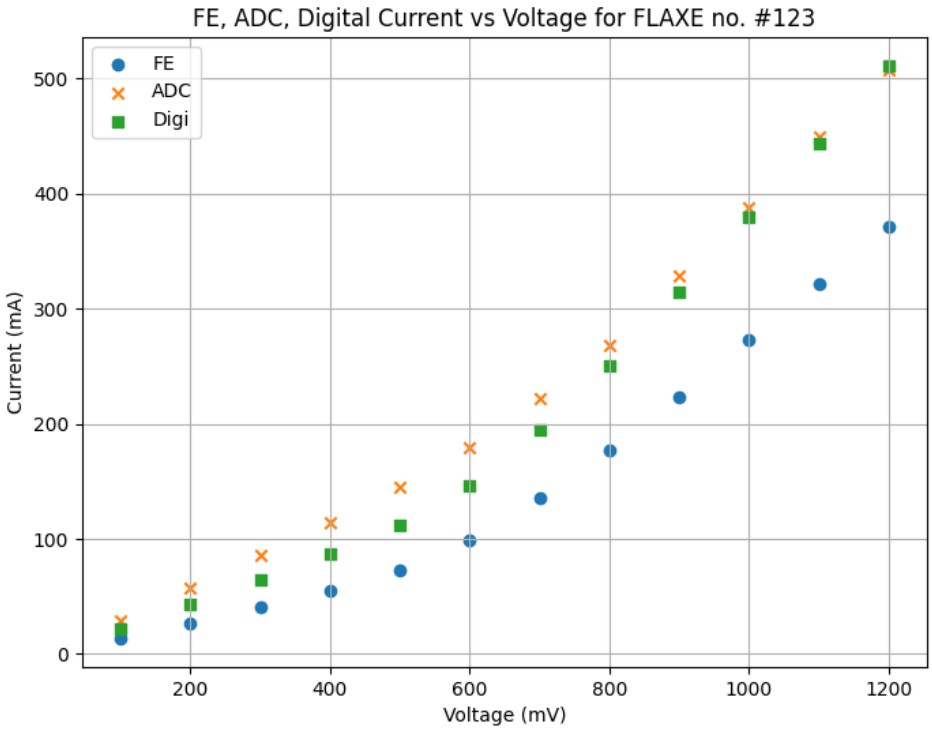

Fig. 3.5. Plot showcasing shortage currents for each of the domain in ASIC no. 123 in the function of voltage.

an overall grade of "Acceptable". It is unlikely that these two chips were measured incorrectly because, as the first two chips, tests were performed on them quite frequently. One theory could be that those chips were undergoing some gradual internal changes, which only revealed themselves in the second phase of testing, which took place roughly one month after the first. Another anomaly was chip number 68, in which the front-end wasn't functioning at all, supply short current was 0 across all voltages.

Since 49 plots of supply shorts in total were produced, there came a need to present data in a more concise and compacted manner. The data chosen to be presented are as follows:

– the number of chips which exhibit a single ohmic or di ohmic characteristic of supply shorts

– resistance of single ohmic chips

– resistances of di ohmic chips (both slopes)

– di ohmic breakpoint voltage.

Di ohmic characteristics counted 42 for the front-end, 10 for the ADC and 8 for the digital domains. Conversely, single ohmic characteristics counted 6 for the front-end, 39 for the ADC and 41 for the digital domains. The number of total characteristics for the front-end doesn't add up to 49, since one chip had an entirely nonfunctional front-end domain. The rest of the information has been compiled into

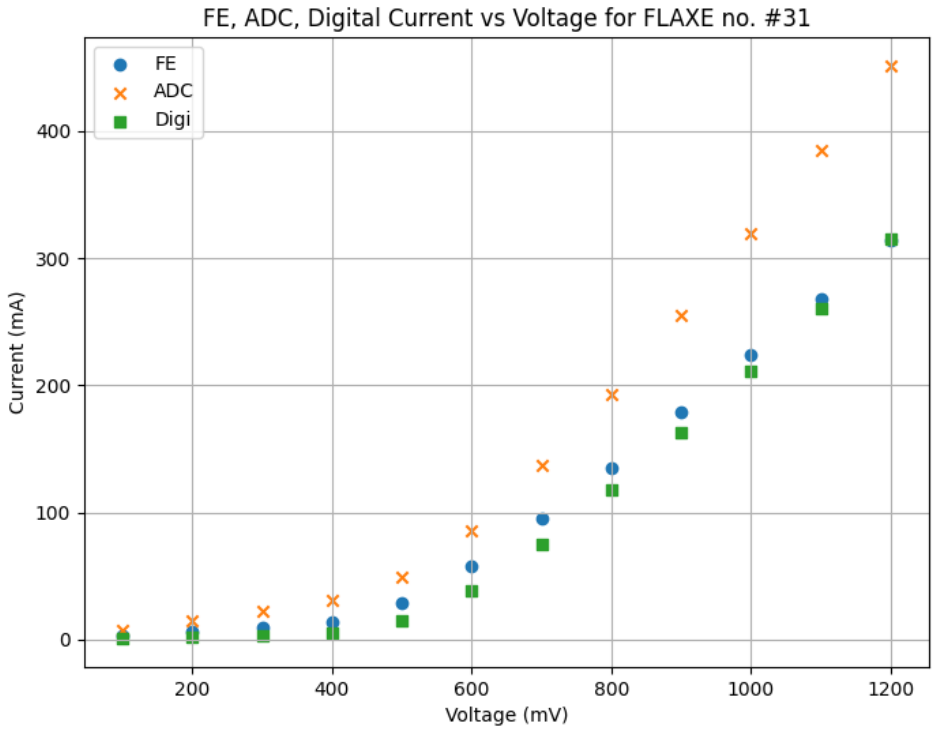

Fig. 3.6. Plot showcasing shortage currents for each of the domain in ASIC no. 31 in the function of voltage.

histograms. The resistances of single and di ohmic chips were easily calculated as the linear coefficients of appropriate slopes. As for the breakpoint voltage, it's value was naturally obtained as the programme had to recognize whether the chips behavior was single or di ohmic. Sample histograms are shown in the subsequently mentioned Figures, meanwhile their complete set can be found in the appendix (Figures 3.40 to 3.45).

We see the dominant value for ohmic resistance in the digital domains with a single ohmic resistance characteristic is 2.5 ohms (Figure 3.8). Overall the values are quite low, within a few to a dozen ohms throughout the entire data set. The analogous histogram for ADC is similar: the majority of values are below 10 ohms, however there is an outlier at 100 ohms.

The resistances of the first (within 0 to 700 mV) slopes in di ohmic behavior also tend to oscillate within a few ohms. As for the second slope, it depends on the domain; the digital domain seems to posses a resistance of a few ohms on average, with one outlier, and so does ADC, albeit the amount of data there is quite low, so nothing concrete can be said (Figure 3.9). Front-end's ohmic resistance on the second slope seems to be slightly larger, approaching values of 25 ohms (Figure 3.10). The supply short curves for both ADC and front-end tend to break down at voltages between 600 to 700 mV.

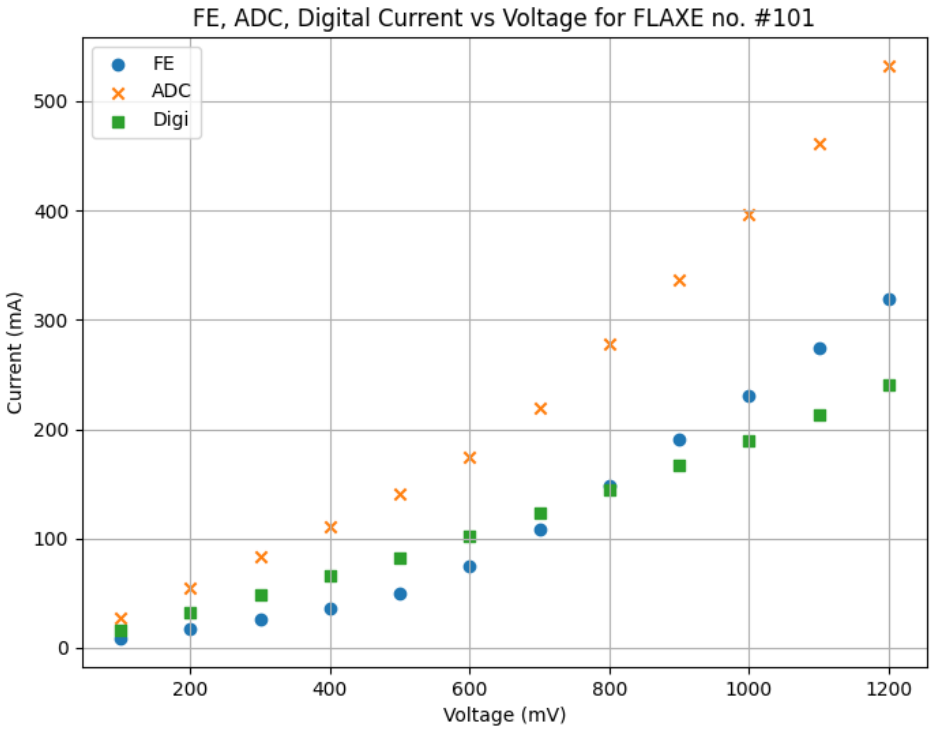

Fig. 3.7. Plot showcasing shortage currents for each of the domain in ASIC no. 101 in the function of voltage.

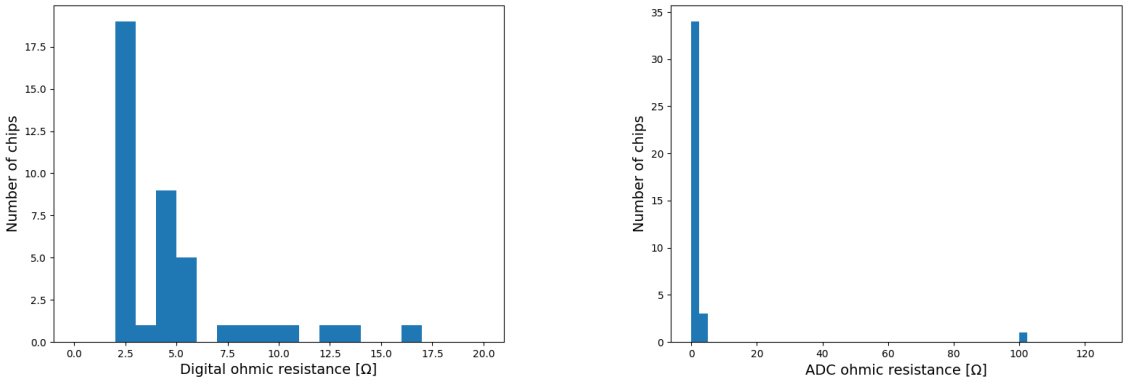

Fig. 3.8. Histogram of ohmic resistances for the digital domain (left) and ADC domain (right) when the behavior of supply shorts was single ohmic.

3.4. Summary of FLAXE measurement results

After performing the qualification tests, summary information about the production yield and the grades of each of the chip's qualities was compiled in the form of table 3.2. Additionally, where applicable, histograms were plotted in order to learn about the general behavior of parameters such as the peaking time of the shaper or the gain of the front-end.

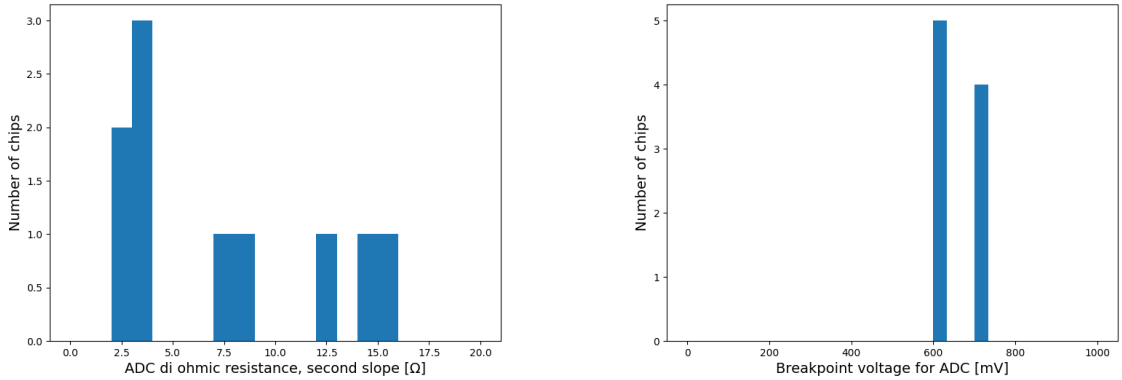

Fig. 3.9. Histogram of ohmic resistances for the ADC domain when the behavior of supply shorts was di ohmic (left) and the breakpoint voltage values for that domain (right).

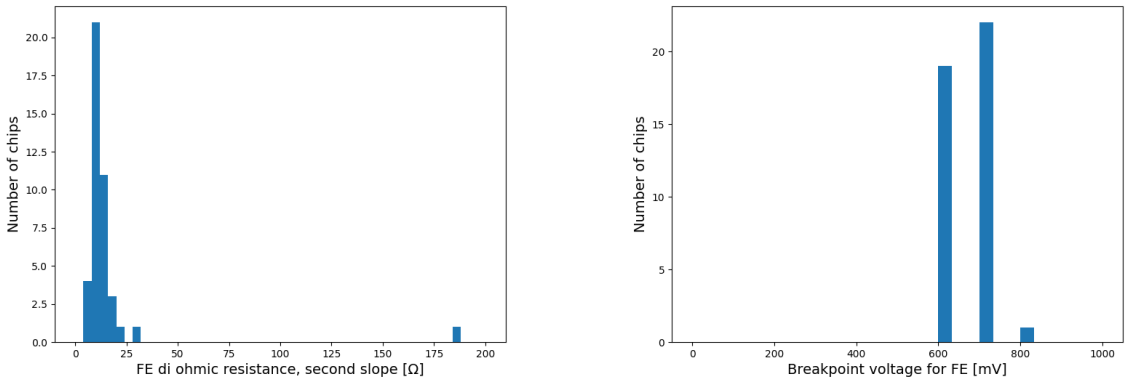

Fig. 3.10. Histogram of ohmic resistances for the front-end domain when the behavior of supply shorts was di ohmic (left) and the breakpoint voltage values for that domain (right).

As for analog tests, only 21 out of the batch of 142 chips managed to get to this part of qualification tests without any previous critical failures. Of these 21, 11 had any usable channels. In total, 215 out of 672 channels are working (39.9%). Channels that do work, in 91.6% of cases, have a peaking time within 10% of the expected value of 53 nanoseconds, as can be seen on Figure 3.11 (the median of the measurements is 53.82 ns). As for the gain of the front-end (Figure 3.12), 98.7% of the working channels have a gain within 10% of the expected value of 4 LSB/fC. From these results it is apparent that the issue with the front-end isn't the parameters themselves, but rather the fact that not many channels are functional on average per chip.

In the end, only 7 of the chips managed to pass the last analog tests with a grade of acceptable and pass all previous tests. Out of those seven, one chip had to be taken down a grade, because of it's poor channel readability, so we end up with 6 chips that might at all be used in the experiment. Summary data

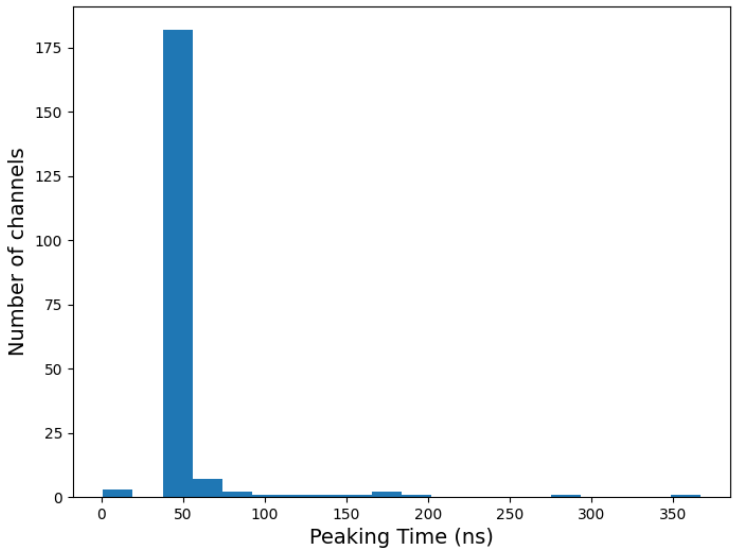

Fig. 3.11. Histogram of peaking times in all working channels across 11 chips. Only positive values of peaking times were included.

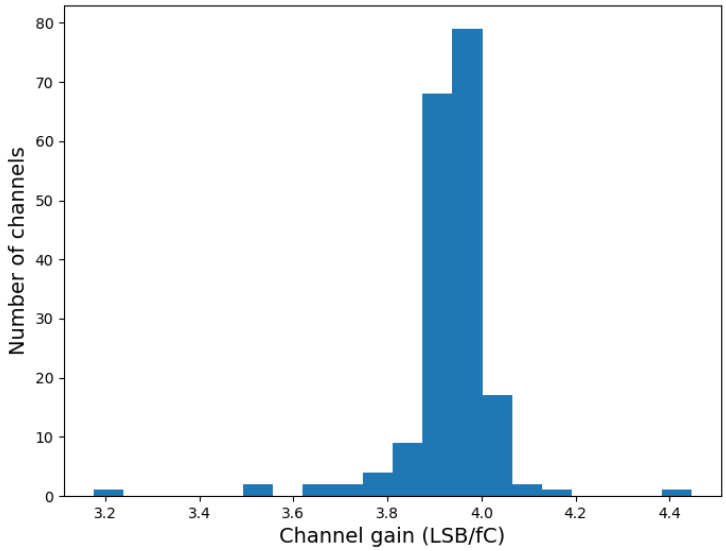

Fig. 3.12. Histogram of front-end gains in all working channels across 11 chips.

about these working chips is included in table 3.3. We can see that the functioning of one analog system, correlates with functioning of all other systems, with the exception of chips 25 and 84, which have a lower number of channels in which the pulse shape is correct. Out of those 6 working ASIC's, the best one is chip number 136, with 30 working channels, 29 Good channels, and 1 erroneous RAM memory

cell. The plots of this ASIC's pulse shape, gain and trimDAC's can be seen in Figures 3.13 and 3.14. The same plots for the rest of the chips are in the appendix (Figures 3.46 to 3.62).

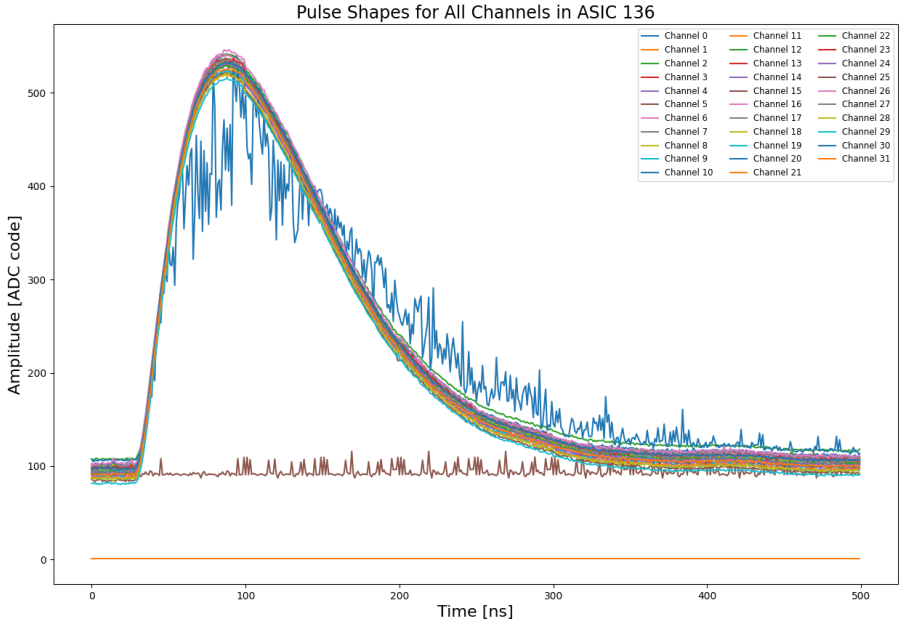

Fig. 3.13. Pulse shapes of all channels in ASIC number 136.

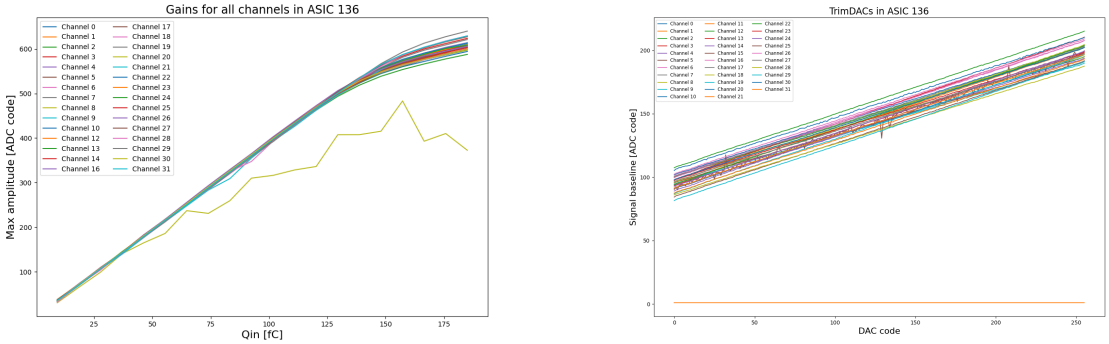

Fig. 3.14. Plots of gain (left) and trimDAC pedestals (right) for ASIC number 136.

Table 3.2. Aggregated results of qualification tests.

Test	Good	Acceptable	Bad	Failed
Overall ASIC yield	0 [0%]	6 [4.2%]	5 [3.5%]	131 [92.3%]
Supply shorts	92 [64.8%]	0 [0%]	0 [0%]	50 [35.2%]
Power consumption in sleep mode	7 [7.6%]	9 [9.8%]	30 [32.6%]	46 [50%]
Power consumption in always on	6 [12.8%]	9 [19.1%]	25 [53.2%]	7 [14.9%]
SPI SC register default read	33 [35.9%]	10 [10.9%]	46 [50%]	3 [3.3%]
SPI SC register write	10 [10.9%]	16 [17.4%]	21 [22.8%]	45 [48.9%]
Datapath RAM error map	0 [0%]	18 [38.3%]	3 [6.4%]	26 [55.3%]
Datapath RAM input sample	41 [87.2%]	3 [6.4%]	2 [4.3%]	1 [2.1%]
Biasing DAC's	17 [36.2%]	15 [31.9%]	1 [2.1%]	14 [29.8%]
Channel data readability	5 [10.6%]	12 [25.5%]	4 [8.5%]	26 [55.3%]
Channel trimDAC	0 [0%]	19 [90.5%]	1 [4.8%]	1 [4.8%]
FE response and pulse shape	0 [0%]	7 [33.3%]	4 [19%]	10 [47.6%]
FE gain	0 [0%]	7 [33.3%]	4 [19%]	10 [47.6%]

Table 3.3. More specific information about the chips which had passed analog testing.

Chip Number	No. of working channels	No. of correct trimDAC's	No. of correct shapes	No. of correct gains
25	19	20	11	16
32	26	25	25	26
76	22	23	19	20
84	27	28	16	27
136	30	30	28	29
139	27	27	25	26

Summary

Using software provided by the faculty, qualification tests of the first batch of 142 FLAXE ASIC's were conducted. Some of the collected data is included in this thesis, meanwhile the rest is present on an internet site created by faculty staff *http://asic.fis.agh.edu.pl/luxe/index.html*. Based on the initial results of the qualification tests, further production of the chips was halted. Later down the line, supply shorts were studied more closely. Currents flowing in each of the domains were measured in a function of voltage up to 1200 mV, and a programme was written which detected if these linear dependencies break down, and where. Afterwards, plots and histograms were created which illustrated the nature of the supply shorts, or analog tests results, such as pulse shape, trimDAC pedestals and signal gain.

Overall, the yield of the production came out to be 7.7% of the total amount of chips, and that is counting chips which were quite deficient, with the second to worst grade. Needless to say, such results are unacceptable for the purposes of the LUXE experiment. The main bottlenecks for our chips seem to be the tests of supply shorts, power consumption in sleep mode, slow control register write, and issues with RAM memory and channel readability. Such predicaments might suggest that the fault lies on behalf of the production process, rather than the design of the chips. Di ohmic characteristics dominate in the front-end, meanwhile the ADC and digital back-end usually exhibit a single ohmic characteristic. If the dependencies for the front-end or ADC break down, they do so between 600 to 700 mV the majority of the time.

Appendix

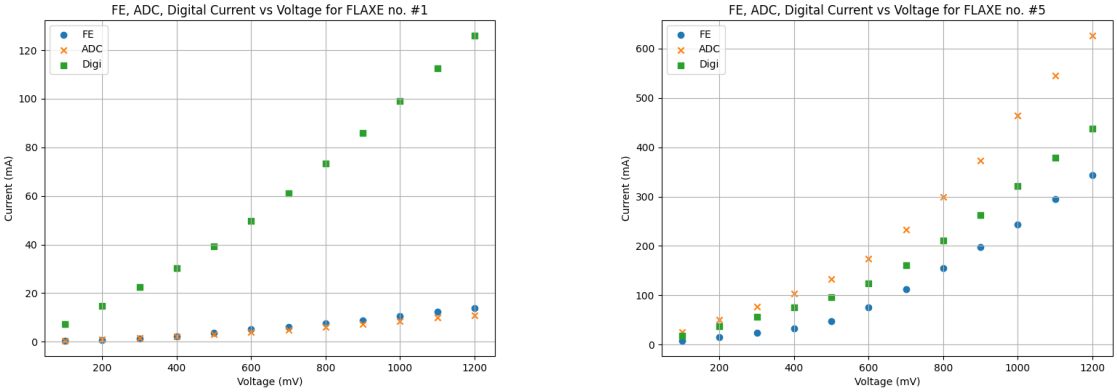

Fig. 3.15. Shortage currents in each of the domains in chip number 1 (left) and number 5 (right) in the function of voltage.

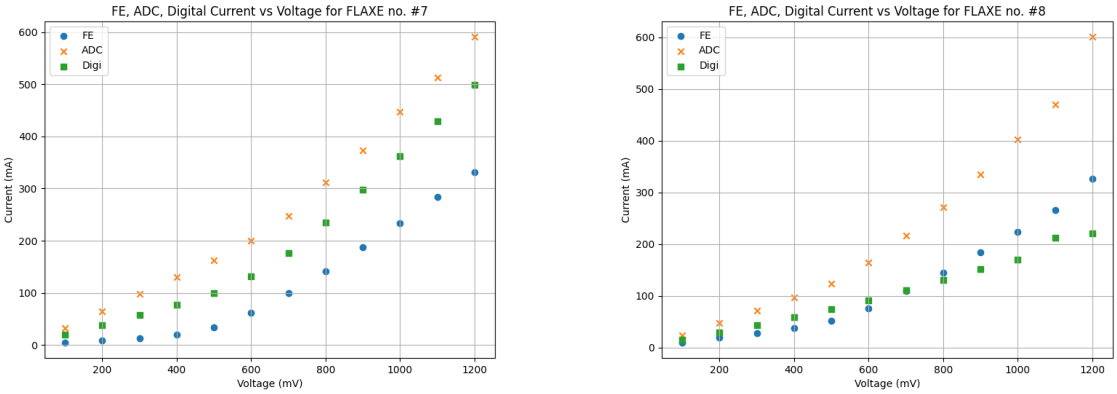

Fig. 3.16. Shortage currents in each of the domains in chip number 7 (left) and number 8 (right) in the function of voltage.

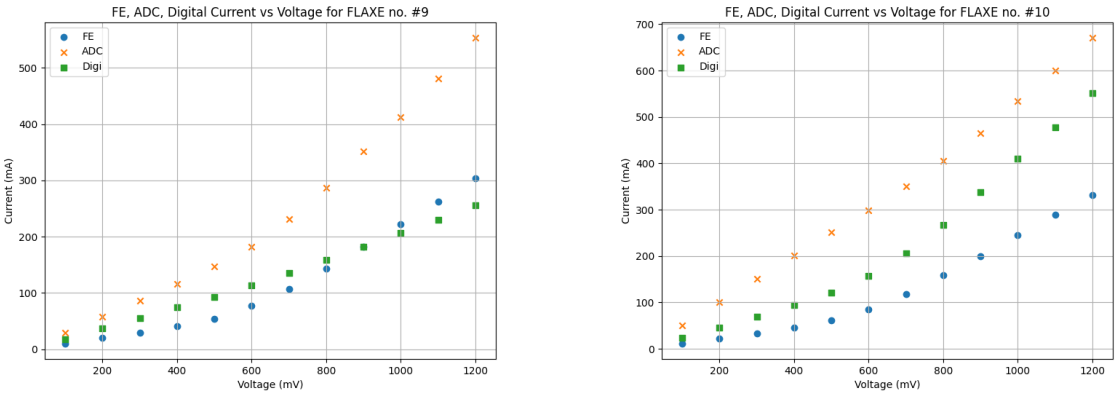

Fig. 3.17. Shortage currents in each of the domains in chip number 9 (left) and number 10 (right) in the function of voltage.

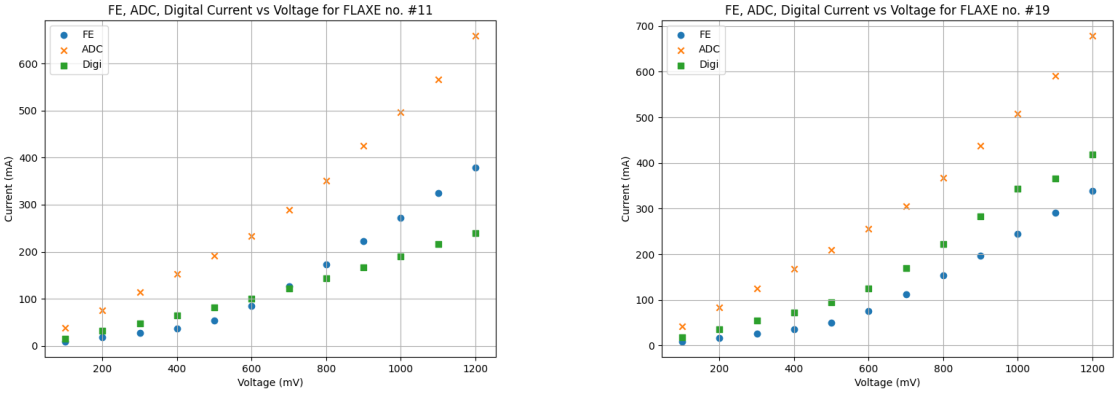

Fig. 3.18. Shortage currents in each of the domains in chip number 11 (left) and number 19 (right) in the function of voltage.

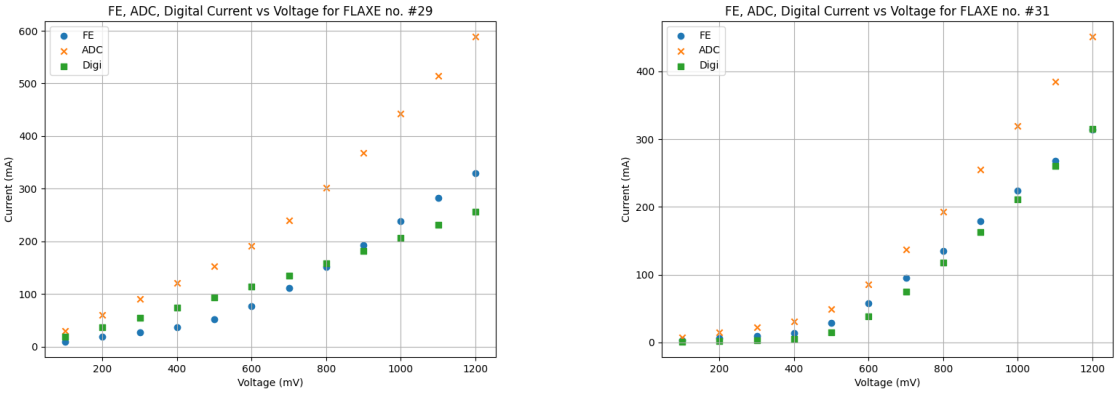

Fig. 3.19. Shortage currents in each of the domains in chip number 29 (left) and number 31 (right) in the function of voltage.

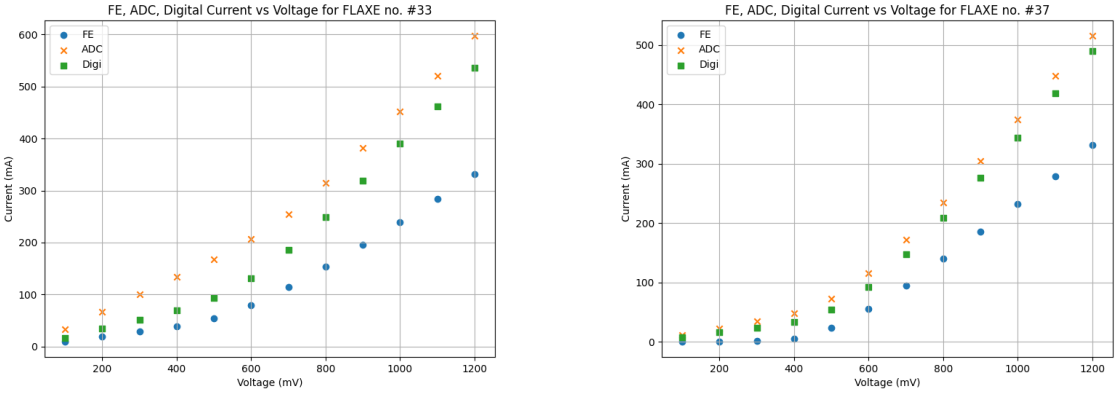

Fig. 3.20. Shortage currents in each of the domains in chip number 33 (left) and number 37 (right) in the function of voltage.

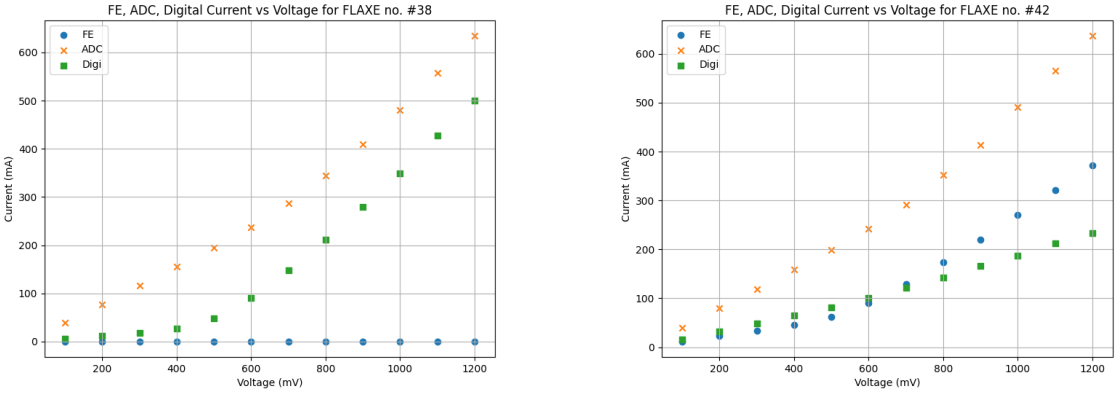

Fig. 3.21. Shortage currents in each of the domains in chip number 38 (left) and number 42 (right) in the function of voltage.

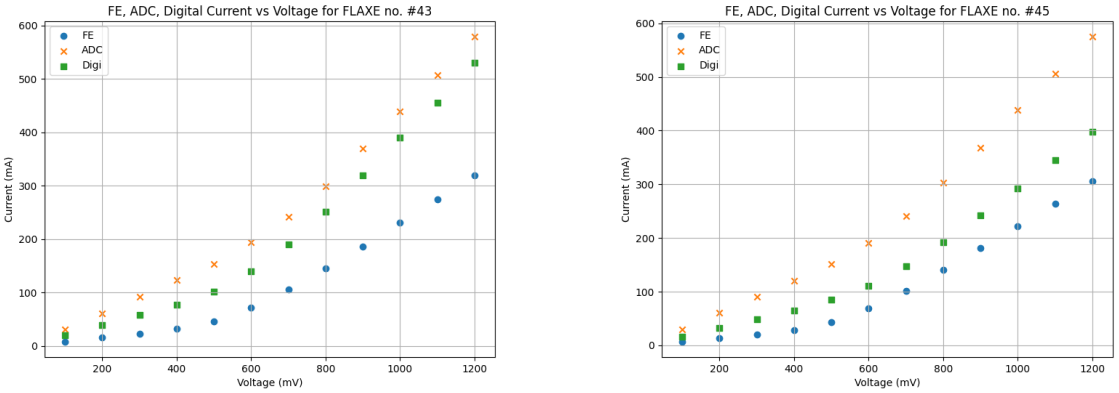

Fig. 3.22. Shortage currents in each of the domains in chip number 43 (left) and number 45 (right) in the function of voltage.

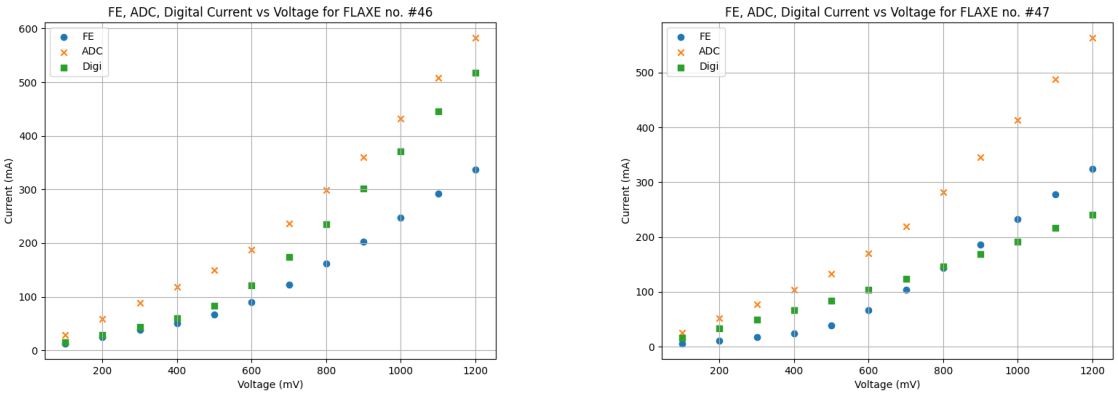

Fig. 3.23. Shortage currents in each of the domains in chip number 46 (left) and number 47 (right) in the function of voltage.

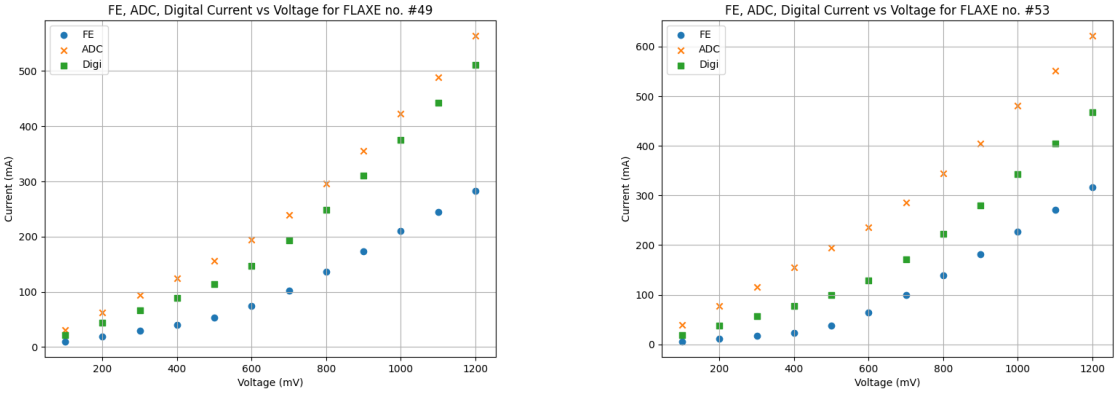

Fig. 3.24. Shortage currents in each of the domains in chip number 49 (left) and number 53 (right) in the function of voltage.

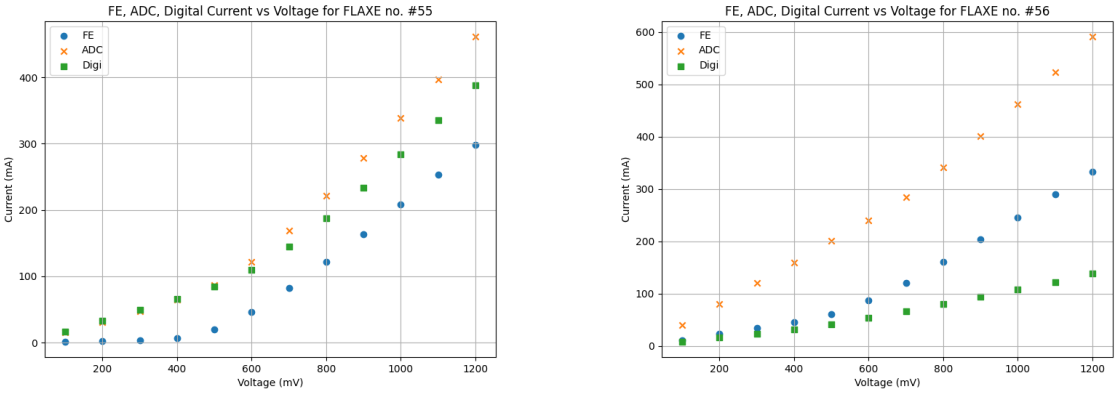

Fig. 3.25. Shortage currents in each of the domains in chip number 55 (left) and number 56 (right) in the function of voltage.

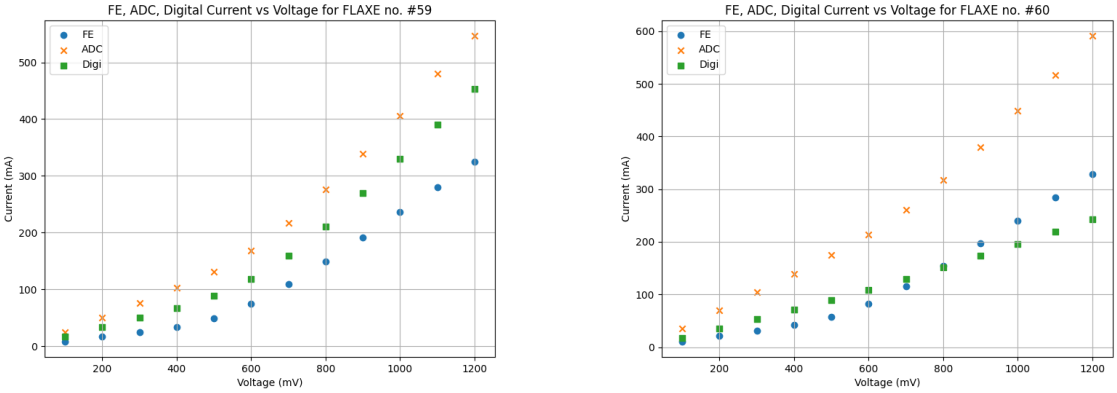

Fig. 3.26. Shortage currents in each of the domains in chip number 59 (left) and number 60 (right) in the function of voltage.

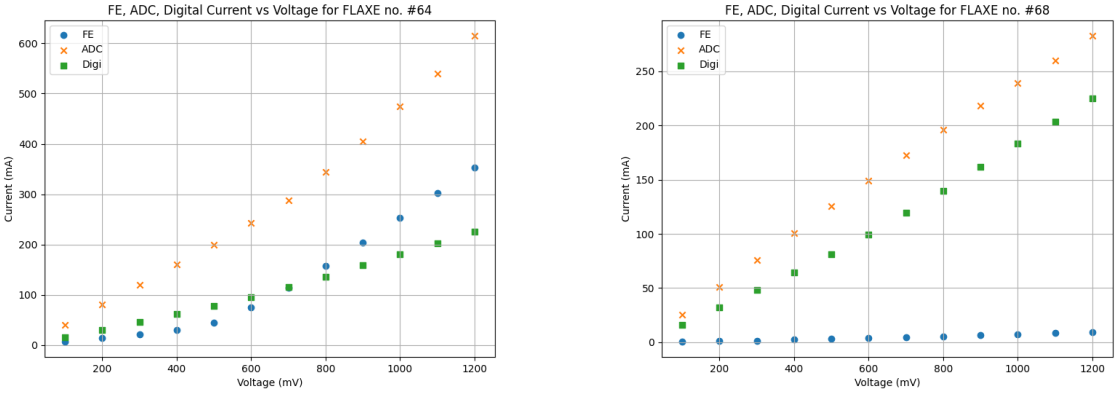

Fig. 3.27. Shortage currents in each of the domains in chip number 64 (left) and number 68 (right) in the function of voltage.

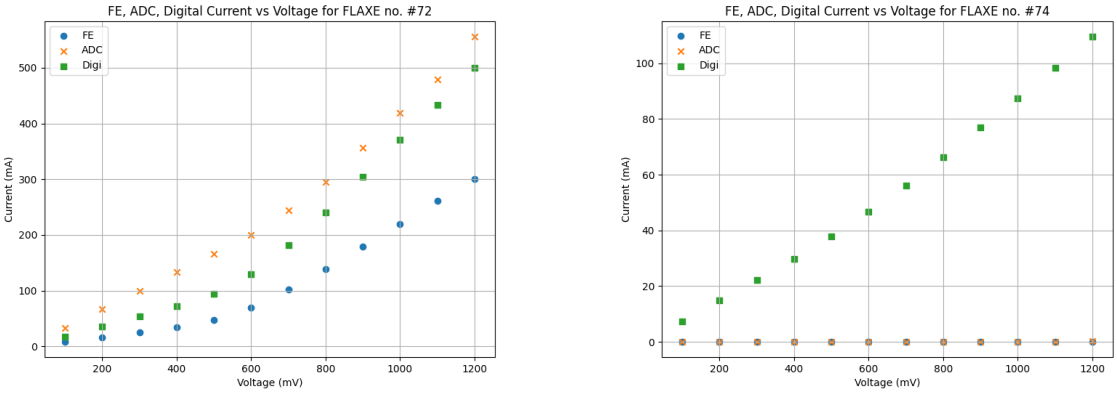

Fig. 3.28. Shortage currents in each of the domains in chip number 72 (left) and number 74 (right) in the function of voltage.

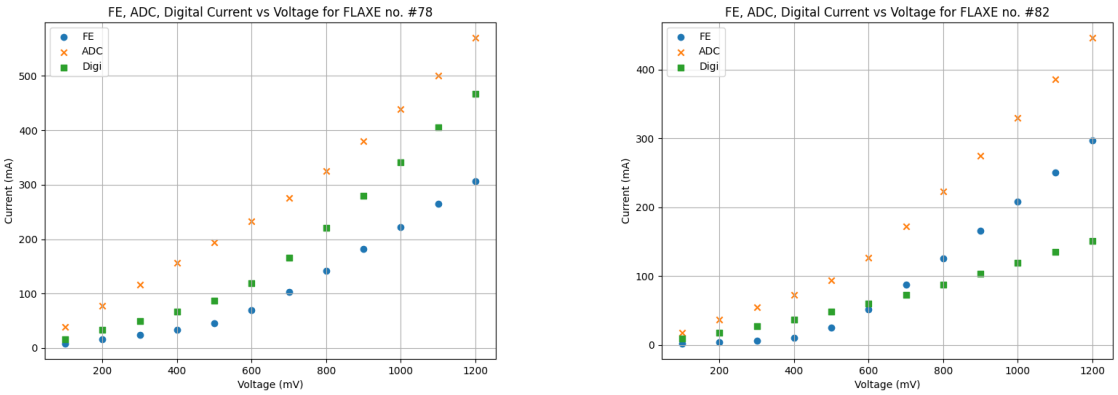

Fig. 3.29. Shortage currents in each of the domains in chip number 78 (left) and number 82 (right) in the function of voltage.

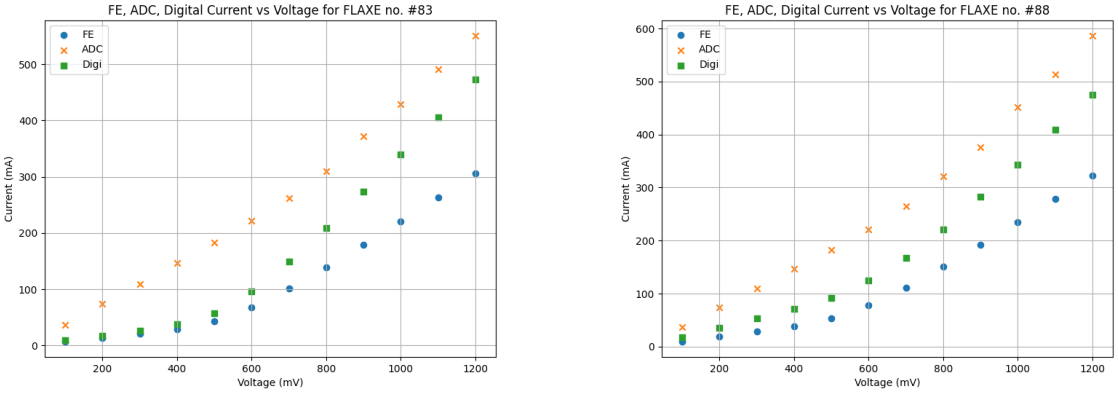

Fig. 3.30. Shortage currents in each of the domains in chip number 83 (left) and number 88 (right) in the function of voltage.

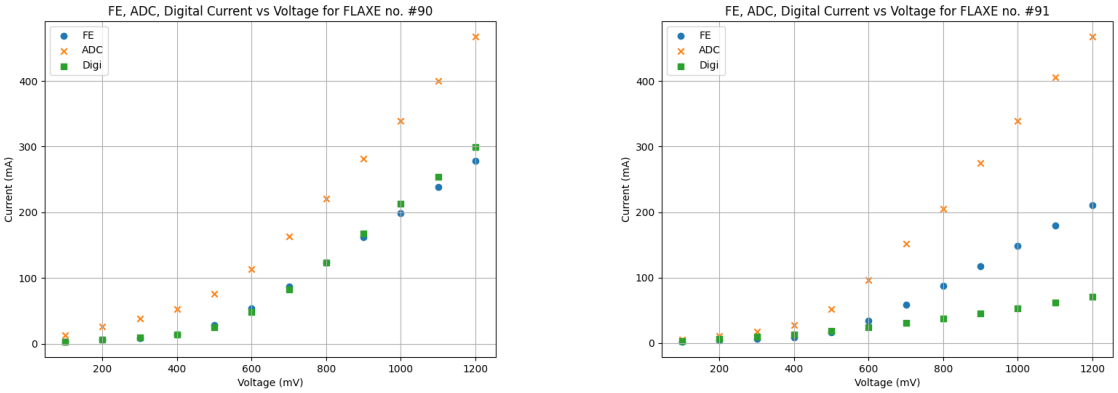

Fig. 3.31. Shortage currents in each of the domains in chip number 90 (left) and number 91 (right) in the function of voltage.

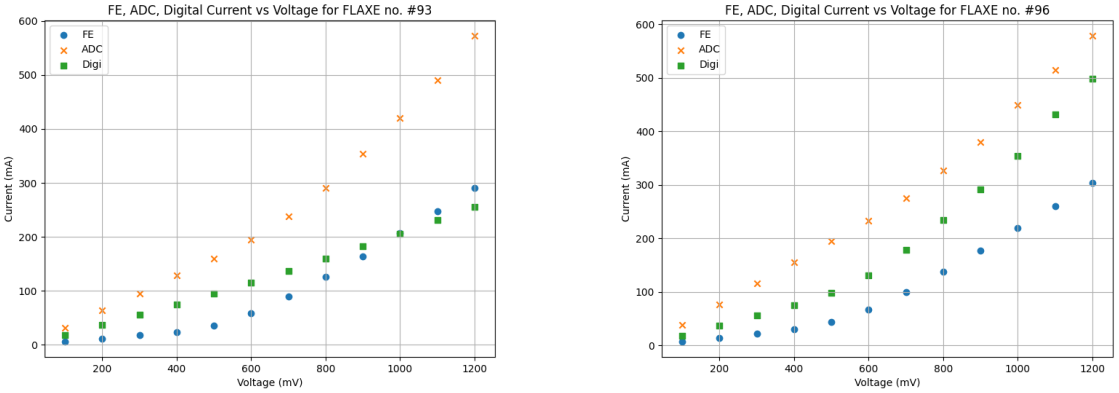

Fig. 3.32. Shortage currents in each of the domains in chip number 93 (left) and number 96 (right) in the function of voltage.

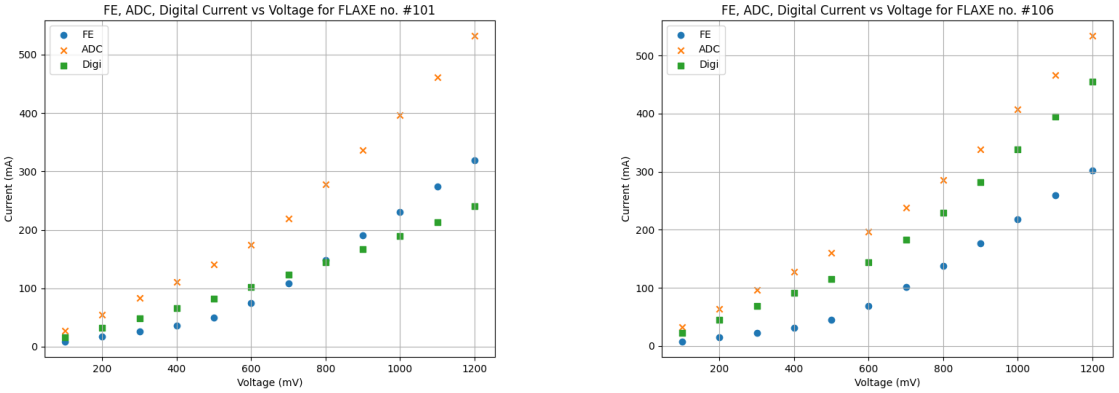

Fig. 3.33. Shortage currents in each of the domains in chip number 101 (left) and number 106 (right) in the function of voltage.

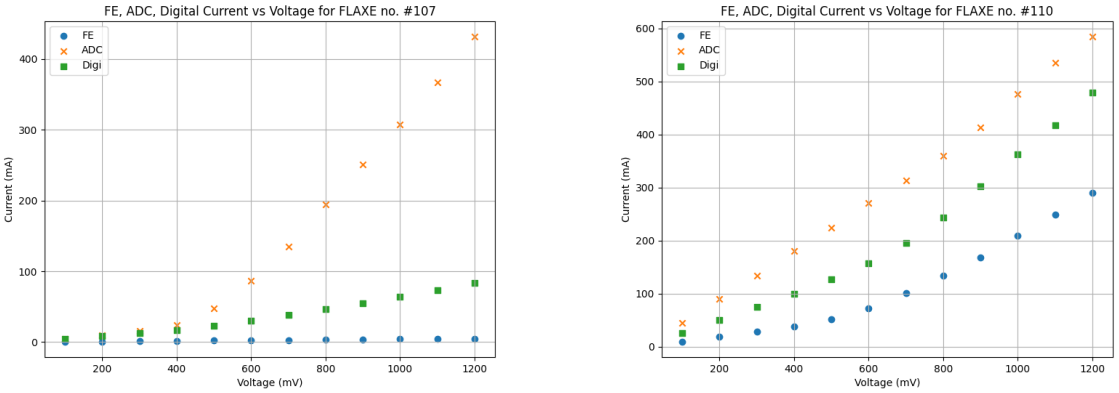

Fig. 3.34. Shortage currents in each of the domains in chip number 107 (left) and number 110 (right) in the function of voltage.

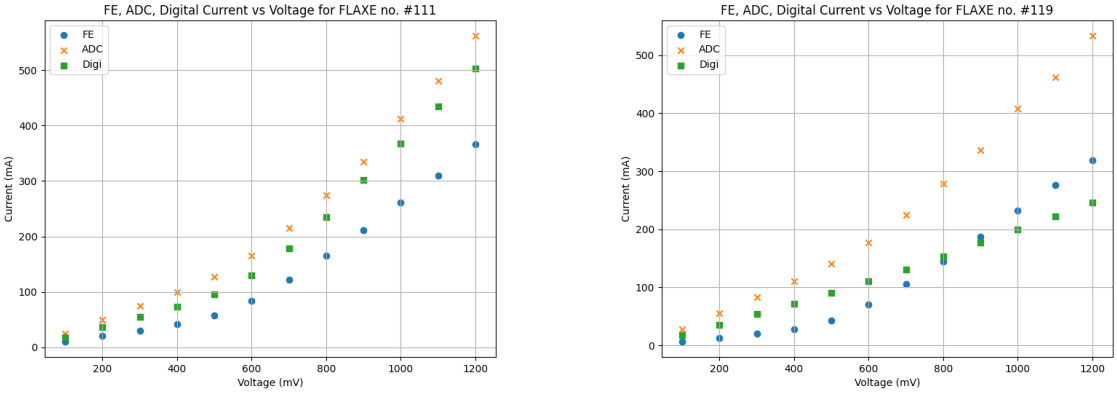

Fig. 3.35. Shortage currents in each of the domains in chip number 111 (left) and number 119 (right) in the function of voltage.

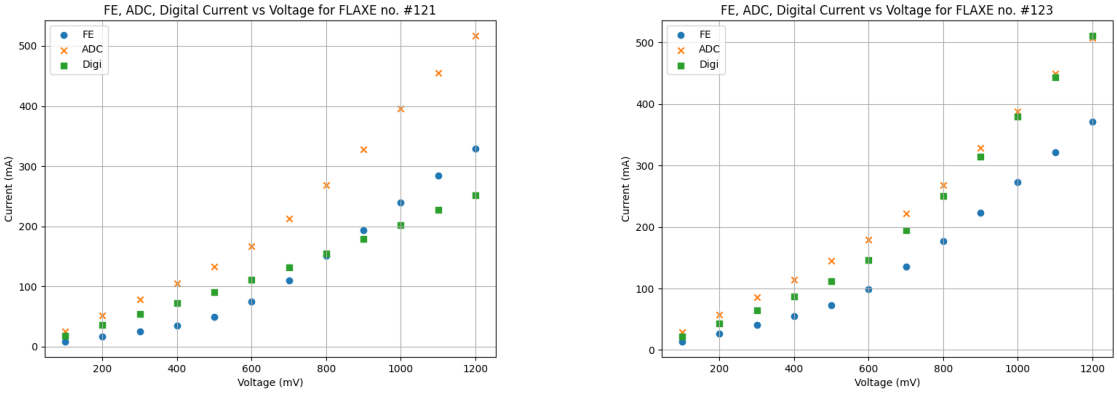

Fig. 3.36. Shortage currents in each of the domains in chip number 121 (left) and number 123 (right) in the function of voltage.

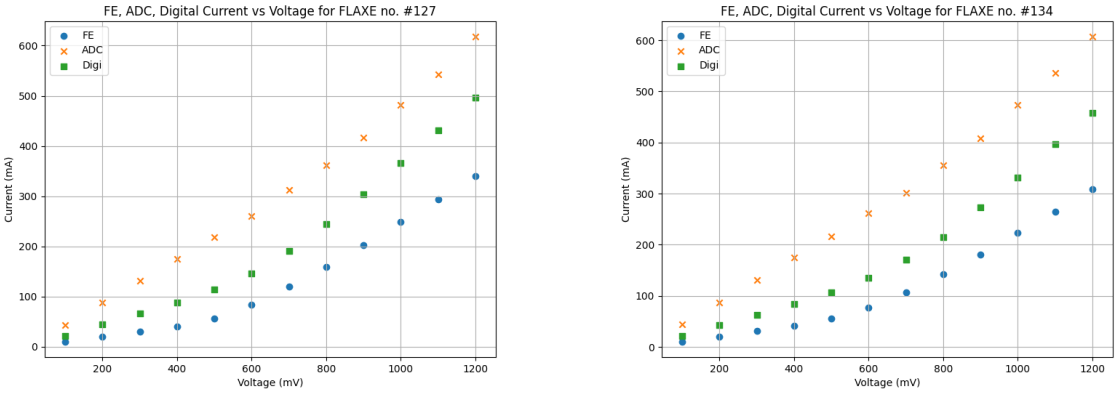

Fig. 3.37. Shortage currents in each of the domains in chip number 127 (left) and number 134 (right) in the function of voltage.

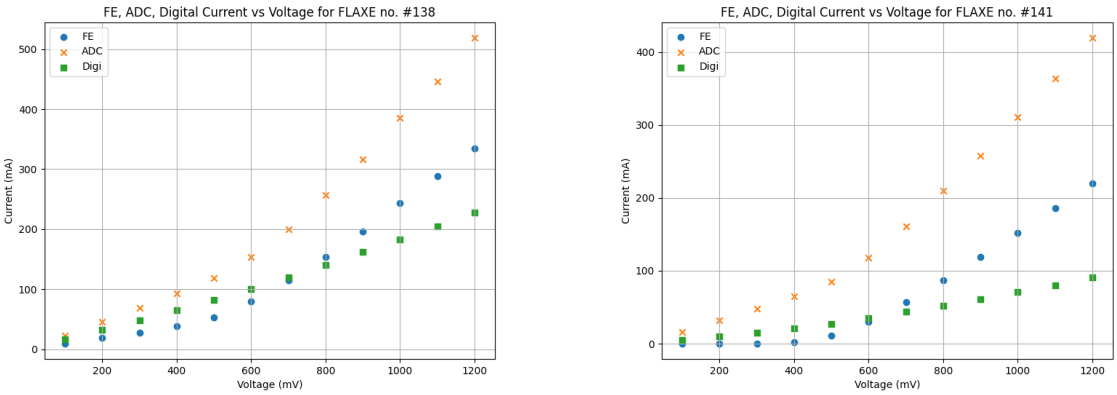

Fig. 3.38. Shortage currents in each of the domains in chip number 138 (left) and number 141 (right) in the function of voltage.

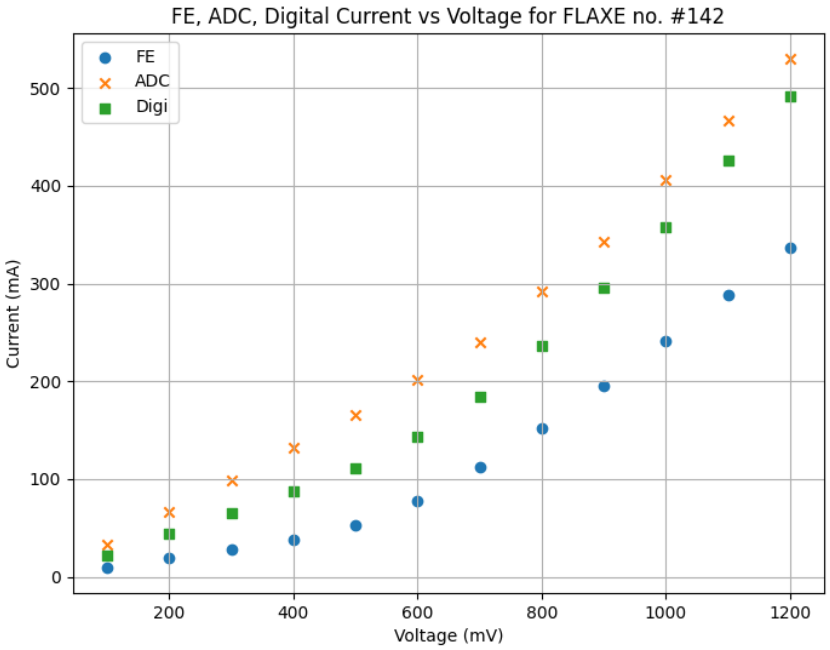

Fig. 3.39. Shortage currents in each of the domains in chip number 142 in the function of voltage.

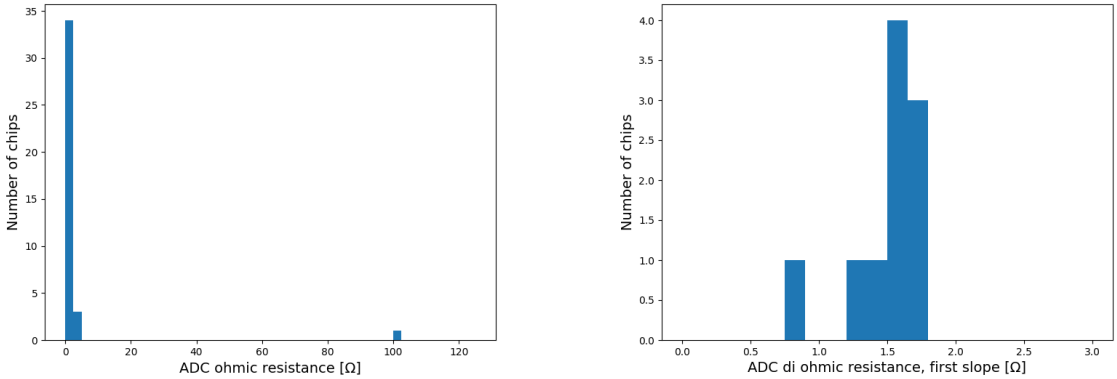

Fig. 3.40. From left to right: histograms of resistances of the shorts in the ADC domain when the characteristic was single ohmic, and when it was di ohmic, for the first slope.

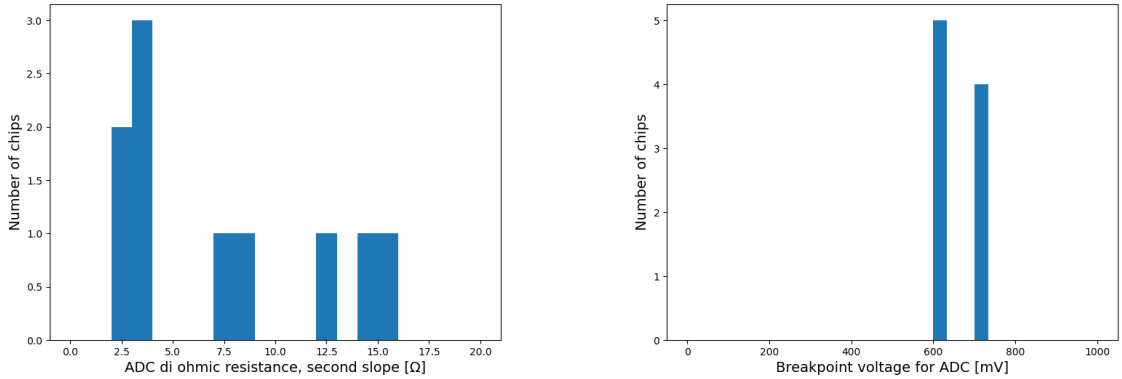

Fig. 3.41. From left to right: histogram of resistances of the shorts in the ADC domain when the characteristic was di ohmic for the second slope, and a histogram of breakpoint voltages.

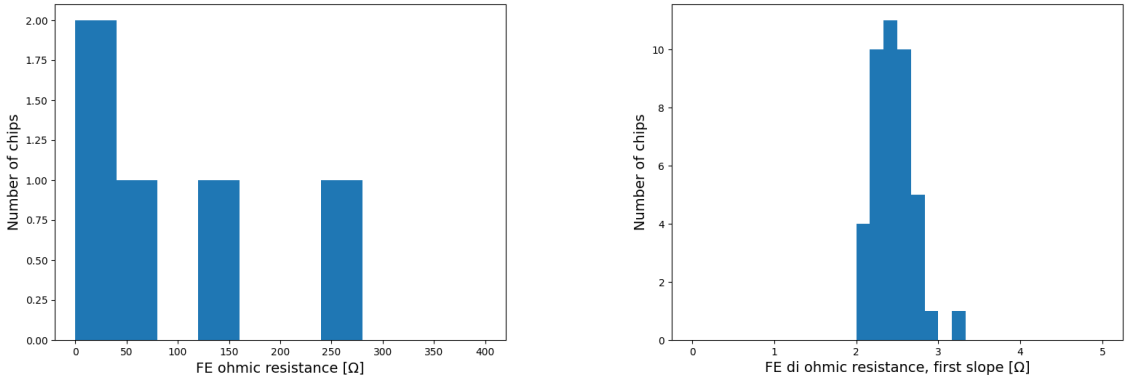

Fig. 3.42. From left to right: histograms of resistances of the shorts in the front-end domain when the characteristic was single ohmic, and when it was di ohmic, for the first slope.

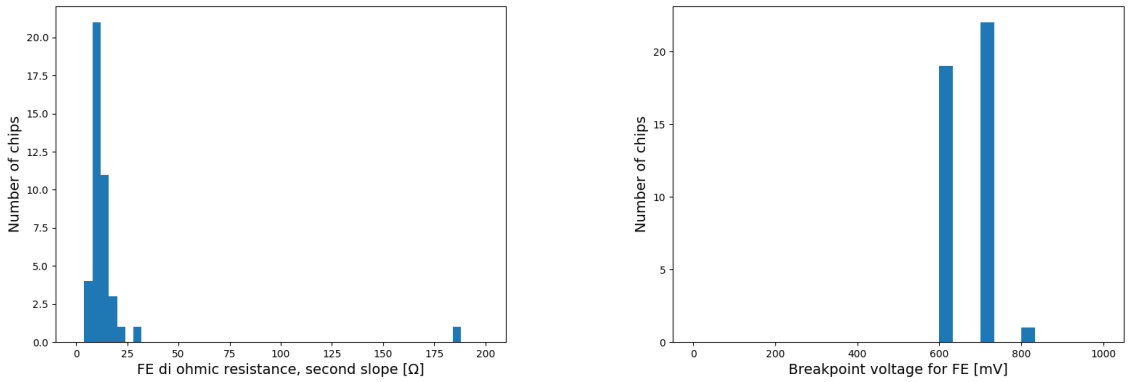

Fig. 3.43. From left to right: histogram of resistances of the shorts in the front-end domain when the characteristic was di ohmic for the second slope, and a histogram of breakpoint voltages.

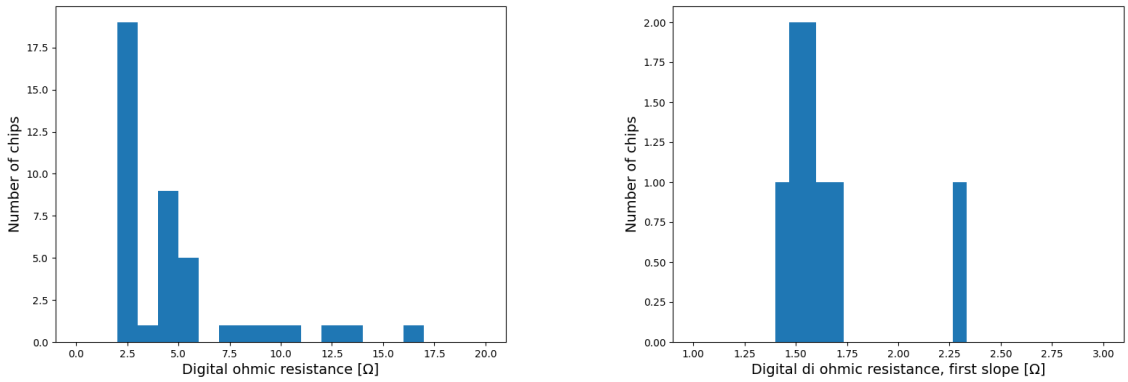

Fig. 3.44. From left to right: histograms of resistances of the shorts in the digital back-end domain when the characteristic was single ohmic, and when it was di ohmic, for the first slope.

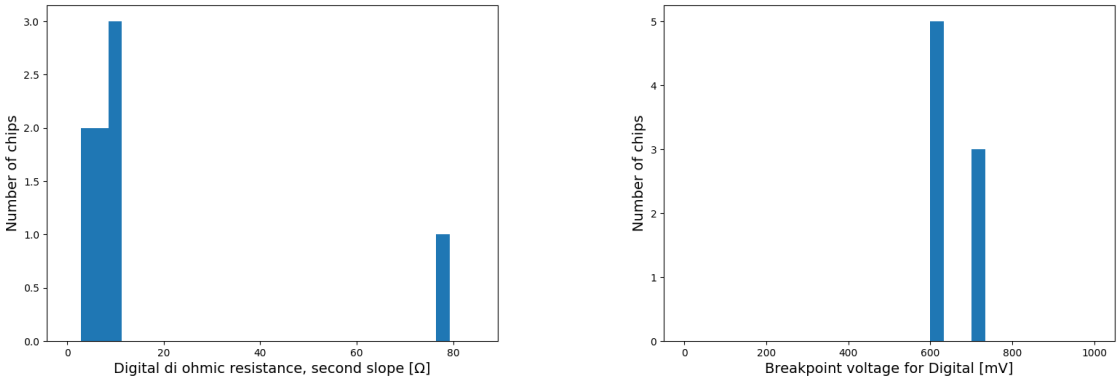

Fig. 3.45. From left to right: histogram of resistances of the shorts in the digital back-end domain when the characteristic was di ohmic for the second slope, and a histogram of breakpoint voltages.

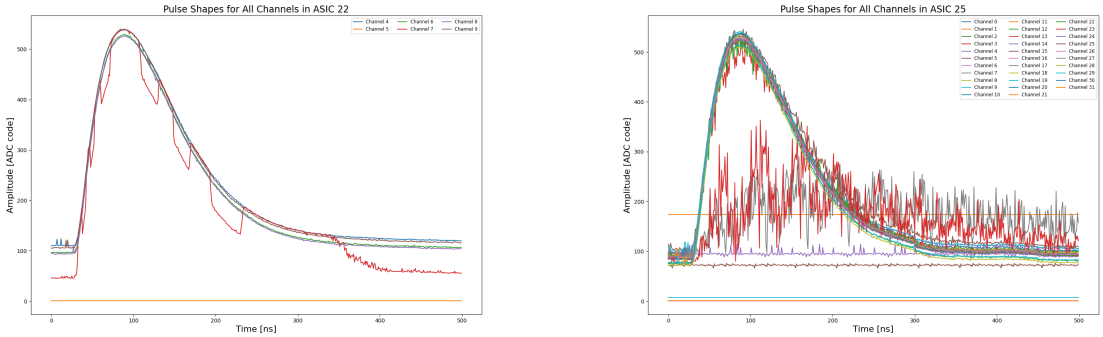

Fig. 3.46. From left to right: pulse shapes for all channels in chips number 22 and 25.

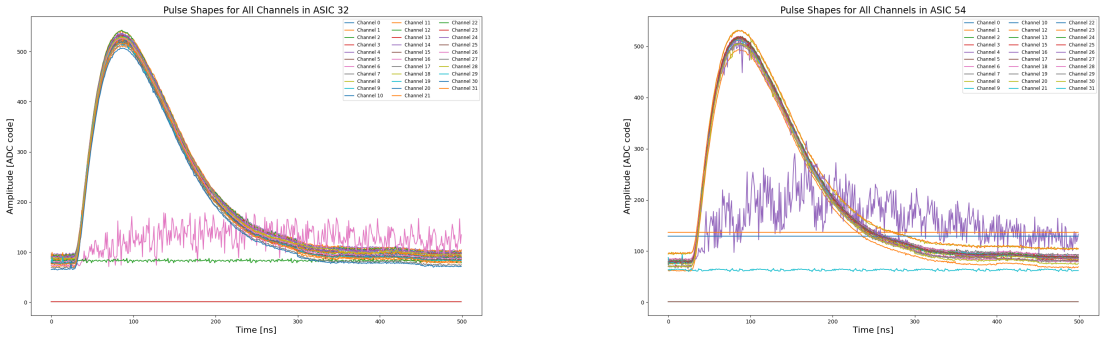

Fig. 3.47. From left to right: pulse shapes for all channels in chips number 32 and 54.

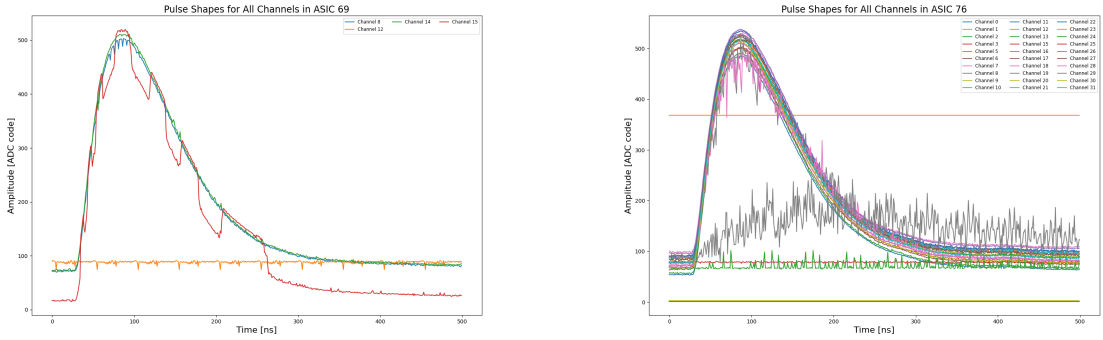

Fig. 3.48. From left to right: pulse shapes for all channels in chips number 69 and 76.

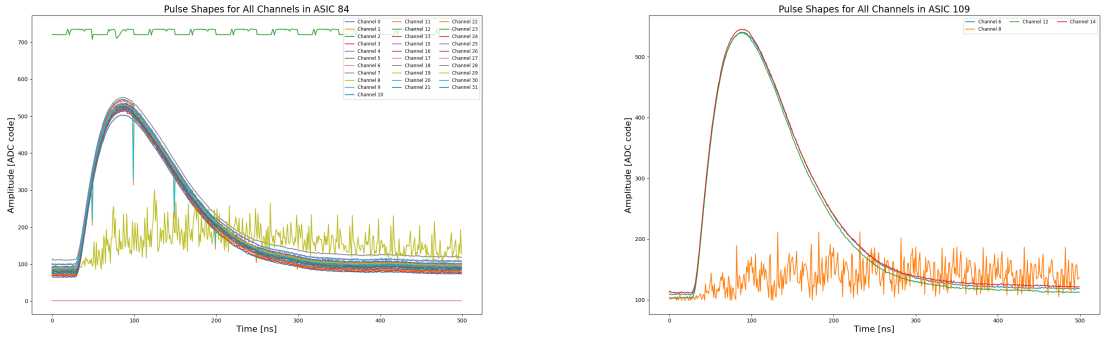

Fig. 3.49. From left to right: pulse shapes for all channels in chips number 84 and 109.

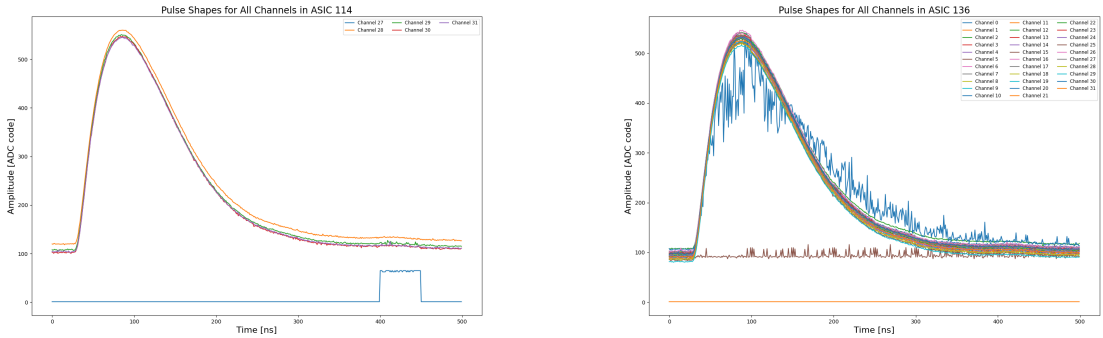

Fig. 3.50. From left to right: pulse shapes for all channels in chips number 114 and 136.

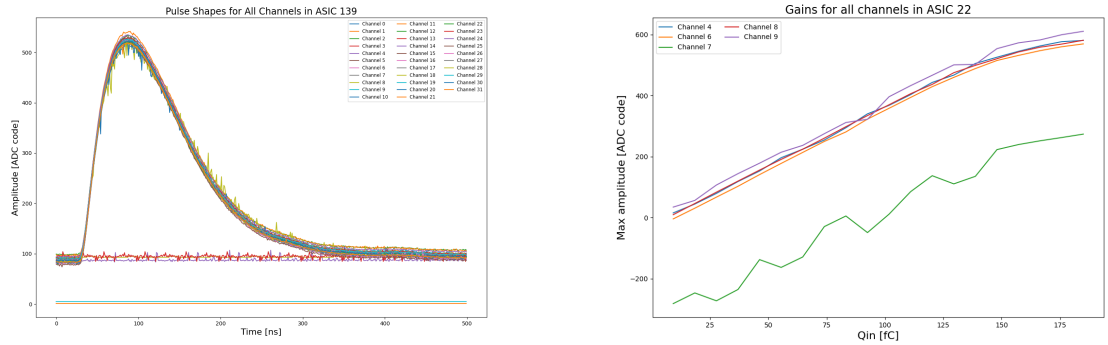

Fig. 3.51. From left to right: pulse shapes for all channels in chips number 139 and gain in all channels in chip number 22.

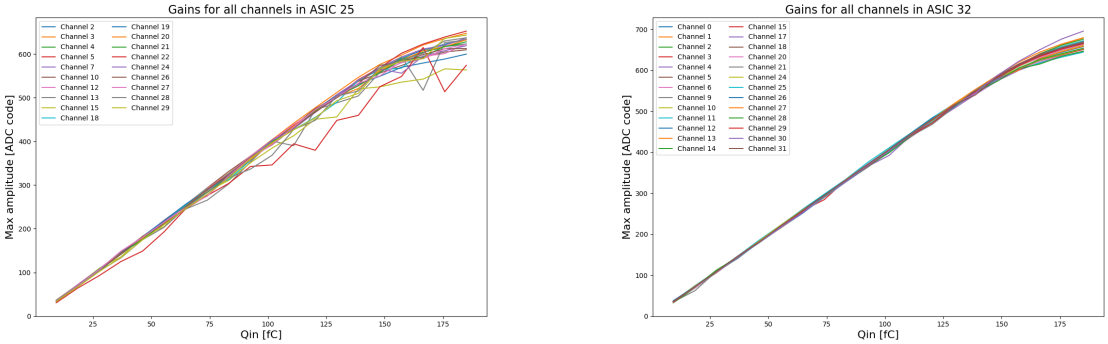

Fig. 3.52. From left to right: gains in all channels for chips number 25 and 32.

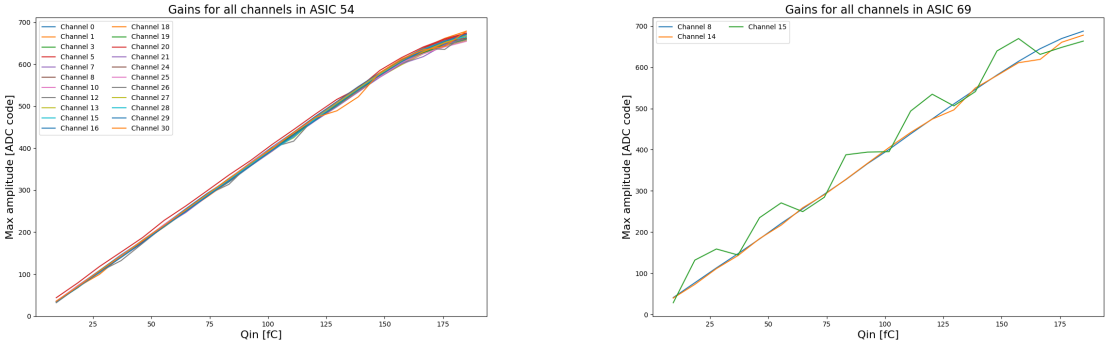

Fig. 3.53. From left to right: gains in all channels for chips number 54 and 69.

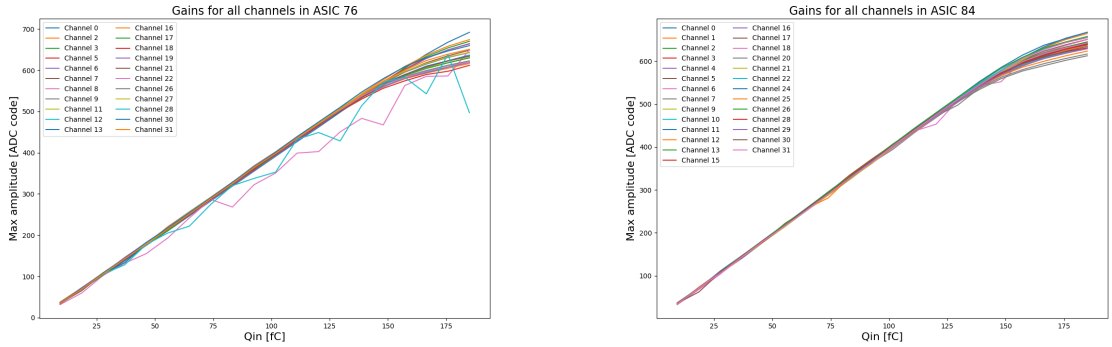

Fig. 3.54. From left to right: gains in all channels for chips number 76 and 84.

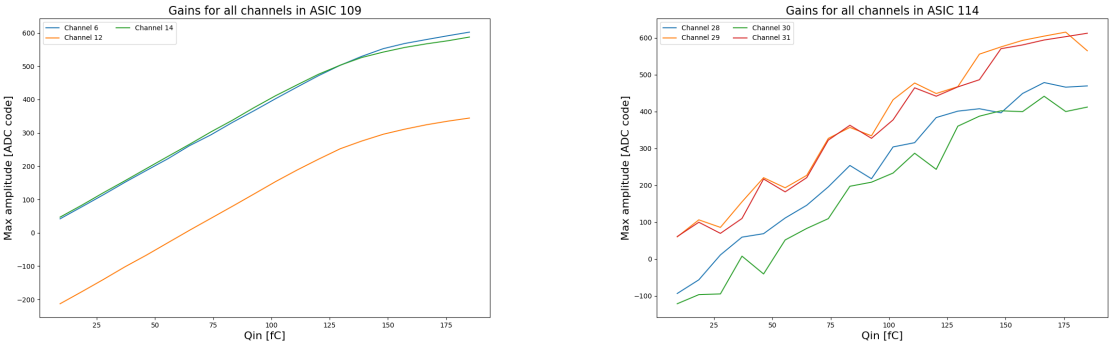

Fig. 3.55. From left to right: gains in all channels for chips number 109 and 114.

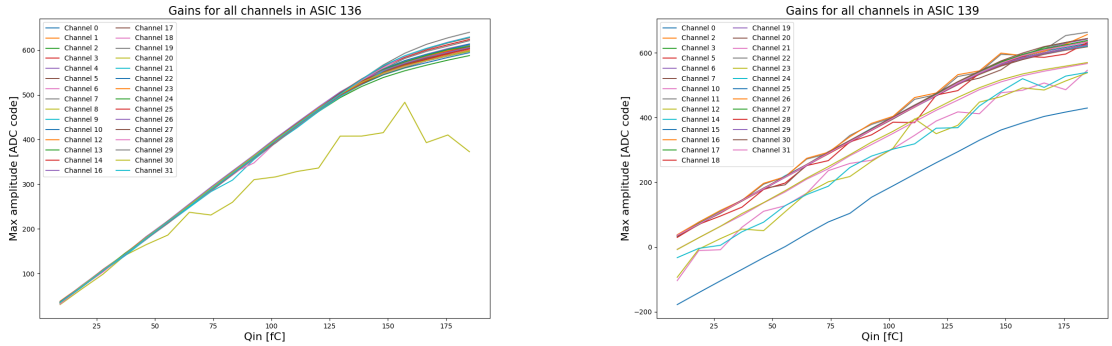

Fig. 3.56. From left to right: gains in all channels for chips number 136 and 139.

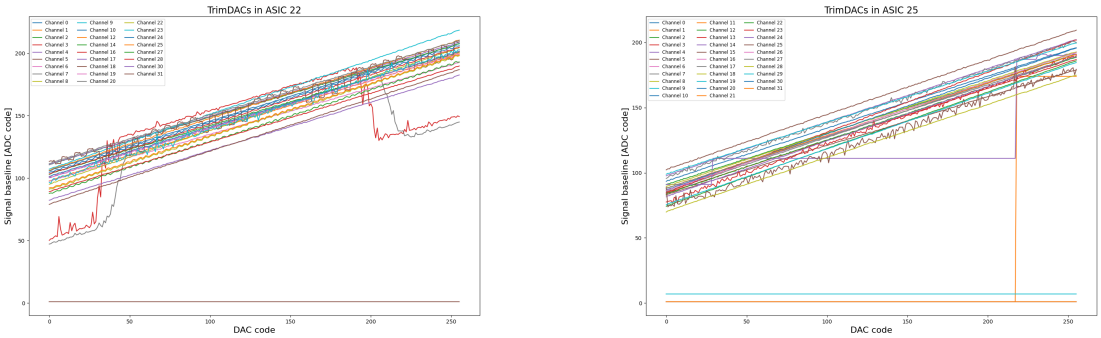

Fig. 3.57. From left to right: trimDAC pedestals for all channels in chips number 22 and 25.

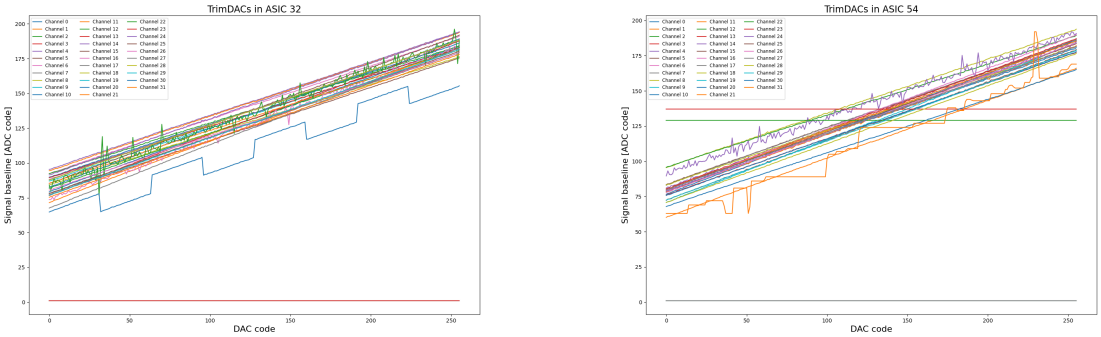

Fig. 3.58. From left to right: trimDAC pedestals for all channels in chips number 32 and 54.

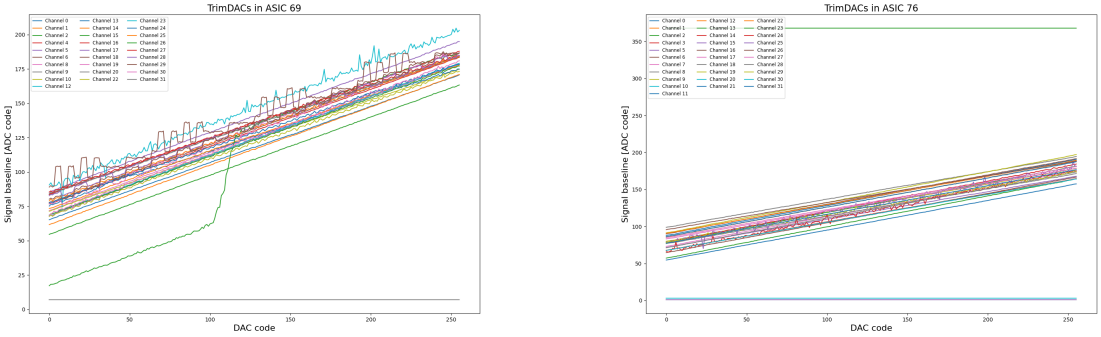

Fig. 3.59. From left to right: trimDAC pedestals for all channels in chips number 69 and 76.

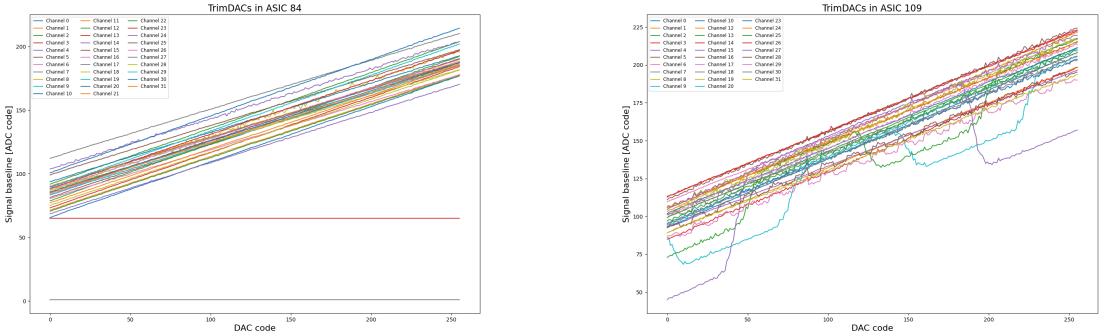

Fig. 3.60. From left to right: trimDAC pedestals for all channels in chips number 84 and 109.

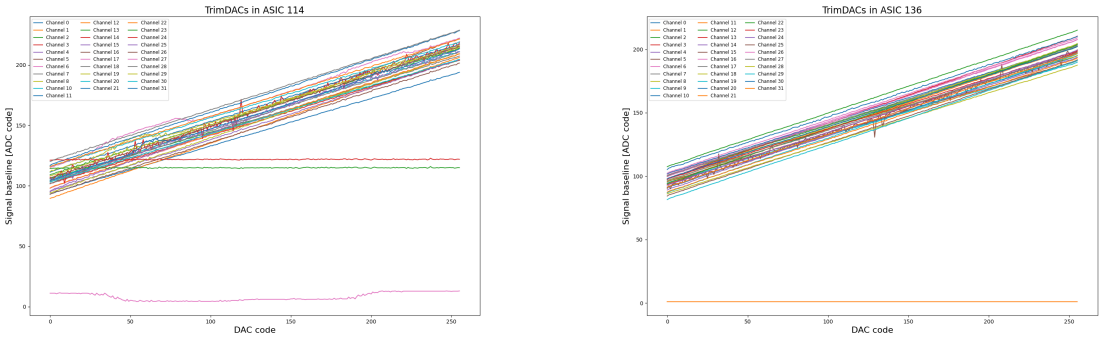

Fig. 3.61. From left to right: trimDAC pedestals for all channels in chips number 114 and 136.

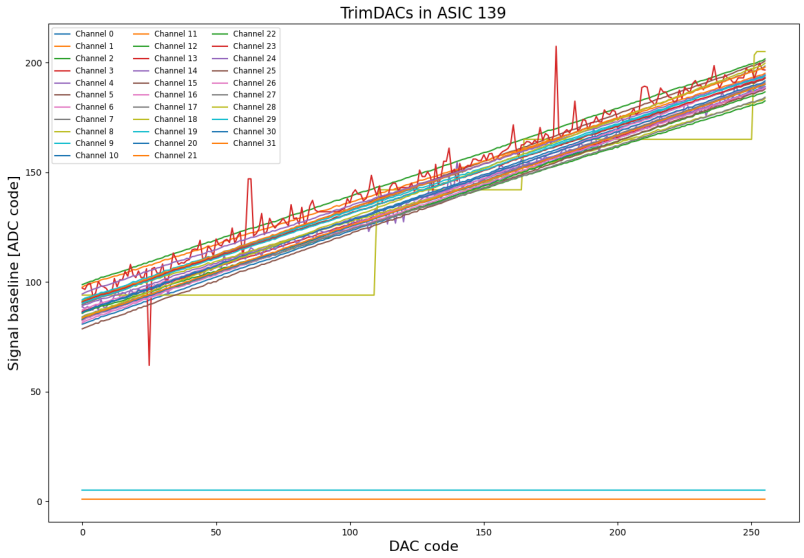

Fig. 3.62. TrimDAC pedestals of all channels in chip number 139.

Bibliography

[1] Helmuth Spieler. *Semiconductor Detector Systems*. OUP Oxford, 2005. ISBN: 0198527845, 9780198527848.

[2] Hermann Kolanoski; Norbert Wermes. *Particle Detectors: Fundamentals and Applications*. Oxford University Press, 2020. ISBN: 9780198858362,0198858361.

[3] Angelo Rivetti. *CMOS: Front-End Electronics for Radiation Sensors*. CRC Press, 2018. ISBN: 9781351832014, 1351832018.

[4] F.N. Hooge. "1/f noise sources". In: *IEEE Transactions on Electron Devices* 41.11 (1994), pp. 1926–1935. DOI: *10.1109/16.333808*.

[5] Noura AlHinai. "Chapter 1 - Introduction to biomedical signal processing and artificial intelligence". In: *Biomedical Signal Processing and Artificial Intelligence in Healthcare*. Ed. by Walid Zgallai. Developments in Biomedical Engineering and Bioelectronics. Academic Press, 2020, pp. 1–28. DOI: *https://doi.org/10.1016/B978-0-12-818946-7.00001-9*.

[6] W. H. Press. "Flicker noises in astronomy and elsewhere." In: *Comments on Astrophysics* 7.4 (Jan. 1978), pp. 103–119.

[7] Robert Szczygiel. "Krummenacher feedback analysis for high-count-rate semiconductor pixel detector readout". In: *Proceedings of the 17th International Conference Mixed Design of Integrated Circuits and Systems - MIXDES 2010*. 2010, pp. 412–415.

[8] Jakub Moroń; Krzysztof Piotr Świętek; Marek Idzik; Mirosław Firlej; Tomasz Andrzej Fiutowski. "FLAXE, a SoC readout ASIC for electromagnetic calorimeter at LUXE experiment". TWEPP 2024 Topical Workshop on Electronics for Particle Physics. 2024.

[9] Xiyuan Tang et al. "Low-Power SAR ADC Design: Overview and Survey of State-of-the-Art Techniques". In: *IEEE Transactions on Circuits and Systems I: Regular Papers* 69.6 (2022), pp. 2249–2262. DOI: *10.1109/TCSI.2022.3166792*.