

AGH UNIVERSITY OF SCIENCE AND TECHNOLOGY

DOCTORAL THESIS

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# Development of monolithic pixel detectors

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# Declaration of Authorship

**Declaration of the author of this dissertation:**

Aware of legal responsibility for making untrue statements I hereby declare that I have written this dissertation myself and all the contents of the dissertation have been obtained by legal means.

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**Declaration of the dissertation Supervisors:**

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# Abstract

Szymon BUGIEL

*Development of monolithic pixel detectors*

The main goal of the presented thesis was the research and development on the capabilities of the Lapis 200 nm SOI (Silicon-On-Insulator) technology in terms of its usage for the design of monolithic detectors. In the SOI structure a thin silicon layer, dedicated for the electronic circuitry implementation, is separated from the handling wafer by an insulator layer. Since for the handling wafer a highly resistive silicon can be used, it may be directly used as a sensing element. The researches were aimed to broaden the existing knowledge of the SOI monolithic detectors behaviour by designing and characterizing different detector prototypes.

The studies began with the measurements of INTPIX6 detector prototypes which are a large area integrating type pixel detectors, suitable for imaging applications, developed by the Japanese group from KEK (The High Energy Accelerator Research Organization). The prototypes fabricated on different handling wafers have been investigated and all have shown very good energy resolution with the equivalent noise charge (ENC) on the level of  $70 e^-$ . They have also proved good imaging capabilities sharply reproducing small  $100 \mu\text{m}$  wide details of the photographed structures. The measurements of INTPIX6 detector have also revealed the main weakness of the SOI technology that is a poor radiation hardness. The selected device has been irradiated up to 60 krad dose, but its performance has started to significantly deteriorate after exceeding 25 krad.

Further research covered not only the measurements of different monolithic detector prototypes, but have been extended also to their design as well as the preparation of the appropriate measurement setup. Several different detectors have been developed by the Cracow group and the two most meaningful are presented in this thesis.

The first one is a general purpose pixel detector designed to get familiar with the technology, test different readout architectures and sensor geometries. Various measurements performed with different radiation sources (from soft X-rays to MIPs (minimum ionizing particles)) allowed for the full characterisation of that device. The studies comprised also the comparison of the standard SOI structure with its modification called the Double SOI. The detailed analysis of gathered data revealed a strong dependence of the readout circuitry performance from the substrate structure and sensor geometry, which provided an important guidance for future designs. This detector also showed a good energy resolution with the ENC of about  $100 e^-$  for the best case, but its main advantage was an excellent spatial resolution reaching  $2.1 \mu\text{m}$ , with the  $30 \mu\text{m} \times 30 \mu\text{m}$  pixels.

The second presented device is CLIPS (CLIC pixel SOI) detector, which is targeting the requirements of the CLIC (Compact Linear Collider) vertex detector. Besides a precise position reconstruction it has to provide also the ToA (Time-of-Arrival) timing information. This device has been designed and is already fabricated, but its measurements have not yet started. Currently, a dedicated readout system is under preparation and the measurements are foreseen in the nearest future. Nevertheless, basing on the simulation results presented in this thesis one can expect the spatial resolution below  $3\ \mu\text{m}$ , obtained with the sensor thinned down to  $150\ \mu\text{m}$  and the ToA accuracy on the order of several nanoseconds.

All of the presented measurement results and their comparison with the simulations provide a broad overview of the Lapis SOI process capabilities in terms of its usage for the monolithic detectors fabrication. The performed studies show a high potential of presented technology for applications in high energy physics experiments, as well as for imaging purposes.

# Abstrakt

Szymon BUGIEL

*Development of monolithic pixel detectors*

Głównym celem przedstawionej pracy były badania możliwości oferowanych przez technologię Lapis 200 nm SOI (*Silicon-On-Insulator*) w kontekście jej wykorzystania do produkcji monolitycznych pikselowych detektorów promieniowania jonizującego. Istotą tego rozwiązania jest wykorzystanie wafla krzemowego, który zawiera cienką warstwę krzemu dedykowaną pod elektronikę, oddzieloną izolatorem od podłoża. Podłoże, które może być wykonane z użyciem wysokorezystywnego krzemu, stanowi zarazem element detekcyjny. Przeprowadzone badania miały na celu poszerzenie obecnej wiedzy na temat zachowania detektorów wyprodukowanych w technologii SOI, poprzez badanie właściwości wyprodukowanych prototypów jak i projektowanie nowych.

Prace badawcze rozpoczęły się od pomiarów detektorów z rodziny INTPIX6. Są to wielkopowierzchniowe detektory pikselowe pracujące w trybie całkującym, odpowiednie do zastosowań w obrazowaniu. Są one rozwijane przez japońską grupę naukowców z KEK (*The High Energy Accelerator Research Organization*) w Tsukubie. Pomiaru kilku prototypów wyprodukowanych z wykorzystaniem różnych podłoży pokazały, że detektory te charakteryzują się wysoką rozdzielczością energetyczną, potwierdzoną przez ekwiwalentny ładunek szumowy (ENC) na poziomie  $70 e^-$ . Wyniki pomiarów wskazują również na ich wysokie predyspozycje do wykorzystania w obrazowaniu. Bez trudu rekonstruowały one detale fotografowanych struktur o rozmiarach rzędu  $100 \mu\text{m}$ . Badania prowadzone z wykorzystaniem tych detektorów pokazały także największą słabość technologii SOI, jaką niewątpliwie jest słaba odporność radiacyjna. Jeden z prototypów napromieniowany został dawką około 60 krad, a jego właściwości zaczęły się znacząco pogarszać już po przekroczeniu 25 krad.

Dalsze badania dotyczyły nie tylko pomiarów kolejnych prototypów detektorów, lecz także ich projektowania oraz przygotowywania dedykowanej infrastruktury pomiarowej. Krakowska grupa, w której skład wchodzi autor niniejszej pracy, przygotowała kilka własnych prototypów, z których dwa najbardziej znaczące w kontekście tematyki tej pracy zostały szczegółowo przedstawione.

Pierwszym z nich jest detektor, którego projekt miał na celu zaznajomienie się z technologią Lapis 200 nm SOI CMOS oraz przetestowanie różnych architektur odczytu detektora oraz geometrii sensorów. Szczegółowe pomiary tego detektora przeprowadzone z wykorzystaniem różnych typów promieniowania jonizującego (począwszy od miękkiego promieniowania X aż po cząstki minimalnie jonizujące) pozwoliły na jego pełną charakteryzację. Przeprowadzone

badania dotyczyły również porównania działania prototypów wyprodukowanych na różnych podłożach, czyli standardowej struktury SOI oraz jej modyfikacji zwanej *Double SOI*. Analiza zebranych danych wskazała na silną zależność pomiędzy zachowaniem elektroniki odczytu, a użytym podłożem, jak i geometrią sensora. Zebrane informacje pozwoliły na wypracowanie szeregu rozwiązań mających na celu zminimalizowanie negatywnego wpływu sensora na elektronikę. Wyniki pomiarów wskazują, że zaproponowany detektor cechuje się rozdzielczością energetyczną wyrażoną ekwiwalentnym ładunkiem szumowym na poziomie  $100 e^-$ . Jego szczególną zaletą jest znakomita rozdzielczość przestrzenna, sięgająca  $2.1 \mu\text{m}$  przy rozmiarach piksela  $30 \mu\text{m} \times 30 \mu\text{m}$ .

Kolejnym z przedstawionych układów jest detektor pikselowy o nazwie CLIPS (CLIC pixel SOI), który zaprojektowany został z myślą o potencjalnym wykorzystaniu w układzie detekcji wierzchołka w przyszłym zderzaczu liniowym CLIC. W tym wypadku wymagane było przygotowanie detektora potrafiącego nie tylko precyzyjnie wyznaczyć pozycję przechodzącej cząstki, ale także czas jej przybycia. Detektor został już wyprodukowany i obecnie przygotowywany jest dedykowany układ pomiarowy, który pozwoli na rozpoczęcie pomiarów. Niemniej jednak, wyniki symulacji wskazują na to, że można oczekiwać rozdzielczości przestrzennej poniżej  $3 \mu\text{m}$  i dokładności pomiaru czasu rzędu pojedynczych nanosekund, uwzględniając pocienienie detektora do  $150 \mu\text{m}$ .

Wyniki pomiarów oraz symulacji prezentowanych w niniejszej pracy pozwoliły uzyskać szeroki wgląd w potencjał technologii SOI w kontekście zastosowania jej do produkcji monolitycznych detektorów pikselowych. Przeprowadzone badania wskazują jednoznacznie na wysoki potencjał użytej technologii zarówno dla eksperymentów fizyki wysokich energii, jak i dla zastosowań w obrazowaniu.



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# List of Abbreviations

<b>ASIC</b>	<b>A</b> pplication- <b>S</b> pecific <b>I</b> ntegrated <b>C</b> ircuit
<b>ADC</b>	<b>A</b> nalog to <b>D</b> igital <b>C</b> onverter
<b>ADU</b>	<b>A</b> nalog to <b>D</b> igital converter <b>U</b> nits
<b>BNL</b>	<b>B</b> rookhaven <b>N</b> ational <b>L</b> aboratory
<b>BNW</b>	<b>B</b> uried <b>N</b> - <b>W</b> ell
<b>BPW</b>	<b>B</b> uried <b>P</b> - <b>W</b> ell
<b>BOX</b>	<b>B</b> uried <b>O</b> Xide
<b>BSOI</b>	<b>B</b> ond <b>S</b> ilicon <b>O</b> n <b>I</b> nsulator
<b>CCD</b>	<b>C</b> harge <b>C</b> oupled <b>D</b> evice
<b>CERN</b>	<b>T</b> he <b>E</b> uropean <b>O</b> rganization for <b>N</b> uclear <b>R</b> esearch
<b>CDS</b>	<b>C</b> orrelated <b>D</b> ouble <b>S</b> ampling
<b>CMFB</b>	<b>C</b> ommon <b>M</b> ode <b>F</b> eed <b>B</b> ack
<b>CMOS</b>	<b>C</b> omplementary <b>M</b> etal- <b>O</b> xide <b>S</b> emiconductor
<b>CLIC</b>	<b>C</b> ompact <b>L</b> inear <b>C</b> ollider
<b>CLIPS</b>	<b>CLIC</b> <b>P</b> ixel <b>S</b> OI
<b>CPA</b>	<b>C</b> harge-sensitive <b>P</b> re- <b>A</b> mplifier
<b>CZ(n)</b>	<b>C</b> zochralski type <b>n</b>
<b>DAC</b>	<b>D</b> igital to <b>A</b> nalog <b>C</b> onverter
<b>DAQ</b>	<b>D</b> ata <b>A</b> c <b>Q</b> uisition
<b>DC</b>	<b>D</b> irect <b>C</b> urrent
<b>DRC</b>	<b>D</b> esign <b>R</b> ule <b>C</b> heck
<b>DSOI</b>	<b>D</b> ouble <b>S</b> OI
<b>DUT</b>	<b>D</b> evice <b>U</b> nder <b>T</b> est
<b>ENC</b>	<b>E</b> quivalent <b>N</b> oise <b>C</b> harge
<b>ELO</b>	<b>E</b> pitaxial <b>L</b> ayer <b>O</b> vergrowth
<b>ELT</b>	<b>E</b> nclosed <b>L</b> ayout <b>T</b> ransistor
<b>ELTRAN</b>	<b>E</b> pitaxial <b>L</b> ayer <b>T</b> RANsfer
<b>FC</b>	<b>F</b> olded <b>C</b> ascode
<b>FD-SOI</b>	<b>F</b> ully- <b>D</b> epleted <b>S</b> OI
<b>FPGA</b>	<b>F</b> ield- <b>P</b> rogrammable <b>G</b> ate <b>A</b> rray
<b>FZ(n)</b>	<b>F</b> loating <b>Z</b> one type <b>n</b>
<b>FZ(p)</b>	<b>F</b> loating <b>Z</b> one type <b>p</b>
<b>GUI</b>	<b>G</b> raphical <b>U</b> ser <b>I</b> nterface
<b>HEP</b>	<b>H</b> igh <b>E</b> nergy <b>P</b> hysics
<b>HL-LHC</b>	<b>H</b> igh- <b>L</b> uminosity <b>L</b> arge <b>H</b> adron <b>C</b> ollider

<b>HR-CMOS</b>	<b>H</b> igh- <b>R</b> esistivity <b>C</b> MOS
<b>HV</b>	<b>H</b> igh <b>V</b> oltage
<b>HV-CMOS</b>	<b>H</b> igh- <b>V</b> oltage <b>C</b> MOS
<b>I/O</b>	<b>I</b> nput/ <b>O</b> utput
<b>ILC</b>	<b>I</b> nternational <b>L</b> inear <b>C</b> ollider
<b>INTPIX</b>	<b>I</b> NTegration type <b>P</b> IXels
<b>KEK</b>	The <b>H</b> igh <b>E</b> nergy <b>A</b> ccelerator <b>R</b> esearch <b>O</b> rganization
<b>LHC</b>	<b>L</b> arge <b>H</b> adron <b>C</b> ollider
<b>LDD</b>	<b>L</b> ightly <b>D</b> opped <b>D</b> rain
<b>MIP</b>	<b>M</b> inimum <b>I</b> onizing <b>P</b> article
<b>MIP</b>	<b>M</b> etal <b>I</b> nsulator <b>M</b> etal
<b>MPV</b>	<b>M</b> ost <b>P</b> robable <b>V</b> alue
<b>nMOS</b>	<b>n</b> -channel <b>M</b> OSFET
<b>PD-SOI</b>	<b>P</b> artially- <b>D</b> epleted <b>S</b> OI
<b>PCB</b>	<b>P</b> rinted <b>C</b> ircuit <b>B</b> oard
<b>pMOS</b>	<b>p</b> -channel <b>M</b> OSFET
<b>R&amp;D</b>	<b>R</b> esearch and <b>D</b> evelopment
<b>RFC</b>	<b>R</b> ecycling <b>F</b> olded <b>C</b> ascode
<b>RHIC</b>	<b>R</b> elativistic <b>H</b> eavy <b>I</b> on <b>C</b> ollider
<b>RMS</b>	<b>R</b> oot <b>M</b> ean <b>S</b> quare
<b>ROI</b>	<b>R</b> egion <b>O</b> f <b>I</b> nterest
<b>SEABAS</b>	<b>S</b> OI <b>E</b> vAluation <b>B</b> oArd with <b>S</b> iTep
<b>SEE</b>	<b>S</b> ingle <b>E</b> vent <b>E</b> ffects
<b>SEU</b>	<b>S</b> ingle <b>E</b> vent <b>U</b> pset
<b>SET</b>	<b>S</b> ingle <b>E</b> vent <b>T</b> ransient
<b>SF</b>	<b>S</b> ource <b>F</b> ollower
<b>SIMOX</b>	<b>S</b> eparation by <b>I</b> mplementation of <b>O</b> Xygen
<b>SNR</b>	<b>S</b> ignal to <b>N</b> oise <b>R</b> atio
<b>SOI</b>	<b>S</b> ilicon- <b>O</b> n- <b>I</b> nsulator
<b>SOS</b>	<b>S</b> ilicon- <b>O</b> n- <b>S</b> apphire
<b>TCP/IP</b>	<b>T</b> ransmission <b>C</b> ontrol <b>P</b> rotocol/ <b>I</b> nternet <b>P</b> rotocol
<b>TID</b>	<b>T</b> otal <b>I</b> onizing <b>D</b> ose
<b>ToA</b>	<b>T</b> ime of <b>A</b> rrival
<b>UDP</b>	<b>U</b> ser <b>D</b> atagram <b>P</b> rotocol
<b>VHDCI</b>	<b>V</b> ery- <b>H</b> igh- <b>D</b> ensity <b>C</b> able <b>I</b> nterconnect
<b>VLSI</b>	<b>V</b> ery <b>L</b> arge <b>S</b> cale of <b>I</b> ntegration



# Introduction

The growing demands on the performance of the detection systems for the high energy physics experiments, medical imaging, as well as for commercial applications, force the continuous development of the detector technologies. This allows to overcome the existing limitations (in example on detector segmentation) and ensures the constant technology upgrading. In terms of the tracking detectors, presently the standard solution are hybrid pixels detectors that are widely used in particle physics experiments. In this approach the readout electronics is fabricated independently from the sensor and those two components are connected using the bump-bonding technique. Unfortunately, such solution introduces a lot of “non-active” material into the whole detection system. The existence of that additional material highly increases the probability of Coulomb scattering of the measured particles, which directly deteriorates the measurement precision. Moreover, physical dimensions of the bumps are limiting the granularity of the device. For these reasons, the requirements for the future detection systems have recently started to exceed the capabilities of the hybrid detectors.

Fortunately, there is an alternative solution to the hybrid devices, namely the monolithic pixel detectors. For this type of devices the readout electronics is implemented on the same wafer as the sensing matrix. This solution allows to overcome the limitations of the hybrid detectors, but its implementation is technologically challenging. There are several different approaches for the monolithic detectors fabrication, each having its own strong and weak points that have to be taken into account when considering its application.

This thesis is fully devoted to the development of the monolithic detectors utilizing the Silicon-On-Insulator (SOI) technology. On the top of the SOI structure there is a thin silicon layer dedicated for the electronics implementation. This layer is electrically separated from the handling wafer by an insulator layer, which allows to use the existing silicon substrate as a radiation sensitive element. The goal of this thesis was the research and development on the monolithic pixel detectors fabricated in the Lapis 200 nm SOI CMOS technology. The work was aimed to verify its capabilities in terms of the usage for ionizing radiation detection, mainly for the future high energy experiments. Thus, the researches were aimed to estimate noise performance of different SOI detector prototypes, verify their imaging potential and the spatial resolution, as well as test their radiation hardness. For that purpose, not only a precise characterisation of several detectors was needed, but also a direct comparison of their operation with the simulations.

The core of this thesis is comprised of two chapters providing the essential theoretical background followed by three chapters devoted to different detector prototypes characterisation. The whole work is summarized in the final part with conclusion. Chapter 1 begins with a short historical introduction into the topic of semiconductor radiation detectors. After that a basic

working principles of semiconductor sensors are presented. The next chapter is fully devoted to the description of the Lapis 200 nm SOI CMOS technology. It describes different methods of SOI wafers production and shows all main features of the SOI structure. In chapter 3 the characterization of the first detector prototype is presented. The studies have been performed with the INTPIX6 – a large area, integrating type pixel detector, suitable for imaging applications, which was developed by the Japanese group from KEK. Its measurements were focused on the estimation of the energy resolution as well as its imaging capabilities.

Beside the INTPIX6, there are two another detectors presented in this thesis. These were fully developed by the Cracow group and author of this thesis was one of theirs main designer. First device is introduced in chapter 4. It is a general purpose detector aimed for tests of different readout architectures as well as different sensor geometries. It has been precisely characterized thanks to the complete set of lab measurements and tests with the particle beam.

The second prototype is the CLIPS detector presented in chapter 5. It was designed to fulfil the requirements of the CLIC vertex detector. Its measurements have not yet been performed, but a detailed description of its architecture together with the simulation results are presented.

The conclusions summarize the obtained results remaining the most meaningful outcomes and also give an overview on future works being a continuation of studies presented in this thesis.

## Chapter 1

# Basics of radiation detectors

### 1.1 Historical outline of semiconductor radiation sensors

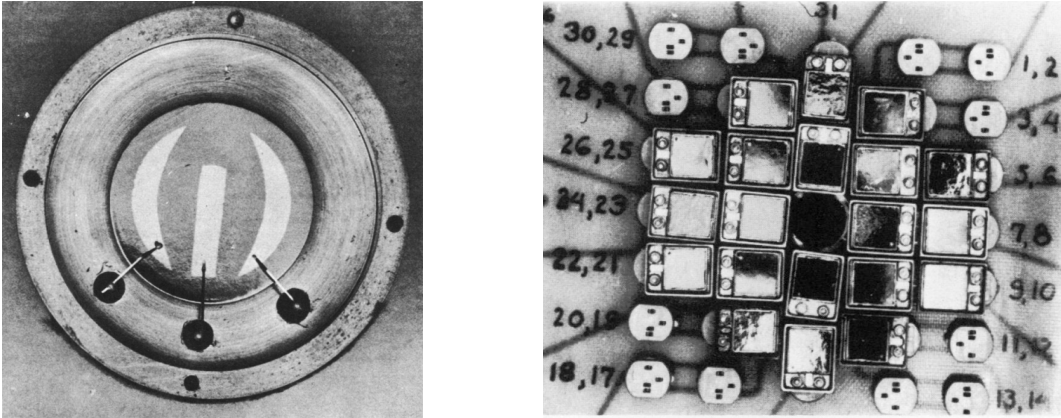
The history of semiconductor nuclear detectors has began in 1943. At that time it was already known that “some kind of solids” namely crystals are sensitive to the light due to the photoelectric effect. P.J. van Heerden concluded that they could also be sensitive to the ionizing particles ( $\alpha$ ,  $\beta$  and  $\gamma$ ). He performed an experiment in which 4 mm thick AgCl crystal with silver contacts was cooled down by liquid air. The high voltage was applied and the *sensor* was connected to two stage tube amplifier. Finally, the signal induced in crystal (or semiconductor using contemporary language) by ionising particles was observed on cathode ray oscillograph. The obtained dataset was precise enough to calculate the energy needed to generate an electron–hole pair in AgCl to be 7.6 eV and the bandgap energy of 3.2 eV [1], which is in good agreement with later measurements.

Shortly after that, in the early 1950s, the germanium detectors were developed in Bell Telephone Laboratories by Kenneth McKay. Germanium was chosen because at that time it was already possible to produce large single crystals of known properties and because of its similarities to diamond. This time it was already a *pn*-junction created by a germanium rod, half *n*-type and half *p*-type, reversely biased and exposed to  $\alpha$  particles. With this setup an energy loss of  $\alpha$  particle per electron-hole pair creation of 3.04 eV was measured [2].

Few years later, when the silicon monocrystals became available, different groups have started the development of the silicon nuclear detectors. Two approaches were investigated in parallel, devices based on evaporated gold surface barriers and a *pn*-junction [3]. At that time the silicon devices started to be very interesting for nuclear physics experiments. In comparison to the available gaseous detectors they had offered extremely short response times, convenient physical dimensions, insensitivity to magnetic fields together with excellent energy resolution (due to around ten times lower electron-hole pair creation energy).

The growing interest and continues improvement of technology resulted in a rapid development of the silicon detectors. Already in year 1961, the first segmented detector was fabricated by Dearnaley [4]. It contained three separate surface barrier counters evaporated on a single silicon wafer (as showin in Fig. 1.1A).

At the same time there was a demand for large area detectors able to provide not only the energy but also position information. An example of such system built for heavy ion Coulomb excitation, shown in Fig. 1.1B, worked at Yale University and was constructed by



(A) Triple semiconductor surface barrier detector. (B) Large area parallel semiconductor mosaic detector.

FIGURE 1.1: Examples of pioneering silicon detectors from the early 1960s (pictures from [4]).

J. S. Greenberg [4]. It was a mosaic of 32 individual,  $1 \text{ cm}^2$  large, silicon detectors arranged in an array with a dedicated readout for each channel. Therefore, it can be treated as a precursor of today's pixel detectors.

Next, in 1969, the concept of a single detector providing 2D spatial information had been introduced, the Charge Coupled Device (CCD) proposed by W. Boyle and G. Smith [5]. This invention had a huge impact on digital imaging technology. CCD's had dominated the digital camera market and were, and still are, widely used in medicine and scientific applications, because they could provide an excellent signal to noise ratio together with the large area coverage. The CCD invention was found to be so important that in 2009 Boyle and Smith were awarded the Nobel Prize for Physics. In spite of that, CCD's at that time were not suitable for particle physics experiments because of too small signal from minimum ionizing particles (due to very shallow depletion).

In the early 1970's few groups around the world had been developing the strip sensors which were much more suitable for particle physics experiments. For example, in 1971 a group from Karlsruhe reported [6] the strip silicon detector providing angular information together with energy information. In their device one side of the sensor was segmented into 5 or 12 strips by using a thin-wire mask during the gold evaporation, whereas the second side was fully covered with aluminium. In contrast to the today's solutions the segmented side provided only the information about the position while the energy was measured by a common channel connected to the aluminium electrode.

The first usage of silicon detector as a tracking device was in 1981 dictated by the willingness of observation of the short living mesons containing charm quark. Their predicted live-times were of an order of  $0.1 \text{ ps}$  (corresponding to decay lengths  $c\tau \sim 30 \mu\text{m}$ ), so the fast and precise devices were needed. Therefore, NA11 and NA32 experiments at CERN have installed planes of silicon strip detectors located close to the interaction point, for precise tracking and vertex reconstruction. It was also a time when silicon detectors have started to gain profits from the planar technology development for the integrated circuits production. By using the planar

process it became possible to design much more fine and precise sensor geometries.

The successful operation of the NA11 and NA32 experiments proved the high capabilities of silicon sensors for the precise track and vertex reconstruction in a high particle multiplicity environment, therefore they started to dominate all the high energy physics (HEP) experiments. But with the constantly increasing multiplicities the problem with proper signal assignment from strips had grown. Thus, there was a high demand for a two-dimensional detector [7]. Finally in year 1983, group from the Rutherford Laboratory reported the successful usage of the CCD for ionizing particles tracking [8] with a 12.7 mm by 8.5 mm large matrix of 576 times 385 pixels with a pitch of 22  $\mu\text{m}$ . The depletion thickness was only 8  $\mu\text{m}$ , but the detection was still possible thanks to limiting the dark current by cooling the sensor down to 120 K. Even with the signal of only 1300 electrons the device showed very good performance of a pointing resolution of 4.3  $\mu\text{m}$  in X direction and 6.1  $\mu\text{m}$  in Y, with the efficiency on the level of 98 %. This kind of the detectors were later used in NA32 experiment in the vertex telescope.

In the next years the progress of the technology allowed for the continuous development of the detectors with more compact readouts thanks to the VLSI (Very Large Scale of Integration) electronics, but the real milestone was made in 1990's, when hybrid pixel detectors appeared in the HEP experiments [9]. Similar to the CCD's they allowed for two dimensional tracking, but in addition they overcome the main limitation of CCD's which was the long readout time. From that time pixel detectors have become almost obligatory part of the innermost tracking system and started to gradually replace strip detectors [1, 10].

Together with the hybridization concept another approach towards pixelization has been introduced – monolithic detectors. It was an idea of integrating the readout electronics and the detector on the same wafer. Since both of them are made of silicon it seems to be a natural solution, but there are few technical difficulties that have to be overcome. To allow a large depletion depths of a sensor a high resistivity wafers are needed, which are not a typical solution for the electronics production. First successful attempts were performed already in early 1990's [11]. Later on, this kind of detectors have started to gradually supersede the CCD's from the digital cameras market and currently they are the most widely used solution for a visible light imaging.

Despite of their success in commercial market, currently operating particle physics experiments use almost only hybrid pixel detectors, which is mainly caused by their high radiation hardness. Only recently, in year 2014, STAR experiment at the Relativistic Heavy Ion Collider (RHIC) at the Brookhaven National Laboratory (BNL) has installed a first large-scale tracking device based on monolithic detectors [12]. For the future, post-LHC experiments, many monolithic solutions are being considered, since it seems to be the only solution allowing for a further material budget reduction while the technology starts to be mature enough to deal with the high radiation.

## 1.2 Basic principles of semiconductor sensors

Silicon is the second most abundant element in the Earth's crust (about 28 % by mass) after oxygen (about 47 %), but it very rarely occurs in the pure form. It mainly exists in various forms of silica (silicon dioxide) or silicates. Silicate minerals are the main rock-forming materials that make up around 90 % of the Earth's crust.

In case of pure silicon there are two allotropic forms that exist at room temperature, amorphous and crystalline. Amorphous silicon appears as a brown powder while crystalline one has a greyish, metallic color. For the first time the crystalline silicon was prepared by Henri Deville in 1854, but large monocrystals became widely available after year 1915 when Czochralski process was introduced.

The physical properties of silicon qualify it as a semiconductor with an energy gap between the valence and conduction bands of about 1.12 eV at the room temperature. In its crystal form it has a face-centred cubic lattice structure (the same as diamond), with a lattice constant of 5.34 Å.

### 1.2.1 *pn*-junction as a sensor

Silicon wafers are often used as radiation sensors, but even in an intrinsic, pure crystal structure, there are about  $10^{10}$  free charge carriers per cubic centimetre [13], whereas the number of electrons induced by an ionising particle is in the order of  $10^4$ . It is obvious that in such conditions the signal from the passing particle would be lost. Therefore, there is a need for the mechanism allowing a significant reduction of free charges. In principle there are two solutions to achieve that. First, it can be done by cooling down the sensor to reduce the probability of thermal excitation of electron to the conduction band. But since a cryogenic temperatures are needed it is not a convenient method especially for a large scale applications. Therefore the second solution, which is based on a *pn*-junction, is much more popular.

To control the conductivity of a semiconductor a small fraction of impurities can be introduced into a silicon lattice (with typical concentrations between  $10^{12}$  and  $10^{19}$  cm<sup>-3</sup>). This process is called doping and depending on what kind of the additional element is used, the silicon can be *n* or *p* doped. In *n*-type silicon the introduced impurities comes from V-th group of the periodic table (most commonly it is Phosphorus) providing extra electrons to the lattice. Therefore, they are often termed as donors. The excessive electrons are not tightly bound with the atom so they form an additional energy band located close to the conduction band. The energy gap differs for different doping atoms, but usually the difference is so small that these spare electrons have enough thermal energy to easily transfer into conduction band.

On the other hand, when the impurities come from III-rd group (mainly Boron) the deficiency of electrons appears. This kind of dopant is therefore often called as acceptor. In terms of a band theory an additional energy level is introduced just above the valence band, close enough for thermal excitations of valance electrons. The configurations of the valence electrons in the pure and doped silicon are schematically shown in Fig. 1.2.

At the first glance, introducing a doping into the silicon only affects its conductivity (resistivity). But its real potential reveals after connecting a *p*-type and *n*-type regions, forming

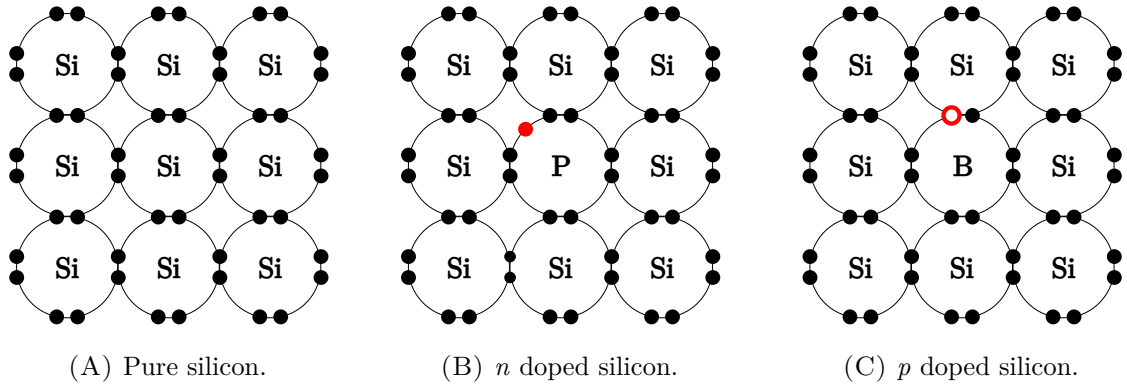


FIGURE 1.2: Electronic configurations of the valence electrons in pure and doped silicon lattice. Excessive and missing electrons are marked with filled and empty red circles respectively.

a  $pn$ -junction. In such a case an excess of the electrons from the  $n$  doped side can freely diffuse into a  $p$  doped side and fill out the holes. After moving out of the  $n$ -type side electrons are leaving there uncovered positively charged ions. Similarly on the  $p$ -type side, the additional electrons occupying the holes generate an uncompensated negative space charge. The existence of this space charge on both sides results in the build-up of an electric field across the junction, which acts against the carriers exchange. At some point an equilibrium state is reached when the electric field is large enough to stop further migration. Therefore, in the steady state three regions can be distinguished:  $p$  doped side,  $n$  doped side and between them a region without free charge carriers – depletion region (as sketched in Fig. 1.3). Its worth to notice, that the reduction of free charges was needed to use the silicon as a radiation sensor and that is exactly what is happening within the depletion region.

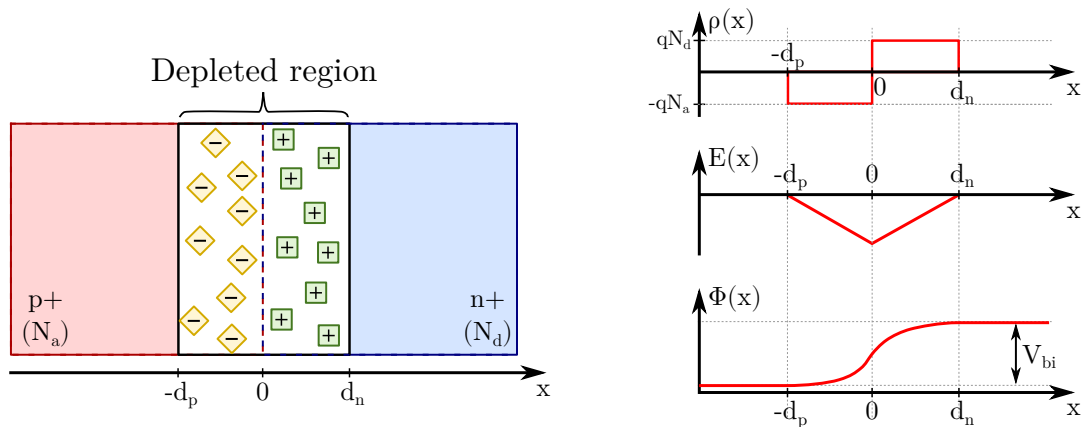


FIGURE 1.3: Sketch of a  $pn$ -junction and corresponding distributions of space charge  $\rho(x)$ , electric field  $E(x)$ , and build-in potential  $\phi(x)$ . Uncovered, positively and negatively charged ions are marked with squares and rhombuses respectively.

The size of the depletion region and the electric field across the junction depends on the doping concentration of both sides and can be calculated assuming that all dopant atoms are ionized within the depletion region.

The electric field  $E(x)$  can be obtained using the Gauss law:

$$\frac{dE(x)}{dx} = \frac{\rho(x)}{\epsilon_0 \epsilon_r} \quad (1.1)$$

where  $\rho(x)$  is space charge distribution,  $\epsilon_0$  and  $\epsilon_r$  are respectively vacuum permittivity and relative permittivity. Since in the depletion region there are no free charges the space charge distribution is formed only by uniformly distributed dopant ions. Because of the charge conservation:

$$qN_d d_n = qN_a d_p \quad (1.2)$$

where:

- $q$  – electron charge,
- $N_a$  – acceptor concentration,
- $N_d$  – donor concentration,
- $d_p$  – depletion depth on acceptor side,
- $d_n$  – depletion depth on donor side.

Assuming the junction at  $x = 0$  with  $p$ -type doping on the left side and  $n$ -type doping on the right side (as presented in Fig. 1.3), the space charge can be expressed as:

$$\rho(x) = \begin{cases} -qN_a & \text{for } x \in (-d_p : 0) \\ qN_d & \text{for } x \in (0 : d_n) \end{cases} \quad (1.3)$$

After applying to Eq. 1.1 and performing integration:

$$E(x) = \begin{cases} \frac{-qN_a}{\epsilon_0 \epsilon_r} (x + d_p) & \text{for } x \in (-d_p : 0) \\ \frac{qN_d}{\epsilon_0 \epsilon_r} (x - d_n) & \text{for } x \in (0 : d_n) \end{cases} \quad (1.4)$$

To get the distribution of the build-in potential  $\phi(x)$  one more integration is needed. Therefore, taking as a boundary condition  $\phi(x = 0) = 0$ , one gets:

$$\phi(x) = \begin{cases} \frac{qN_a}{\epsilon_0 \epsilon_r} \left( \frac{1}{2}x^2 + xd_p \right) & \text{for } x \in (-d_p : 0) \\ \frac{-qN_d}{\epsilon_0 \epsilon_r} \left( \frac{1}{2}x^2 - xd_n \right) & \text{for } x \in (0 : d_n) \end{cases} \quad (1.5)$$

The build-in voltage ( $V_{bi}$ ) across the junction can be calculated as:

$$V_{bi} = \phi(d_n) - \phi(-d_p) = \frac{q}{2\epsilon_0 \epsilon_r} (N_d d_n^2 + N_a d_p^2) \quad (1.6)$$

Finally, the relation for the total depletion depth  $D = d_n + d_p$  may be obtained from Eq. 1.2 and Eq. 1.6:

$$D = \sqrt{\frac{2\epsilon_0 \epsilon_r}{q} \frac{N_d + N_a}{N_d N_a} V_{bi}} \quad (1.7)$$

Since the build-in voltage in silicon is around 0.6-0.7 V the self-created depletion region usually



spreads only across several dozen micrometers. However, by applying an external voltage to the junction its width may be changed: shorten for a forward bias and widen for a reverse bias. Since for the radiation sensor the larger the depletion region is the better, let us consider the second option. By applying the negative voltage to the  $p$  side and positive to the  $n$  side more electrons are forced to leave the  $n$  side, leaving unbalanced donor ions. And *vice versa* in the  $p$  type part, which straightforwardly leads to the extension of the volume without free charges. Since all the mechanisms leading to build-up the depletion region are the same as in derivation above, the equation 1.7 for the total depletion depth can be simply adopted by introducing an additional variable corresponding to the external bias voltage  $V_{bias}$ .

$$D = \sqrt{\frac{2\epsilon_0\epsilon_r}{q} \frac{N_d + N_a}{N_d N_a} (V_{bi} + V_{bias})} \quad (1.8)$$

As it was already mentioned, the signal can be extracted from the silicon devoid of free charges. Therefore, in most applications the depletion of the whole sensor volume is desired. For that reason a highly asymmetrical (in the sense of dopings) junctions are often used. Following the equation 1.2 it is clear that having a  $N_a \gg N_d$  (or  $N_d \gg N_a$ ) the depletion range towards  $n$ -doped side (or  $p$ -doped side respectively) will be much larger than to the opposite. That is why the sensors are usually made of very lightly doped wafers (either  $p$  or  $n$  type) with the typical concentrations on the order of  $10^{12}$  to  $10^{14}$  atoms per cubic centimeter and shallow highly doped implants of the type opposite to the wafer on the top side.

An often used sensor parameter is a full depletion voltage  $V_{FD}$  which is the minimum voltage that provides depletion across the whole sensor thickness. It can be directly extracted from equation 1.8, assuming certain detector thickness  $D_{det}$  and neglecting the build-in potential which is typically orders of magnitude lower than the external bias voltage:

$$V_{FD} = \frac{q}{2\epsilon_0\epsilon_r} \frac{N_d N_a}{N_d + N_a} D_{det}^2 \quad (1.9)$$

Having in mind the condition of high asymmetry in the doping concentration, the highly doped factor can be cancelled out leaving only a term connected with the wafer doping concentration  $N_w$  ( $N_w = N_d$  for  $n$ -type wafer or  $N_w = N_a$  for  $p$ -type):

$$V_{FD} \simeq \frac{q}{2\epsilon_0\epsilon_r} N_w D_{det}^2 \quad (1.10)$$

It can be further written in terms of wafer resistivity  $\rho = \frac{1}{q\mu N_w}$  as:

$$V_{FD} \simeq \frac{D_{det}^2}{2\epsilon_0\epsilon_r\mu\rho} \quad (1.11)$$

where  $\mu$  is electron mobility in silicon ( $\mu_e \sim 1350 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ ) for  $n$ -type wafer or hole mobility ( $\mu_h \sim 450 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ ) for  $p$ -type one [3]. Furthermore, a simplified formula for the depletion depth can be written as:

$$D \simeq \sqrt{2\epsilon_0\epsilon_r\mu\rho V_{bias}} \quad (1.12)$$

Now its clearly visible that the higher the wafer resistivity is the easier the depletion develops, so its very desired to have it as high as possible. Moreover, it may happen that with the low resistive wafer the full depletion voltage can be higher than the breakdown voltage making the full-depletion impossible. Therefore, depending on the sensor bias voltage, a detector may operate in three different conditions: under-depletion ( $V_{bias} < V_{FD}$ ), full-depletion ( $V_{bias} = V_{FD}$ ) and over-depletion ( $V_{bias} > V_{FD}$ ). The electric field distribution inside the wafer is:

$$E(x) = \begin{cases} \frac{2V_{bias}}{D} \left(1 + \frac{x}{D}\right) & \text{for } x \in (0 : D) \quad - \text{ under-depletion} \\ \frac{2V_{FD}}{D_{FD}} \left(1 + \frac{x}{D_{FD}}\right) & \text{for } x \in (0 : D_{FD}) \quad - \text{ full-depletion} \\ \frac{2V_{FD}}{D_{FD}} \left(1 + \frac{x}{D_{FD}}\right) + \frac{V_{bias}-V_{FD}}{D_{FD}} & \text{for } x \in (0 : D_{FD}) \quad - \text{ over-depletion} \end{cases} \quad (1.13)$$

To achieve the possibility of position measurement a top implants are usually segmented into strips (providing one-dimensional information) or into pixels (for two-dimensional measurement). Therefore, each of these segments creates a separate  $pn$ -junction and allow for an independent measurement. The distance between the strips or pixels centers is usually called the pitch. The lower the pitch is the finer the segmentation, allowing for more precise measurement.

Another very important sensor parameter directly connected with the segmentation is the sensing node capacitance  $C_D$ . Since the depletion region acts same as a plate capacitor with the silicon as a dielectric, one can define:

$$C_D = \begin{cases} \frac{\epsilon_0 \epsilon_r S}{D} = \sqrt{\frac{\epsilon_{Si}}{2\rho\mu V_{bias}}} & \text{for } V_{bias} \leq V_{FD} \\ \frac{\epsilon_0 \epsilon_r S}{D_{FD}} = const & \text{for } V_{bias} > V_{FD} \end{cases} \quad (1.14)$$

where,  $S$  is the ‘‘plate’’ area which corresponds to the area of strip or pixel implant size. One has to notice that this formula takes into account only the capacitance created between the sensing node and the back plane of the detector. In some particular situations also other components (for example capacitance between the neighbouring strips/pixels) may not be negligible.

### 1.2.2 Interaction of particles with matter

There are several mechanisms by which a particle may interact with a sensor while passing through its volume, but the most significant are the electromagnetic interactions. The signal formation inside a sensor volume highly depends on the incident particle type, its energy or mass. Fortunately, all different cases can be categorized into few groups, that have to be studied separately.

#### Charged particles

All charged particles may interact electromagnetically either with the electrons or with the atoms nuclei, which will lead to change of theirs energy and movement direction. Nevertheless, the interactions with the nucleus are highly suppressed by the low cross-section, so in the first order only the interactions with the shell electrons have to be considered. The incident

particle mass has also significant impact on the interaction dynamics, therefore light lepton beams (electrons and positrons) have to be studied separately. All the other charged hadronic particles and heavy leptons may be studied together since their mass is at least two orders of magnitude higher than electron mass.

In general, there are two main processes that lead to the energy transfer between the incident particle and the sensor volume, the ionization and the radiative losses. The radiative losses correspond to the interactions of the moving charged particle with the electric field inside a sensor, which can lead for example to the Bremsstrahlung photons emission or the electron-positron pairs creation. For high mass particles this phenomena occurs only at very high energies exceeding several hundred GeV. Therefore, ionization plays a dominant role in the charge generation by the heavy charged particles.

The mean energy loss  $\left\langle \frac{dE}{dx} \right\rangle$  of a charged particle per distance travelled through the matter is described by the Bethe-Bloch formula [14]:

$$-\left\langle \frac{dE}{dx} \right\rangle = 4\pi N_A r_e^2 m_e c^2 \frac{z^2}{\beta^2} \frac{Z}{A} \left[ \frac{1}{2} \ln \frac{2m_e c^2 \beta^2 \gamma^2 T_{max}}{I^2} - \beta^2 - \frac{\delta(\beta\gamma)}{2} \right] \quad (1.15)$$

where:

- $N_A$  – Avogadro number,
- $r_e$  – classical electron radius,
- $m_e$  – rest mass of an electron,
- $c$  – speed of light,
- $z$  – charge of incident particle,
- $Z$  – atomic number of the medium,
- $A$  – atomic mass of the medium,
- $\beta$  – incident particle velocity ( $\beta = \frac{v}{c}$ ),
- $\gamma$  – Lorentz factor ( $\gamma = \frac{1}{\sqrt{1-\beta^2}}$ ),
- $T_{max}$  – maximum kinetic energy that can be transferred in a single collision,
- $I$  – mean excitation energy,
- $\delta(\beta\gamma)$  – density correction.

Fig. 1.4 shows the Bethe-Bloch relation for three exemplary particles in different materials. As one can see the overall function shape remains the same (especially for materials with  $Z > 2$ ) with slightly decreasing mean energy loss for heavier materials. The common feature independent on the passing particle type and the medium is the rapid growth at low energies, which leads to a high energy depositions just before stopping the passing particle. This is commonly known as the Bragg peak. Another common feature is a shallow minimum at  $\beta\gamma \sim 3$ . Particles with energies close to that minimum are often referred to be minimum ionizing particles (MIP). Towards the higher energies the mean energy loss starts to grow slightly due to increasing probability for radiative processes. As one can notice, scales for the muon and pion, which are very close in mass, are very similar, whereas for almost ten times heavier proton the momentum scale is around one order of magnitude higher. Nevertheless, from the practical point of view, all heavy charged particles in high energy experiments are

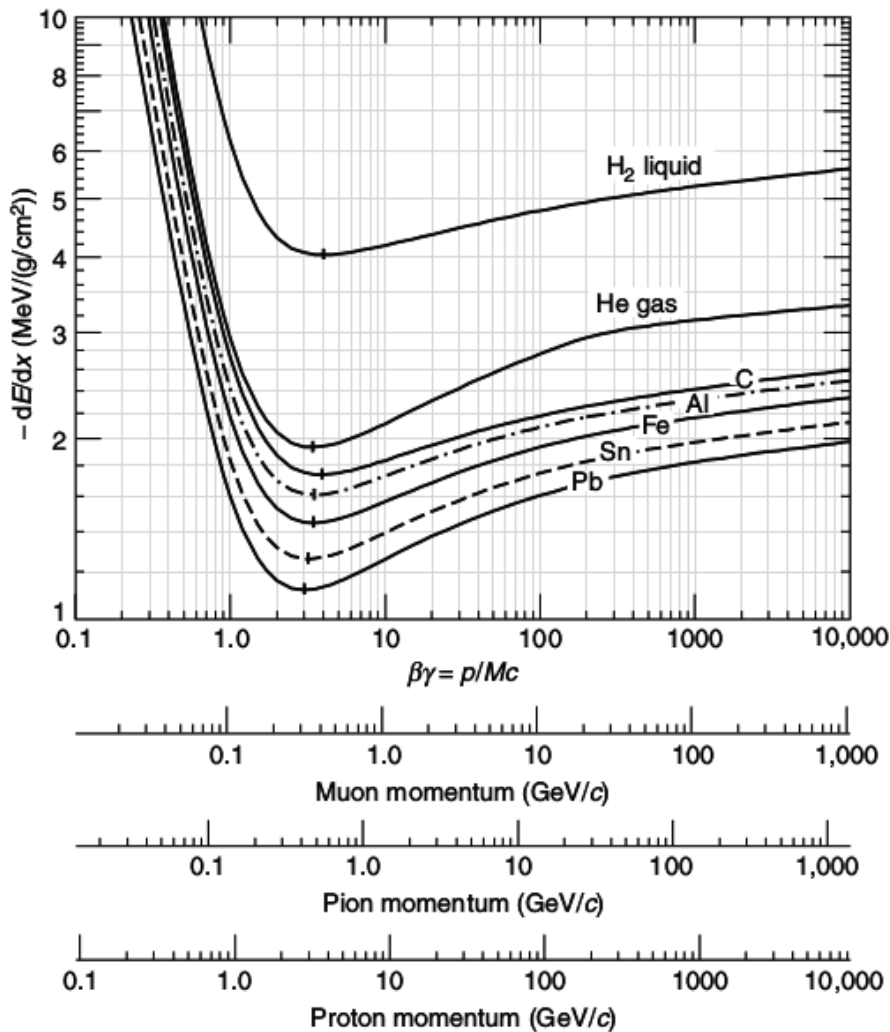


FIGURE 1.4: The mean energy loss in various materials presented for muons, pions and protons (figure from [14].)

often treated as MIPs since their energies are high enough to place them in the plateau region, where the differences in the mean energy loss are minor.

The only exception are the electrons (and positrons) mentioned before. For them the minimum appears slightly above 1 MeV and, what is most important, the radiative processes start to dominate over the ionisation already around 20 MeV, which is still inside the observed momentum range.

Ionisation across the passage of the incident particle is a stochastic process therefore the fluctuations of the energy loss appear, which is not described by the Bethe-Bloch formula. For large energy depositions the fluctuations undergo normal distribution, but this is not the case for a thin radiation sensor typically used in a particle physics experiments. For a thin detector there is a limited number of high-energy transfer collisions, which result in an asymmetric tail towards higher values in the deposited energy distribution. There are few approaches to describe this energy spectrum, but the most common is the Landau-Vavilov distribution that can successfully predict the most probable value (MPV) of the energy deposition (which is

typically the value of interest) instead of mean value [14]:

$$\Delta E = \xi \left[ \ln \frac{2m_e c^2 \beta^2 \gamma^2}{I} + \ln \frac{\xi}{I} + 0.2 - \beta^2 - \delta(\beta\gamma) \right] \quad (1.16)$$

where:

$$\xi = 2\pi N_A r_e^2 m_e c^2 \left\langle \frac{Z}{A} \right\rangle \frac{x}{\beta^2}$$

and  $x$  is moderate sensor thickness given in  $\text{g cm}^{-2}$ .

An example of energy loss spectrum for 500 MeV pions passing through the thin silicon layers of different thickness is shown in Fig. 1.5, where the difference between the mean energy loss and the most probable energy loss is clearly visible. Moreover, comparing the curves obtained for different thicknesses one can directly spot the decreasing energy transfer per micrometer for thin detectors.

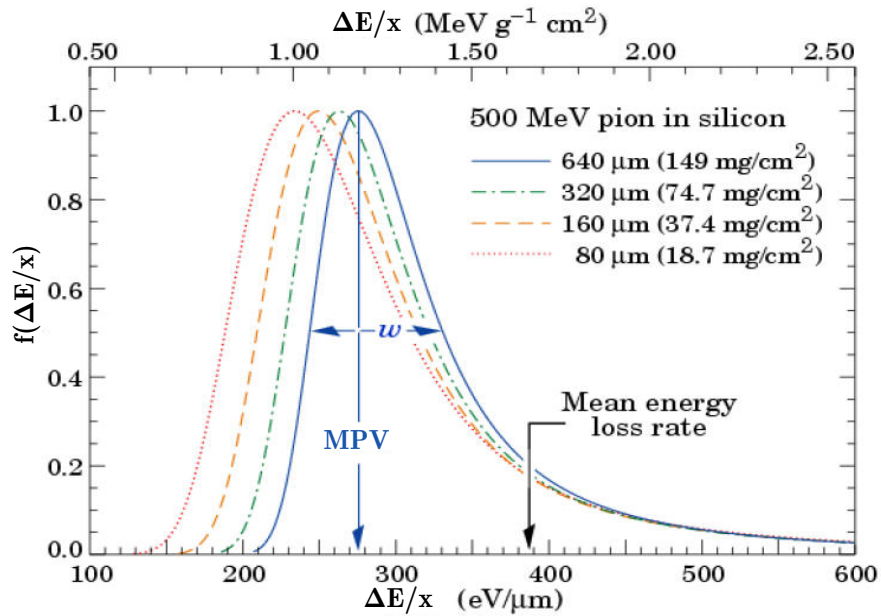


FIGURE 1.5: Energy loss spectrum for thin silicon layers, normalized to unity at the most probable value (figure from [14]).

## Photons

The interaction of photons with matter looks completely different. Contrary to the charged particles they do not lose their energy gradually along the travelled path. There are several different processes through which photons can interact with matter but regardless of that they are usually fully absorbed in a single interaction or at least they transfer a significant fraction of their energy.

For low energetic photons (ultraviolet or soft X-rays) with energies up to  $\sim 10$  keV, the interaction is mainly dominated by the photoelectric effect. In this process an incident photon interacts with an inner-shell electron bound in an atom. Its energy is fully transferred to the

electron which is knocked out of the atom, with the kinetic energy equal to the incident photon energy reduced by the electron binding energy.

For hard X-rays, with energies from  $\sim 100$  keV up to 1 MeV the Compton effect dominates. In this process the incident photon interacts with loosely bind electrons from the valence shell, and its energy is only partially transferred. Therefore, after the interaction, beside the knocked electron also a scattered photon remains, but its energy is usually highly decreased.

After exceeding 1 MeV, photon energy becomes large enough to unlock another process – pair production. In the vicinity of a nucleus the incoming photon may interact with its electric field and convert into an electron-positron pair. The cross-section for all mentioned processes in the function of photon energy is shown in Fig. 1.6.

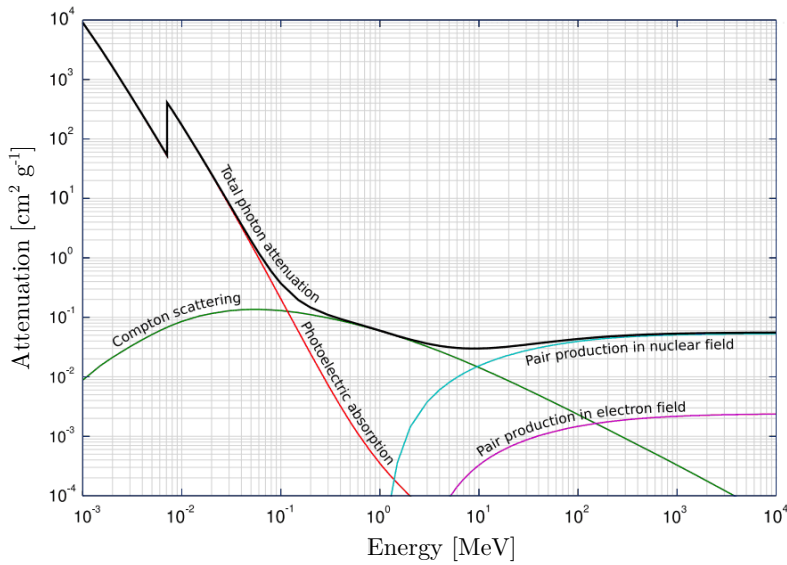


FIGURE 1.6: Photon flux attenuation coefficient in the function of photon energy. Components from different processes drawn with different colours, whereas a combined value is shown in black (figure from [15]).

### 1.2.3 Signal formation – Shockley-Ramo theorem

A common approach is to consider the carriers arriving to the collection electrode as a signal. However, to properly describe the input signal one has to consider the current induced in the sensing node by the motion of the carriers in the electric field of the sensor. Thus to specify the signal seen on the input of the readout electronics one has to follow the Shockley-Ramo theorem [16, 17]. It states that the current  $i_k(t)$  induced by the k-th component  $Q_k$  of the total charge is given by:

$$i_k(t) = Q_k \vec{v}_k(t) \cdot \vec{E}_{w_k}(r) \quad (1.17)$$

where  $\vec{v}_k(t)$  is velocity of the k-th charge component and  $\vec{E}_{w_k}(r)$  is so called weighting field. This is a hypothetical electric field at point  $r$ , that would be induced after removing  $Q_k$

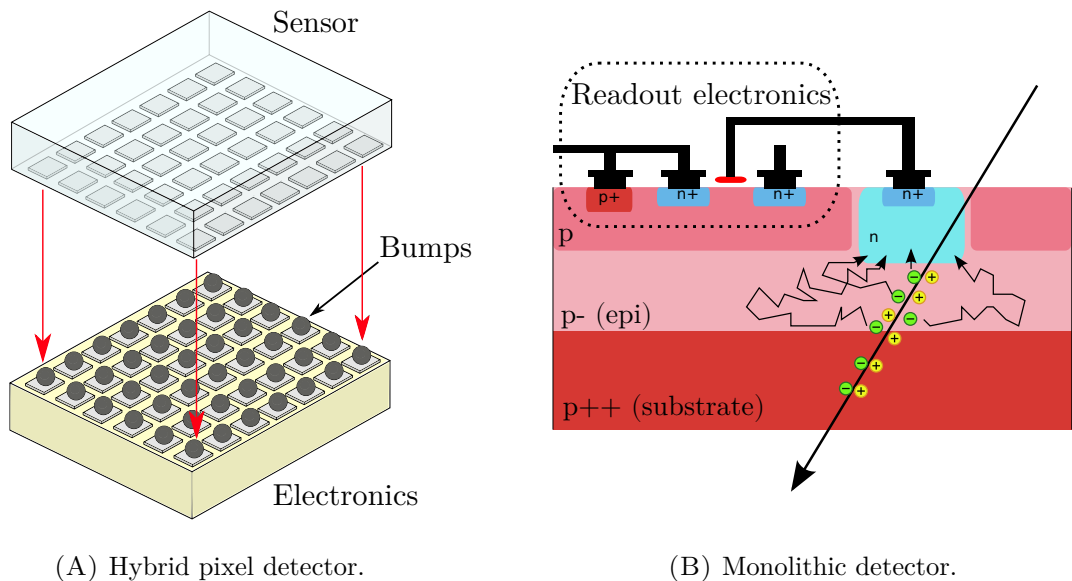
charge from the sensor volume and after applying 1 V to the collecting electrode, with all other electrodes of the sensor grounded.

It has to be pointed out that this method converges with a naive approach, in the sense that the total current signal integrated over the collection time is equal to the total charge collected at the electrode.

## 1.3 Basics of monolithic detectors

### 1.3.1 Monolithic versus hybrid solutions

The idea of hybrid pixel detectors is a straightforward evolution of the concept known from the strip detectors, where a sensor and a readout electronics are fabricated separately and connected afterwards by the wire-bonding. It is a simple and convenient method since both the sensor and the electronics can be developed and optimized separately. Unfortunately, for the pixel detectors the wire-bonding technique is no longer suitable because the number of individual channels becomes too large, but once a bump-bonding technique was developed, the sensor-readout interconnection was no longer a problem (as shown in Fig. 1.7A).



(A) Hybrid pixel detector.

(B) Monolithic detector.

FIGURE 1.7: Schemes of monolithic and hybrid detector.

The flexibility of the hybrid detectors caused their widespread use in many fields of sophisticated and demanding applications. On the other hand, even if the bump-bonding process is used from many years its yield is still not perfect, what highly increases the costs of hybrid detectors. It is one of the reasons why a monolithic approach to the pixel detectors fabrication is being considered. Since both the sensor and the electronics are made on silicon wafers it is somehow natural to try to integrate them and fabricate together on the same wafer (as shown in Fig. 1.7B). Unfortunately, there are several issues that for many years successfully prevented the utilization of monolithic devices. For example the sensing wafer is usually very lightly doped (to allow its easy depletion), whereas for the electronics fabrication a relatively

highly doped wafers are used. Beside that, when both the sensor and the electronics are implemented in the same wafer, they start to interfere with each other, which also causes many issues. Fortunately, after many years of the development and the evolution of the CMOS process, nowadays there are several different methods that allow for the fabrication of monolithic pixel detectors. Of course they are not yet as mature as the hybrid devices, but they have just started showing their capabilities.

### 1.3.2 Available technologies

#### DEPFET

DEpleted P-channel Field Effect Transistor (DEPFET) detectors are based on the concept of the FET transistor, which channel conductivity is controlled by an electric field. Schematic view of the DEPFET structure, with the potential level across its depth is shown in Fig. 1.8.

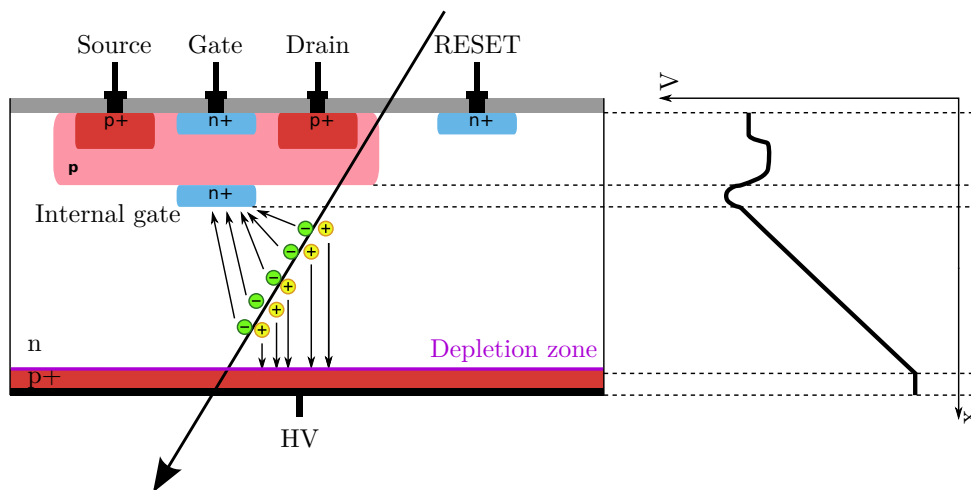


FIGURE 1.8: Schematic of DEPFET detector structure on the  $n$ -type wafer, with the ionizing particle passing through its volume and a waveform showing the electrostatic potential in function of the detector depth.

Its working principle is very simple. Once a charge is induced within a depleted sensing volume the field lines push the electrons towards the local potential maximum located at the internal gate. The growing amount of electrons within the internal gate increases the conductivity of the FET transistor, generating therefore the electric current proportional to the gathered charge. The charges remain in the internal gate until the positive resetting pulse appears, which attracts them to the reset electrode. The main advantage of this kind of structure is that a single FET transistor may act as a sensor, an amplifier and a memory cell. First devices based on DEPFET technology have been recently installed in the Belle II Vertex Detector [18].

#### High Voltage CMOS

High Voltage CMOS (HV-CMOS) technology is based on a standard CMOS process that has been adopted in the way that one can bias the substrate with a high voltage. The scheme



showing the HV-CMOS detector structure is presented in Fig. 1.9. In this approach the whole readout electronics is located in a large well that at the same time acts as the sensing node. This solution ensures shielding of the electronics from the influence of high voltage applied to the substrate, but on the other hand the size of the input node is determined by the complexity of the in-pixel electronics. Thus, in this solution there is a trade-off between the input node capacitance (determining the input noise) and the signal processing capabilities.

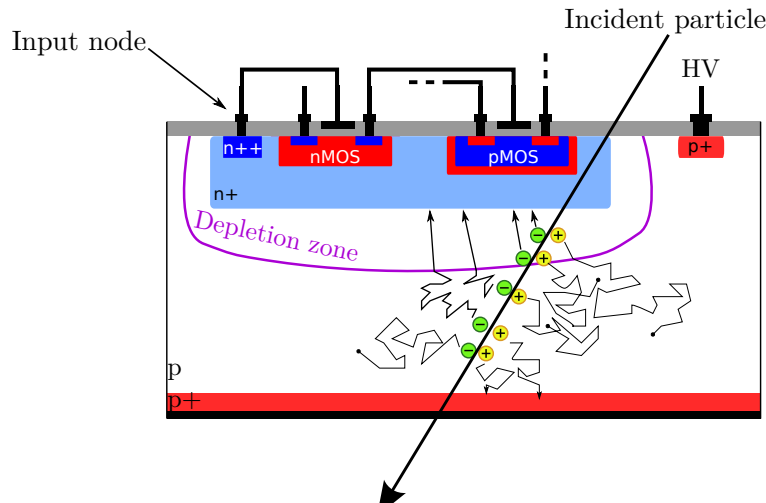


FIGURE 1.9: Schematic of HV-CMOS detector structure on the  $p$ -type wafer, with the ionizing particle passing through its volume.

One of the main advantages of this approach is definitely its similarity to the classical CMOS structure. In principle it may be produced in any foundry offering multiple well CMOS process, and so such devices can be widely available. Unfortunately, there are also several quite important downsides. One of them is already mentioned trade-off between the readout electronics complexity and the input capacitance. Another very important aspect is a major problem with the full-depletion of this kind of devices, which not only reduces the input signal but also may lead to detector inefficiency. Nevertheless, for some applications HV-CMOS detectors may suit very well. For example they are being considered for the *Mu3e* experiment [19] or for the ATLAS Inner Tracker upgrade [20].

### High Resistivity CMOS

The High Resistivity CMOS (HR-CMOS) detectors derive from a very similar approach as the HV-CMOS devices. They are also fabricated in a standard CMOS technology, but slightly modified to allow the substrate depletion. In contrary to the HV-CMOS, in HR-CMOS the readout electronics is not placed within the sensing well, which overcomes one of the main issues of the HV-CMOS. The sketch of the HR-CMOS detector is shown in Fig. 1.10.

In this kind of devices the electronics is placed in the well used for the sensor biasing, whereas the input node is formed by a small implantation of the opposite type to the substrate doping. Moreover, such strategy has several repercussions. First of all it is beneficial in terms of the input capacitance reduction and thus allow for a very low-noise detectors fabrication. But according to Fig. 1.10 one can see that in this approach the  $pn$ -junction is formed not only

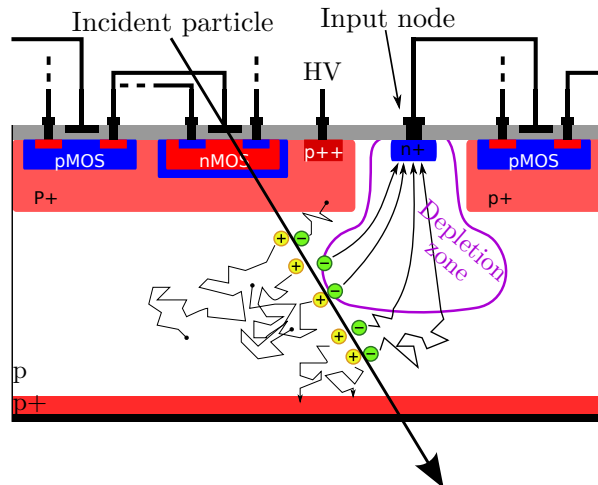


FIGURE 1.10: Schematic of HR-CMOS detector structure on the  $p$ -type wafer, with the ionizing particle passing through its volume.

between the sensor bias (HV) and the input node, like in the previous solution. Here another  $pn$ -junction is also created between the sensor bias and the implemented electronics, which results in a quite restrictive limitation on the maximum sensor bias voltage. In order to prevent from the breakdowns the HV usually has to be kept below  $\sim \pm 10$  V. Unfortunately, low sensor polarization voltage together with a small sensing implantation directly leads to a very small depletion zone, which is the main disadvantage of this solution. In order to minimise this issue one has to utilize a high resistive substrate, which allow for a broader depletion zone development (and give the name of this technique). Nevertheless, even with the highly resistive wafers it is very hard to force the depletion zone development below the wells containing the electronics. Fortunately, several modifications of the doping plan have been proposed recently, that allow for the shallow depletion layer formation over the whole pixel area. This approach seems to be promising and it is developed by many groups. For example HR-CMOS detector called ALIPDE is considered for the ALICE Inner Tracking System upgrade [21].

### Silicon-On-Insulator CMOS

Another CMOS process that may be adopted for the monolithic detectors fabrication is the Silicon-On-Insulator (SOI) CMOS. The schematic view of the SOI detector structure is presented in Fig 1.11. In this approach a thin silicon layer with electronics is being separated from the handling wafer (substrate) by an insulator. Originally it was aimed for the improvement of the circuitry performance, but it also gives a perfect opportunity for the monolithic detectors design. As shown in Fig 1.11 in the SOI detectors the sensor is formed by an  $pn$ -junction implemented within the substrate, whereas the whole readout electronics is located just above.

In the SOI the handling wafer may have completely different characteristics than the silicon dedicated for the electronics. Thus one can freely use a highly resistive substrates similar to the ones used in the hybrid sensors and so there are no major problems with the full depletion of the entire substrate volume, even a thick one.

Since the SOI technology was the one that was exploited for the purpose of this thesis its wider characterization is presented in the next section.

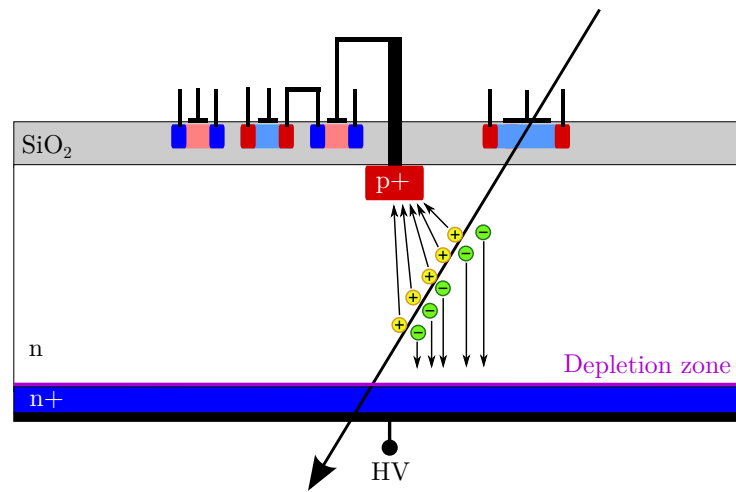


FIGURE 1.11: Schematic of SOI detector structure on the  $n$ -type wafer, with the ionizing particle passing through its volume.



## Chapter 2

# Silicon-On-Insulator technology

### 2.1 General overview

The Silicon-On-Insulator (SOI) CMOS technology refers to the microelectronics manufacturing method where instead of a single crystal substrate wafer a more complex structure is used. The SOI wafer consists of a thin single crystal silicon layer where the electronics is implemented, separated from the handling wafer by an insulating layer (typically silicon dioxide or sapphire).

The SOI structure has been introduced to overcome the limitations encountered during the continuous miniaturization of microelectronics devices. There are several benefits of using the SOI wafer instead of a traditional bulk substrate:

- reduction of the parasitic capacitances to the substrate,
- latch-up immunity due to full isolation of n-well and p-well devices,
- limitation of the leakage currents,
- increased resistance to the Single Event Upsets induced by the ionizing radiation,
- better wafer utilization thanks to higher component densities at the same technology node.

All these advantages allow to increase the operation speed together with the reduction of the power consumption, which is very desired especially for the complex digital circuitries.

Moreover, from the fabrication perspective, the SOI wafers are almost completely compatible with the standard CMOS production process. Therefore, many leading IC companies decided to establish the SOI process for their high-end products. As an example, in the year 2000 IBM released their top microprocessor RS64-IV “Istar” fabricated on the SOI wafer. Also AMD has began to manufacture their x86 architecture microprocessors on the SOI, starting from the single-core Opteron fabricated in 130 nm and its multi-core successors produced in 90 nm, 65 nm, 45 nm and 32 nm nodes. Thanks to the high-performance capabilities of the SOI based processors many of the top supercomputers exploits the SOI microprocessors. For example the supercomputer called “Summit” at Oak Ridge National Laboratory, which currently is the most powerful machine in the world (operating at 143 PFLOPS/s), exploits IBM POWER9 processors manufactured in the 14 nm FinFET SOI technology. Also many of the commercial gaming consoles, like XBOX 360, Play Station or Wii, contain processors fabricated on the SOI wafers [22, 23].

All those examples show how beneficial is the separation of the electronics from the substrate wafer in terms of the chip performance. But concerning the scope of this thesis the most important feature of the SOI wafer is the possibility to use a thick bottom silicon layer as a radiation sensor with a readout electronics placed on top of it in thin silicon layer, and thus forming together a monolithic detector. Moreover, thanks to the fact that the top and the bottom silicon layers in the SOI structure come from two different initial wafers, they may have completely different electrical characteristics. The top layer can have relatively low resistivity suitable for the electronics implementation, whereas for the bottom sensing part a high purity silicon can be used.

## 2.2 Wafer preparation methods

Over the years, many SOI wafer preparation methods have been developed. The first attempts were made in 1960s, where instead of the silicon dioxide, a sapphire was used as an insulator. In 1963 Harold Manasevit successfully prepared a Silicon-On-Sapphire (SOS) wafer utilizing the epitaxial silicon growth over the single crystal sapphire layer. Currently, the SOS wafers are still being prepared using this technique, but obtaining a high quality silicon layer is still a challenge.

In early 70's an alternative method based on the epitaxial lateral overgrowth (*ELO*) was explored. In this approach holes are drilled in initially oxidized silicon wafer, which allows for the lateral growth of the silicon through the hole and later on over the insulator layer. The downside of this method is a substantial limitation on the area of the overgrowth.

The demand for the radiation-hard devices for space and military applications revealed in the intensified interest in the SOI technology. Unfortunately, none of mentioned method was suitable for the industrial scale production. The augmented effort for the evolution of the SOI technologies contributed to the development of *SIMOX* process (Separation by IMplantation of OXYgen), where an insulating silicon dioxide layer is introduced within a standard CMOS wafer. This technique is based on the ion beam implantation. The oxygen ions are introduced at certain depth and afterwards during the high temperature annealing form buried oxide (BOX) layer [24].

Later on several other SOI wafer preparation methods, suitable for mass-scale production, were proposed. In contrary to *SIMOX* process they do not act on a single wafer, but utilize a direct bonding of two silicon wafers. The most widely used are *BSOI* (Bond Silicon-On-Insulator), *Eltran* and *Smart Cut* technologies, which became mature enough to provide the SOI silicon quality comparable with the bulk silicon wafers.

The *BSOI* method was introduced in 1980s when several processes for the direct bonding of silicon wafers were developed. The *BSOI* process employs two initial silicon wafers. In the first step one of them is oxidized over its surface (by the thermal growth or a deposition), which forms a BOX layer. Next, two wafers are bond together and annealed to enhance the connection. Afterwards, one side is being grinded to the desired thickness which finishes the SOI wafer fabrication [24].

*Eltran*, which stands for Epitaxial Layer TRANSfer process was developed by Canon and is more cost-effective because it is non-destructive to the undesired silicon part (no grinding of almost whole wafer thickness as in *BSOI* is needed). The remains from one process can be reused later. Similarly to the *BSOI* technique the *Eltran* also utilizes two initial wafers. On one of them a porous silicon layer is formed on its surface. Later on, a high quality epitaxial layer is deployed on top of the porous layer. After that the BOX layer is formed by the thermal oxidation of the top part of the high quality epitaxial layer. Next, such a structure is bonded to the second (handling) wafer. After the bonding, a separation is done along the mechanically weak, porous layer by applying a mechanical stress. The remaining porous layer is removed, leaving only the high quality epitaxial layer on top of the SOI structure, whereas the second part may be reused during the next iteration [24].

The most recent from the presented techniques, and particularly important concerning the scope of the presented thesis, is the *Smart Cut* technology, which was exploited for the wafer production for all presented prototypes. The *Smart Cut* technique, being developed since 1993, is suitable for the large scale production, therefore it is relatively widely used for the SOI wafer manufacturing. This approach is also based on the direct bonding of two wafers, similar to *BSOI* and *Eltran* methods. The *Smart Cut* process flow is shown in Fig. 2.1. In the first step the surface of one of the initial wafers is thermally oxidized. After that, light ions (like hydrogen or helium) are implanted through the oxide into the silicon, which leads to the formation of mechanically weak surface at the certain depth of the wafer. Later on both wafers are carefully cleaned and their surfaces are prepared for the wafer bonding. When two wafers are bonded together the separation along the previously produced weakened surface takes place. It may be carried out by heating the whole structure up to the temperature, when the thermal energy is sufficient to initiate the splitting or by applying the mechanical force. A final step is a standard conditioning treatment of created SOI structure, which includes polishing of the surface and annealing that strengthen the bonding interface [24].

The leftover wafer part, which was split out off the SOI wafer, is also subjected to the conditioning treatment. The weakened volume is grinded, its surface is repolished and the wafer is suitable for use in the subsequent *Smart Cut* process as one of the initial wafers.

## 2.3 SOI features

There are many benefits of SOI CMOS, which have been already mentioned, but its utilization is limited to the hi-end or very unconventional products. The main obstacle preventing the widespread use of the SOI CMOS are still the wafer quality and higher costs. Moreover, despite many similarities between the SOI and bulk CMOS process, there are several differences that need to be taken into account during the SOI IC design.

### 2.3.1 Partially-Depleted and Fully-Depleted SOI

Apart from the wafer preparation method, there are two types of SOI CMOS processes: Partially-Depleted (PD-SOI) and Fully-Depleted (FD-SOI). This terms refer to the relation between the thickness of the top thin silicon layer and the thickness of channel depletion layer

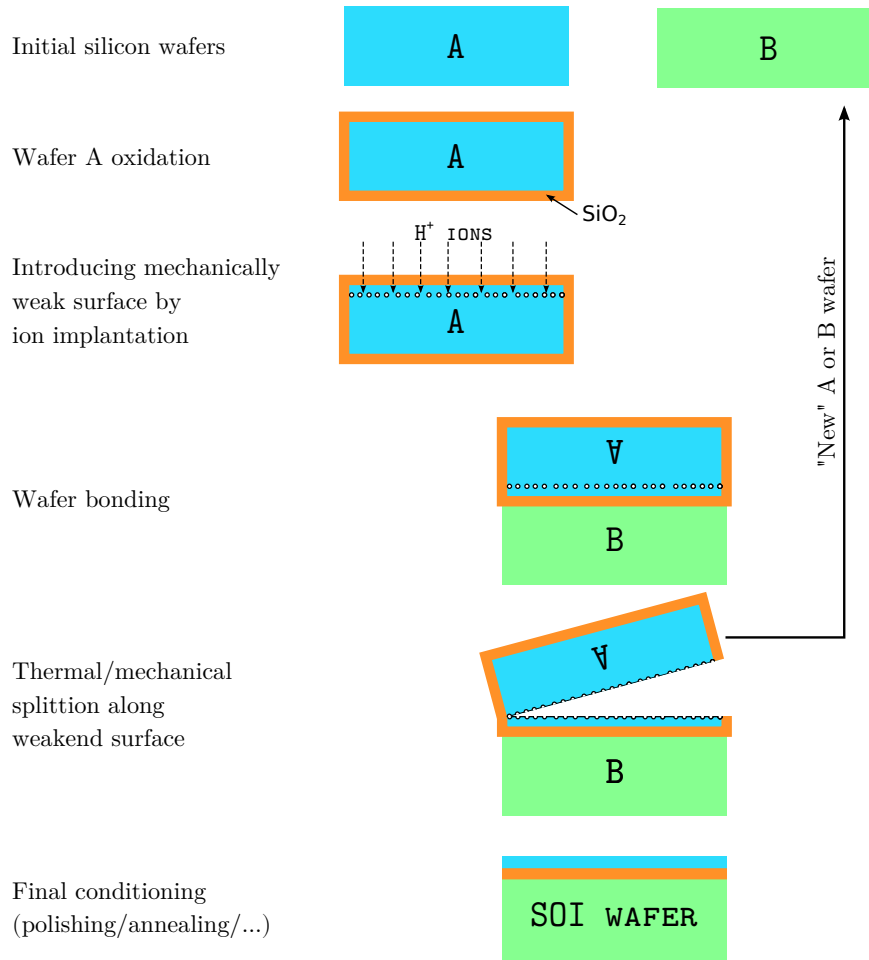


FIGURE 2.1: Sketch of the Smart Cut process flow.

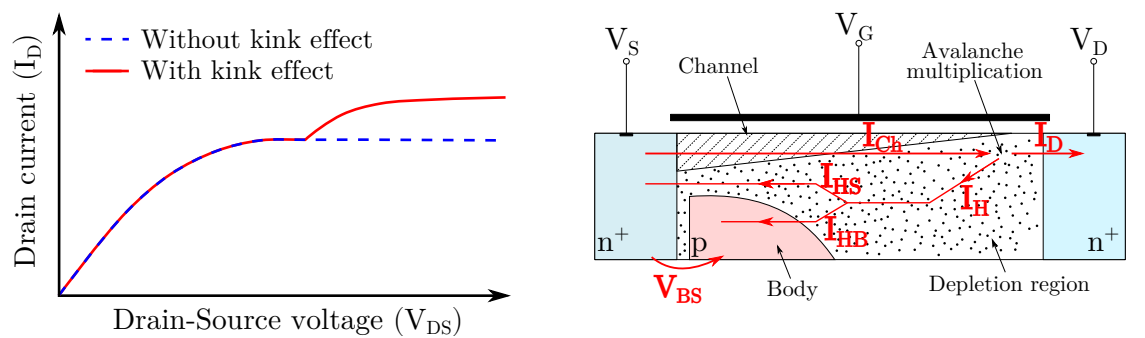
after setting a device into the operating point. In the Partially-Depleted process the silicon layer is thicker than the channel depth, whereas for the Fully-Depleted the channel is created over the whole top silicon thickness. The process classification depends mainly on the silicon layer thickness above the insulator and the doping concentration within the channel volume. Typically, to obtain the Fully-Depleted SOI, the top silicon layer has to be thinned down to about 100 nm or less. For example for 100 nm the transistor channel will spread over the whole silicon volume with the channel doping concentrations corresponding to the threshold voltages in the order of 300 – 400 mV. On the other hand, for 200 nm thick layer the doping should be reduced to the level corresponding to threshold voltages below 100 mV, which is no longer useful in practical applications [25].

There are several specific features of each process type that differ SOI CMOS from bulk CMOS, which have to be taken into account during the design as well as the technology characterization. For example one of the main drawback of the PD-SOI is the existence of the body-like region below the channel. In standard CMOS the bulk potential is always set to the fixed voltage, but in the SOI the undepleted body region remains floating which introduces atypical behaviour of PD-SOI transistors.



### 2.3.2 Kink effect

The most distinctive effect is called the *kink effect* [26] because it reveals as a *kink* in the output characteristic (shown in Fig. 2.2A). To explain it let us consider nMOS transistor in a saturation mode, as shown in Fig. 2.2B. The electrons are flowing through the channel ( $I_{Ch}$ ) to the region with a high electric field located close to the drain. In this region they are accelerated enough to induce the impact ionization and therefore create additional electron-hole pairs. The *new* electrons flow to the drain, whereas holes ( $I_H$ ) flows towards the source. But at the source contact they encounter a potential barrier ( $V_{BS}$ ), therefore holes start to accumulate within a body region. As the number of the gathered holes increases the body potential rises. The accumulation process stops when the body potential is high enough to allow the holes to flow to the source. At that point the system is in a balanced state where a number of generated holes is equal to the number of holes able to flow to the source. But since a certain number of holes is “trapped” within a body region, this causes the reduction of a transistor threshold voltage and thus drain current increases.



(A) Sketch of transistor output characteristic showing the influence of kink effect. (B) Sketch of the nMOS transistor showing the origin of kink effect.

FIGURE 2.2: Kink effect.

### 2.3.3 History effect

Former mechanism refers rather to the analog applications, but it affects also a digital circuitry. In digital applications the transistors analog characteristics are not necessarily concerned, but they have a direct reflection in the transistor switching time which is a very important parameter. Therefore, in the digital domain a similar mechanism reveals in issue called the *history effect*. This term refers to the transistors switching time dependence on its previous state. Since the switching time is directly connected with the transistor threshold voltage, its deviation leads to the excess of the timing uncertainty. On the other hand, for some specific conditions (specified by the previous state), the history effect leads to the reduction of the switching time. Thus, it should be noticed that this issue is not necessarily bad. The conscious usage of this feature may speed up an overall circuitry performance.

To overcome all the floating-body effects, a separate contact may be introduced for the body polarization (as in standard CMOS) or a build-in body connection with source may be implemented within the transistor structure. Unfortunately, this solution makes the transistor

<b>technology</b>	$S_{S-th}$
bulk CMOS	85 – 90 mV/dec
PD-SOI	80 – 85 mV/dec
FD-SOI	65 – 70 mV/dec
theoretical limit	$\sim 60$ mV/dec

TABLE 2.1: Standard subthreshold swing values at room temperature for different technologies [25].

unit larger, which reduces the transistor density per area. Another solution is to use the FD-SOI technology instead of PD where these effects are highly suppressed [24].

### 2.3.4 Subthreshold swing

Another very important factor that enhances the usage of the SOI technology (especially FD-SOI) over the bulk CMOS is a low value of a subthreshold swing  $S_{S-th}$  [27]. It describes the drain current behaviour at very low gate voltages and is usually defined as:

$$S_{S-th} = \ln(10) \cdot \frac{kT}{q} \left(1 + \frac{C_{dep}}{C_{ox}}\right) \quad (2.1)$$

where  $\frac{kT}{q}$  is a thermal voltage,  $C_{dep}$  is a depletion layer capacitance and  $C_{ox}$  is a gate-oxide capacitance.

Basically,  $S_{S-th}$  parameter determines how much the gate voltage has to increase/decrease to obtain ten times larger/smaller drain current. It is very important for the low voltage/low power applications to keep it as close as possible to the theoretical limit. It is so, because from one hand the transistor threshold voltage should be high to keep the leakage currents low (and therefore reduce the static power dissipation). On the other hand the lower the threshold voltage, the higher the speed. So having a low subthreshold swing it is possible to have a device with a relatively low threshold voltage ( $\sim 200$  mV) for high speed performance, but at the same time keeping its off-current low. The typical values for different technologies together with the theoretical limit determined by the thermal voltage are shown in Tab. 2.1 [25].

### 2.3.5 Device parameters mismatch

All features mentioned above show the predominance of the FD-SOI over the PD-SOI. However, there is one issue that affects the fully depleted structure more than the partially depleted one. It is the sensitivity to the nonuniformities of the top silicon layer thickness. This imposes quite excessive requirements on the wafer quality because even a single nanometer variation of the silicon layer thickness results in a threshold voltage shift of around 10 mV. Nevertheless, the wafer fabrication methods became more and more mature, which allows for a significant suppression of the mismatch issue and a straightforward trend towards the FD-SOI is seen [24].

### 2.3.6 Back-gate effect

Besides all the issues connected directly with the electronics fabricated on the SOI wafer, there are also additional effects that come from a nonstandard application of SOI technology, such

as the radiation detectors. As already mentioned to exploit the SOI structure as a monolithic detector, an extra layers have to be implemented within handling wafer to form the sensing diode. Its reverse bias allows to build-up the depletion zone. However, it has turned out that the sensor polarization voltage has a non-negligible impact also on the electronic circuitry implemented on the top of the structure. Since the top silicon is separated from the sensor by an insulator, applying a sensor bias voltage acts on transistor in the similar way as applying a voltage to its gate. This issue has been called a back-gate effect. Of course the *back-gate* has much lower impact than the standard gate because the thickness of the gate oxide is around two orders of magnitude lower than the thickness of a buried oxide. Nevertheless, one has to remember that voltages applied to bias the sensor are usually also hundred times larger than typical gate voltages. In practice, the influence of the sensor biasing voltage is clearly observed in the transistors characteristics, which in the extreme case may even lead to the constantly switched on or off transistors, independently from their gate voltages.

Since this issue became critical in terms of the SOI monolithic detectors, a solution for this problem has to be found out. A simple way to eliminate the back-gate effect is shielding of the electronics from the sensor electric field. The sensor electric field may be easily kept within the handling wafer part by introducing an additional doping layer – a lightly doped buried well located just beneath the oxide, p-type for the n-type substrate (BPW – Buried p-Well) and n-type for the p-type one (BNW – Buried n-Well), as shown in Fig. 2.3. Applying a fixed ground potential to this layer successfully eliminates the back-gate effect [28].

Such a solution works perfectly for the peripheral circuitry but it has also a negative impact on the sensing part of the readout. In order not to lose the efficiency, the buried well can not be directly biased by the fixed voltage because some part of the signal induced within a sensor would flow into this node and therefore would be lost. Thus the only solution is to connect the buried well directly with the sensing node. In this case the electronics is still shielded, the efficiency remains on the similar level but the capacitance of the sensing node is increased. This has a direct impact on increased readout noise and may also deteriorate the signal amplitude (depending on the input stage architecture).

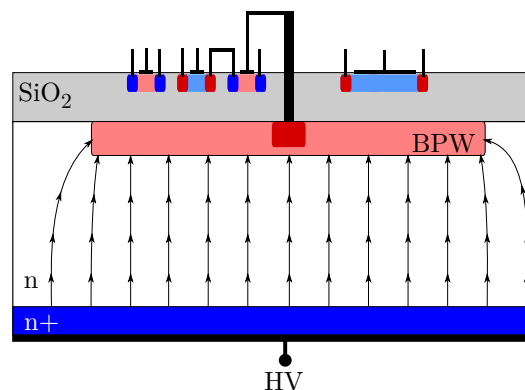


FIGURE 2.3: Sketch of the SOI structure with a BPW layer used to shield the readout electronics from the sensor bias voltage.

### 2.3.7 Radiation hardness

Radiation hardness is another very important parameter that has to be concerned in terms of some specific areas of the SOI devices utilization (for example the military or aerospace applications). It is also one of a key limitations for the applications in highly radiative environments of high energy physics experiments.

There are two major categories of ionizing radiation related issues: Single Event Effects (SEE) and Total Ionization Dose (TID) effects. In general the first group covers all the immediate consequences of the particle passage through the electronics, whereas the second one deals with the long term device parameters modifications. Their influence on the SOI wafer is schematically presented in Fig. 2.4.

The Single Event Effect occurs when a high energy particle or a gamma ray ionizes the electronics active layer. The highly localized charge carriers created in the sensitive device regions may cause an incorrect circuitry behaviour or can even lead to its irreversible damage. Several types of the SEE can be distinguished according to the effects that they cause.

Probably the least harmful is the Single Event Transient (SET) which reveals as a fake signal travelling through the circuitry. This effect may of course lead to a failure behaviour but does not cause any permanent damage. After the fake signal has been propagated, the proper chip operation is restored.

Another type is the Single Event Upset (SEU) that corresponds to the change of the state saved in the memory cell. The consequences of SEU are highly determined by the memory cell purpose. It may have a minor consequence when for example some data storage cell is harmed, but on the other hand when a control bit is flipped the chip operation can be switched into an improper mode or even stopped. Nevertheless, SEUs do not introduce any irreversible changes into the circuitry itself, in the worse case they may extort chip reconfiguration or power cycling to recover.

Finally, the issue that may cause an irreversible change is called the Single Event Latch-up (SEL). As the name suggests, it refers to the creation of a latch-up – a forward biased thyristor-like pnpn structure, induced by the ionization. Since the latch-up's are self-biasing, the low resistivity path that they create between two nodes will be maintained until switching off the device. Moreover, the currents flowing through this parasitic path may be high enough to permanently damage the device.

There are several methods to cope with the SEE issues. Probably the most popular one is the triplication of the critical design parts, followed by the voting system. Therefore even if some kind of issue appears in one part of the circuitry, the other two will remain unaffected and the voting will provide the proper information. This solution highly increases the chip power consumption as well as its area.

Fortunately, the electronics fabricated on the SOI structure is highly resistant to any kind of the SEE issues and does not require any special treatment. Thanks to the full isolation of each transistor it is totally immune to the SEL effect. In case of SET and SEU effects the probability of its occurrence is significantly reduced in comparison with the standard bulk CMOS. This is a direct implication of the low thickness of the top silicon layer, that reduces the volume in which the ionization may occur. This SOI feature makes it a perfect candidate

for all the applications that have to cope with cosmic radiation and require a high reliability. These are for example the space probes or satellites that once launched do not allow for any maintenance. It is also a very desired feature in terms of usage in any kind of aircraft's or spacecraft's.

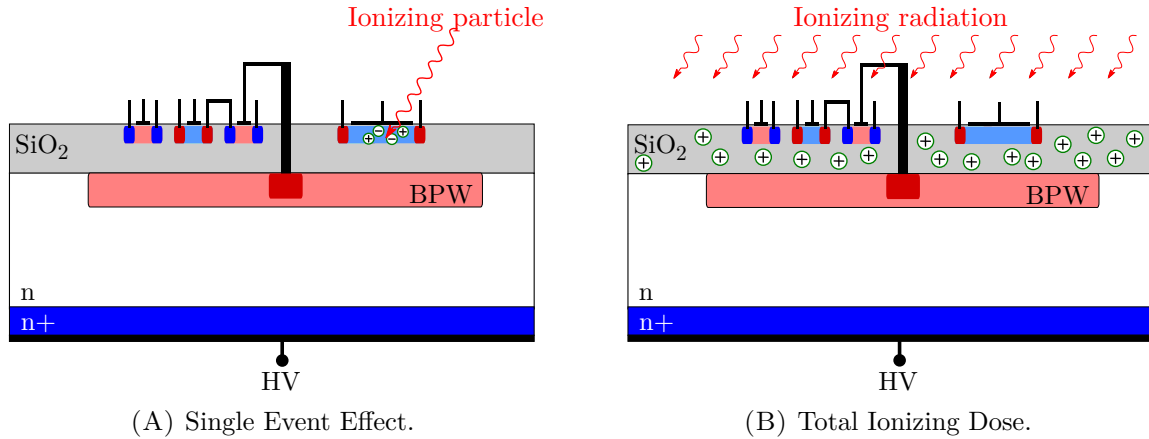


FIGURE 2.4: Schemes showing two main categories of the ionizing radiation damages to the SOI structure.

Unfortunately, the SOI does not show a similar immunity to the Total Ionizing Dose issues, what is worse, it is even much more vulnerable to this kind of effects than a standard CMOS structure. To explain the reason of this, one has to examine how does the long-term ionization affects the CMOS devices. There are several processes that contribute to the behaviour of irradiated MOSFET's but they all originate from the presence of the silicon dioxide in its structure. When the ionization takes place within  $SiO_2$ , electron-hole pairs are created and some fraction of them will recombine almost immediately, but the rest will remain. Since there is a huge difference in the mobility of the electrons and holes in silicon dioxide, in favour of the former, the electrons are swept out of the insulator layer within a nanoseconds or less. Whereas the holes mobility is so low that they remain almost immobile. Overall, this leads to accumulation of a positive charge in the  $SiO_2$  which results in a threshold voltage shift of a MOS device [29].

Another process that has similar consequences is a radiation induced build-up of relatively long-living trap states at the  $Si/SiO_2$  interface, which can remain for hours or years. Such states may be occupied by the holes that have almost escaped from the silicon dioxide or the ones created directly in its vicinity. Nevertheless, the holes trapped in these states are exposed to the annealing process which allows for a gradual recovering after the irradiation.

Bulk CMOS is also affected by this process but on much lower scale. The most vulnerable region in modern CMOS technologies is Shallow Trench Isolation (STI). This refers to the insulator layer that surrounds each transistor and ensures their separation. It is also formed by the silicon dioxide, so it also gathers the positive charges, but because of the side location of the STI its influence is less harmful (comparing to the contribution from the BOX layer in the SOI structure).

In standard CMOS there are several techniques that allow for the radiation-hardening of the circuitry. Predominantly utilized one is the usage of Enclosed Layout Transistors (ELT) instead

of the “classical” ones. In the ELT devices the drain implantation is located in the center of the transistor structure, which is then encircled by the gate, and the gate is further enclosed by the source region. Such a solution moves the STI region away from the transistor channel proximity and thus suppresses its negative influence. It should be also pointed out that the direction of the CMOS technology development is somehow in-lined with its radiation hardening. As the miniaturization process proceeds, the gate oxides becomes thinner, which directly reduces the volume of TID sensitive insulating layer. Moreover, in the smallest technology nodes the gate insulation is so thin that a tunnelling processes starts to take place which increases the probability for holes trapped within  $SiO_2$  recombination.

All the solutions devoted to the bulk CMOS, have similar effects also on the SOI MOS-FET's. Unfortunately, SOI devices are mostly affected by the thick insulator layer located just beneath the top silicon, and none of the standard methods suppresses this influence. Therefore the standard SOI electronics is very prone to the TID radiation effects. To overcome this issue a SOI structure modification, called Double SOI (DSOI), has been proposed [30].

## 2.4 Double SOI

Double SOI structure is presented in the Fig. 2.5A. It is obtained by repeating the SOI fabrication process twice on the same handling wafer, therefore between the top silicon layer dedicated for the electronics and the handle wafer there is additional isolated thin middle silicon layer (MidSi). Such solution introduces several new capabilities, especially in terms of detector applications. The existence of additional conducting layer (with relatively low resistivity) between the sensor and the electronics provides an easy way to shield the circuitry from the negative influence of a back-gate effect. When grounded, this layer prevents the interaction between the radiation sensitive volume and the readout electronics. Moreover, by use of the middle silicon layer for shielding, the restrictions on the sensing node dimensions (explained in section 2.3.6) are no longer valid. Therefore the sensor capacitance can be reduced and its shape may be designed independently from the readout.

Although the electronics shielding ensured by the Double SOI structure is highly beneficial, its main power revels in terms of radiation hardening. The middle silicon layer provides the possibility to overcome the SOI weakest point, which certainly is the TID vulnerability. In Double SOI the influence of the positive charge trapped within BOX layer may be compensated by applying the appropriate negative voltage to the MidSi layer, as shown in Fig. 2.5B. The compensation voltage may constantly follow the dose and thus restore the initial transistor threshold voltage. The results presented in [30] show transistors performance irradiated up to 2 MGy and the SOI detector system maintaining its pre-irradiation capabilities up to 500 kGy.

## 2.5 Lapis Semiconductor process

The Lapis Semiconductor is a Japanese semiconductor manufacturer, which services have been exploited for the scope of the presented thesis. The company was established in 2008 as a spin-off of the OKI Electric Industry Company. Lapis products, which are mainly digital

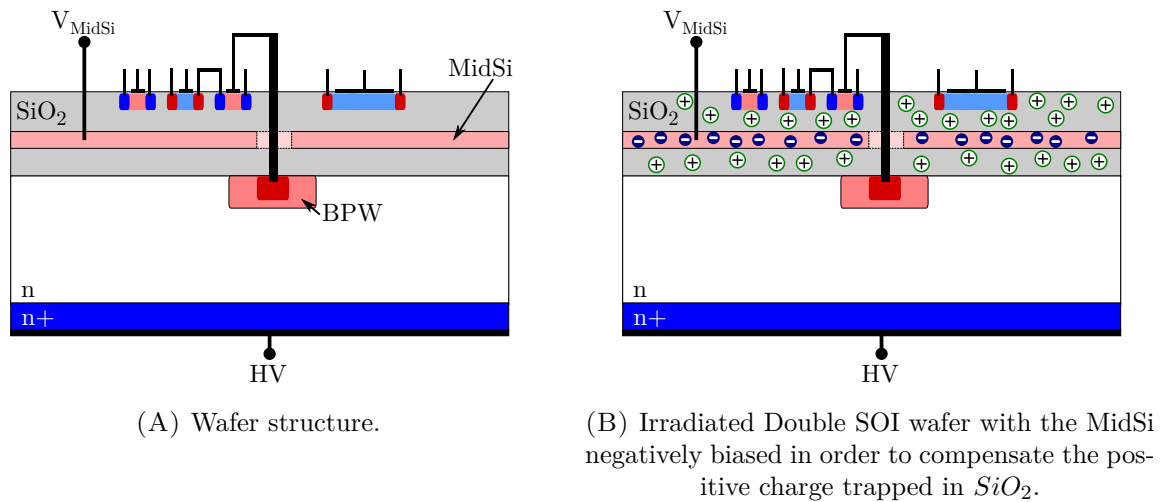


FIGURE 2.5: Schemes showing the Double SOI structure and its utilization for the radiation hardening.

LSI's such as memories, display drivers, logic IC's (Integrated Circuits), are available on the global market. Despite of its commercial activity Lapis provides the 200 nm Fully-Depleted SOI CMOS technology for the scientific applications. The company remains in collaboration with the Japanese High Energy Accelerator Research Organization (KEK).

To provide the possibility for the monolithic radiation detectors manufacturing, Lapis has adopted their process line. They offer several buried wells of different doping concentrations located at different depths of the handle wafer as well as the connection via to the substrate, which are necessary to form a sensing diode.

For the scientific purposes Lapis utilizes the SOI wafers provided by the French company Soitec, which is manufacturing them using the *Smart Cut* technique. Since for the semiconductor detectors the silicon quality is crucial, Lapis decided to offer their products fabricated on different types of substrates. The available wafer types are:

**CZ(n)**  $n$  doped substrate obtained by the Czochralski method, with declared resistivity higher than  $700 \Omega \text{ cm}$ ,

**FZ(n)**  $n$  doped substrate obtained by the Floating Zone method, with declared resistivity higher than  $2 \text{ k}\Omega \text{ cm}$ ,

**FZ(p)**  $p$  doped substrate obtained by the Floating Zone method, with declared resistivity higher than  $4 \text{ k}\Omega \text{ cm}$ ,

**DSOI(p)**  $p$  doped Double SOI wafer, with the substrate obtained by the Floating Zone method, which declared resistivity is higher than  $1 \text{ k}\Omega \text{ cm}$ .

The availability of different substrates does not only provide a flexibility in the choice of the most appropriate sensor for specific application. It is also very useful for the studies of coupling between the electronics and the sensor. Testing the performance of prototypes having exactly the same readout electronics, but fabricated on different substrates helps in in-depth understanding of detectors behaviour.





## Chapter 3

# INTPIX6 detector studies

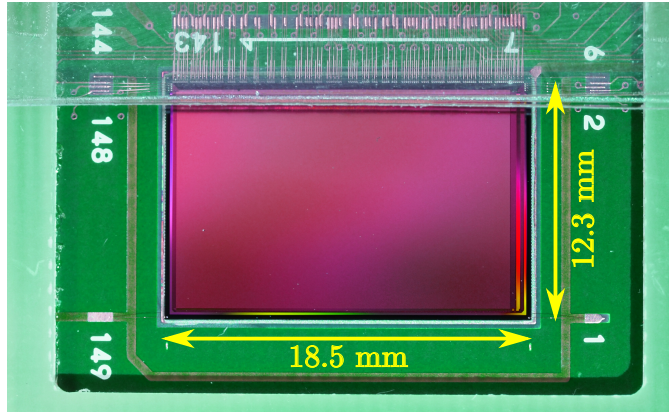
The INTPIX6 detectors represent the sixth generation of the large area, general purpose INTegration type PIXels (INTPIX) family, which are being developed by the Japanese group from KEK under the supervision of Yasuo Arai [31, 32]. The development of the INTPIX detectors has been started in early 2000 and is still ongoing. Successive prototypes and their measurements provided a lot of informations essential to understand the behaviour of monolithic detector based on the SOI technology. For example, a back gate effect was studied with the second generation of INTPIX detectors and provided the knowledge necessary to overcome this issue [30, 33]. Since the KEK group cooperates with the foundry, all informations are beneficial not only for the guidance in the electronics design but also for the modifications of the process itself. The INTPIX6 detector was fabricated on few different wafer types and thanks to the close collaboration with KEK, few prototypes of CZ(n) and FZ(n) devices together with the readout boards were sent for measurements to AGH University.

### 3.1 INTPIX6 architecture

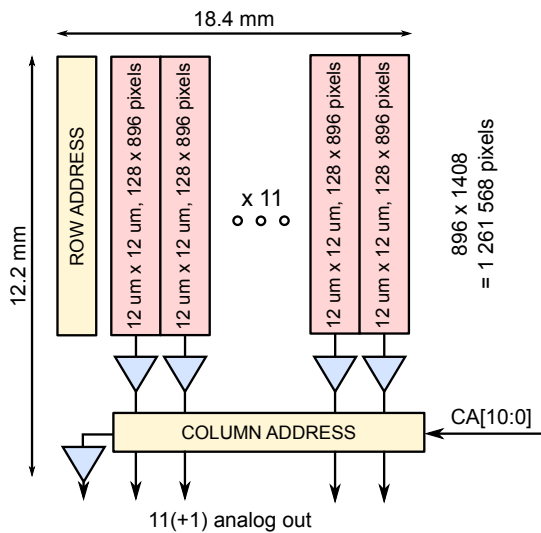
The INTPIX6 detector prototype wire-bonded to the test board is presented in Fig. 3.1A. The chip size after dicing is  $18.5\text{ mm} \times 12.3\text{ mm}$ , with the sensitive area of  $16.9\text{ mm} \times 10.75\text{ mm}$ , which is about 80% of the whole detector. The pixel matrix consists of  $1408 \times 896$  square pixels,  $12\text{ }\mu\text{m} \times 12\text{ }\mu\text{m}$  each. The matrix is logically segmented into eleven blocks of  $128 \times 896$  pixels to provide the possibility of parallel readout of each block to reduce the readout time. The schematic block diagram of the INTPIX6 chip is presented in Fig. 3.1B. The peripheral circuitry is reduced to the necessary minimum, which is the row and column decoders, biasing block and output buffers driving analog signals out of the chip. Regarding the in-pixel readout circuitry, in the input stage there is a pMOS transistor in the source-follower configuration with two gain settings, followed by a simple sample and hold block based on a storage capacitor. The schematic view of the in-pixel circuitry is shown in Fig. 3.1C.

The matrix readout can operate either in a global shutter mode or in a rolling shutter mode. In the global shutter mode the integration period is common for the whole matrix, whereas in the rolling shutter mode the integration periods are different for different matrix sub-parts (usually for each row). Since in the rolling shutter mode the integration period is limited by the readout speed all measurements results presented in this thesis are obtained with the global shutter mode in which the integration time can be set independently. Moreover, unless

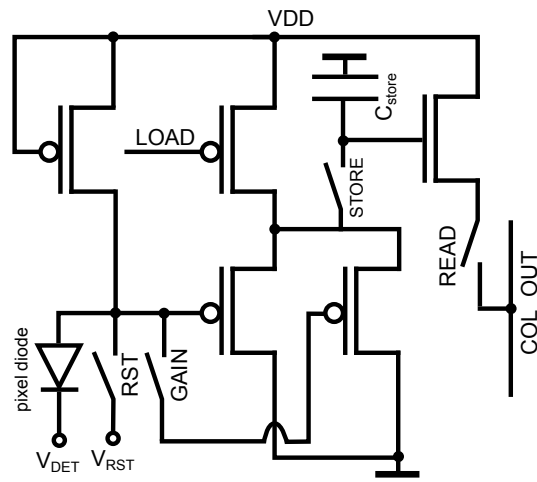
otherwise stated, most of the measurements were performed with the region of interest (ROI) limited to the matrix sub-part of  $256 \times 256$  pixels, which was motivated by the reduction of the readout time.



(A) Photograph of prototype assembled to the test board.



(B) Block diagram of the readout electronics.



(C) Schematic of the in-pixel circuitry.

FIGURE 3.1: INTPIX6 detector.

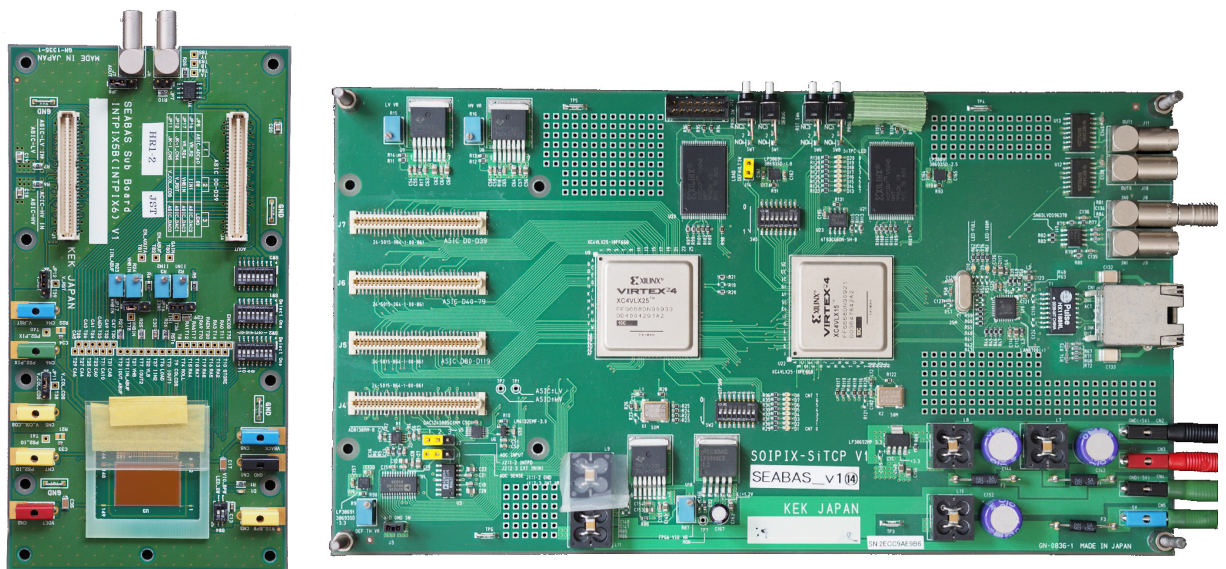
## 3.2 Measurement setup

To carry out the measurements of the INTPIX6 chip the SEABAS (Soi EvAluation BoArd with Sitcp) readout board was used. Each detector chip was glued and wire-bonded to the dedicated small chip board compatible with the SEABAS board, which allows for a fast and easy assemblies replacement without the need of separate readout board for each prototype. The role of this separate chip board is practically limited to routing all of the signals from the chip to the appropriate SEABAS board ports, whereas the whole functionality is moved to the readout board. The INTPIX6 chip board and the SEABAS readout board are presented in Fig. 3.2A and Fig. 3.2B respectively.

A heart of the SEABAS boards are two Virtex4 FPGAs (Field-Programmable Gate Array): the first one is dedicated to the user defined chip communication, data taking and buffering, the second one is responsible for establishing a TCP/IP (Transmission Control Protocol/Internet Protocol) connection and sending the data to PC. Beside that there are several DACs (Digital to Analog Converter) providing biasing currents and voltages and a multi-channel 12-bit ADC (Analog to Digital Converter) for digitalization of all analog outputs.

A dedicated data acquisition software and FPGA firmware were also developed by the group from KEK and provided together with the readout board. The data acquisition software (DAQ) utilizes ROOT Data Analysis Framework [34] to create a simple graphical user interface (GUI), establish TCP/IP sockets for connection with the board, interpret the incoming data and save them in a TTree (data container type) for the offline analysis. It provides all functionalities required for the chip configuration: preparation of an appropriate command sequence necessary to set up a desired chip operation mode, adjustment of all biasing voltages and currents, controlling the matrix timing settings and selecting the region of interest. Additionally, through the GUI one can also control the data acquisition itself by setting up a number of frames to be measured, data file name and its path. Beside that, it assures basic online data quality check, thanks to the possibility of online monitoring of every n-th frame and its basic properties (for example the mean value of pixels amplitudes).

The INTPIX6 detector is sensitive to a visible light therefore all the measurement have to be performed in light sealed environment. For this reason the readout board and chip board were always placed in a metal box.



(A) INTPIX6 chip board.

(B) SEABAS readout board.

FIGURE 3.2: Photograph of the readout boards used for the INTPIX6 detector measurements.

### 3.3 Data processing and analysis flow

The data analysis software for hit reconstruction was not provided by the KEK group. Therefore, a dedicated analysis chain was developed by the author of this thesis. Since raw data are stored in ROOT files the analysis software was also implemented basing on ROOT6 libraries. The main steps of the data evaluation process and the functionality it provides are discussed below.

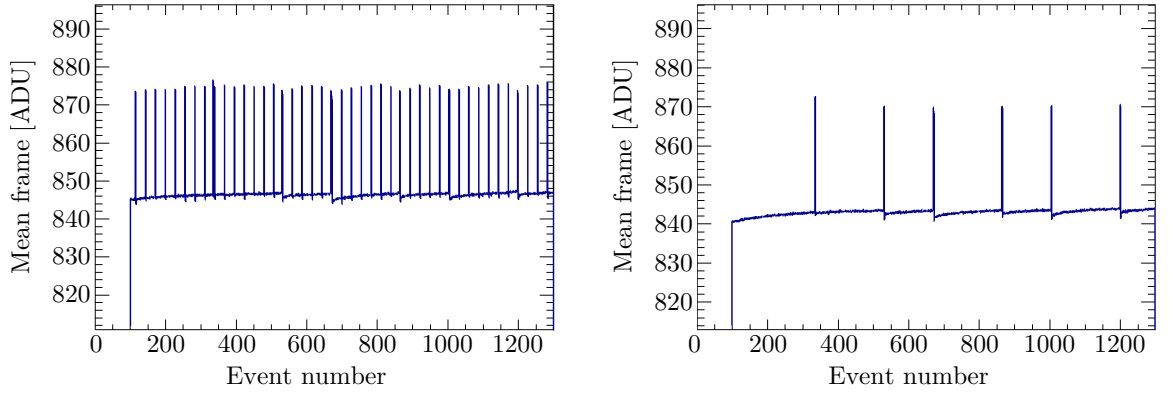
- **Raw data reader**

To perform the analysis an appropriate input file has to be loaded. Each measurement saves the separate file comprising a single ROOT TTree container, which holds several leafs (representing certain variable) carrying basic informations about chip configuration and the main leaf with the 2D array containing raw signal amplitude value of each pixel. Therefore each consecutive event in the tree represents a single frame. Each data file consists of several thousands of “calibration” data (taken without any radiation source) and “true” data taken with the signal source.

- **Bad frames rejection**

The first step before the analysis is the bad frame rejection, which was added to the analysis flow after spotting an issue with the readout. It was observed that some frames have significantly increased mean frame value  $M_{\text{Frame}}$  (mean value of the amplitudes collected by each pixel in single frame). The example plot showing the mean frame value for the “calibration” events sample is presented in Fig. 3.3A, where all the “spikes” correspond to the mentioned issue. It was also noticed that the frequency of these “spikes” depends on the speed of the link between the readout board and the PC. Fig. 3.3A and Fig. 3.3B show a comparison of two similar samples taken with different settings of the online data quality monitoring. During the data-taking of the sample shown in Fig. 3.3A the data quality checks were done every 1 s, whereas for the sample shown in Fig. 3.3B every 100 s. Since the DAQ software is single-threaded, the time needed for computations related with data quality checks slows down the link throughput, which directly reflects in more frequent buffer overloading. This was further leading to the disturbance in the timing of control signals in given frame, which reveals in highly increased mean frame value. In the end, to minimize this issue the data were taken with the lowest frequency of online quality checks, but even then some frames were still affected, therefore a bad frame rejection algorithm was implemented. For this purpose the mean value of mean frame  $\langle M_{\text{Frame}} \rangle$  over the whole data sample and its standard deviation  $\sigma_{M_{\text{Frame}}}$  are calculated. A frame is marked as a “bad” one and rejected from the further analysis if its mean value is more than three sigma away from the mean value of all frames:

$$| M_{\text{Frame}} - \langle M_{\text{Frame}} \rangle | > 3 \cdot \sigma_{M_{\text{Frame}}} \quad (3.1)$$

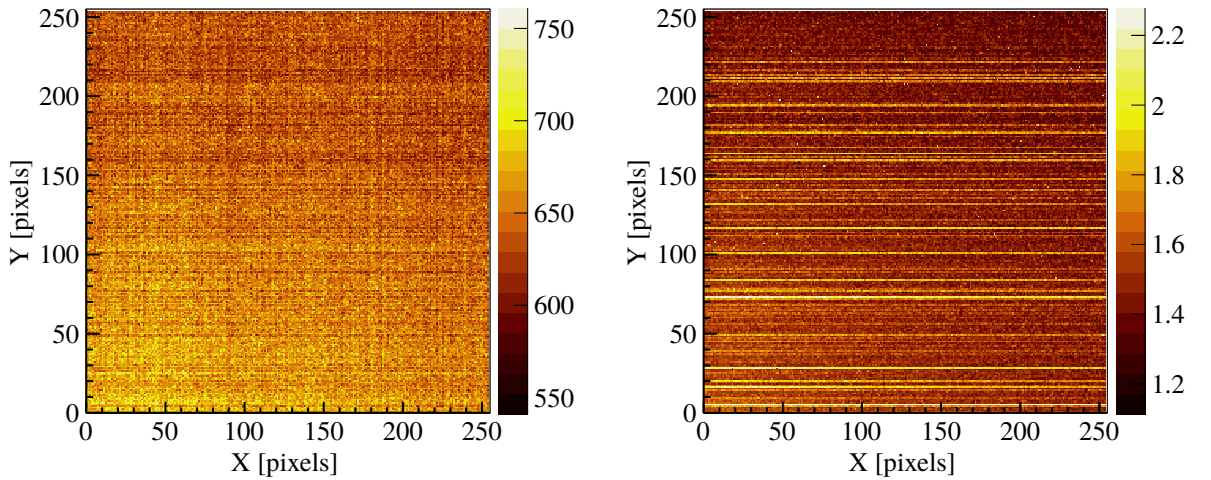


(A) Data quality checks repeated once per second. (B) Data quality checks repeated once per one hundred seconds.

FIGURE 3.3: Plots showing the mean frame values in consecutive frames for the “calibration” events sample at two different frequencies of data quality checks. Observed spikes indicate improper readout behaviour.

#### • Pedestal and noise calculation

The core of the analysis starts with estimation of the pedestal and noise values for each pixel in the matrix. These parameters are extracted from the “calibration” sample. For each single pixel a separate histogram is created and filled with its measured raw signal amplitudes. The mean value of this distribution is the pixel pedestal  $P[i][j]$  and its standard deviation the pixel noise  $\sigma[i][j]$  (where  $i$  is row number and  $j$  is column number). The examples of plots showing the pedestal and noise distribution over the matrix are presented in the Fig. 3.4A and Fig. 3.4B. On the noise distribution one can easily spot that for several rows the noise is notably increased. The origin of such behaviour has been studied but unfortunately the conclusive explanation of this issue was not found.



(A) Pedestal map  $P[i][j]$ .

(B) Noise map  $\sigma[i][j]$ .

FIGURE 3.4: Plots showing map of the pedestal and noise distribution over the INTPIX6 matrix given in ADC counts (ADU). Results obtained with the INTPIX6 detector fabricated on CZ(n) wafer.

### • Signal extraction

The next step in the analysis is the signal extraction. A pixel signal  $S[i][j]$  is basically obtained by subtracting the pedestal value from the raw amplitude recorded by each pixel in a given frame. The correctness of this algorithm can be cross-checked by plotting the pixels signal spectrum for the “calibration” data. Since these data do not contain any “true” signal, the signal spectrum should undergo a Gaussian distribution centred around zero with the standard deviation equal to the pixel noise value. The plots showing the pixel signal spectrum for whole “calibration” sample and the pixel noise distribution are shown in Fig.3.5A and Fig.3.5B respectively.

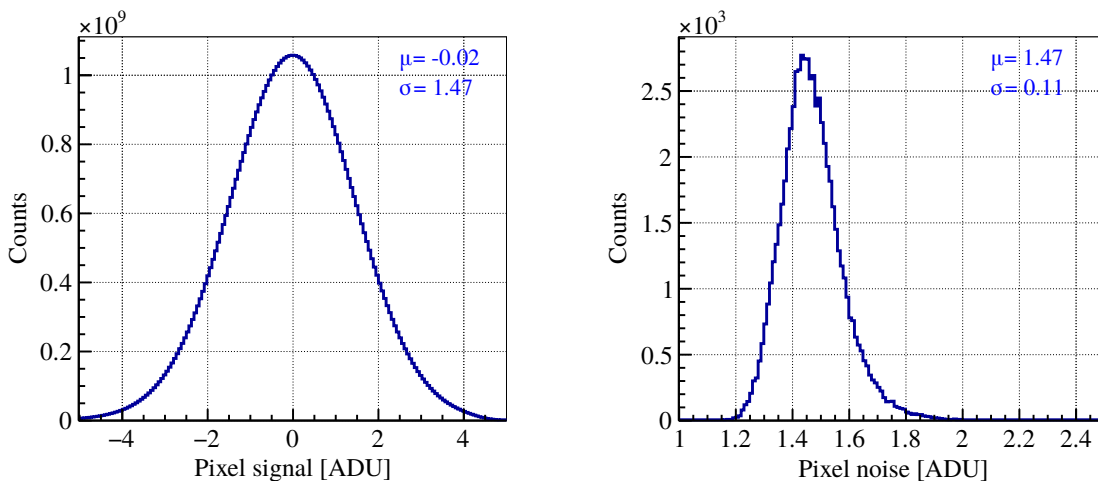
The signal spectrum changes significantly for the “true” data where an external signal source distorts symmetrical Gaussian shape by introducing a long tail towards the higher signal values. The examples of plots showing the pixel signal map for the “true” data frame and the corresponding signal spectrum are presented in Fig.3.6A and Fig.3.6B.

### • Clusterization

The total signal generated by a single particle may be splitted over more than one pixel, so to extract its energy a clusterization algorithm has to be introduced. In the presented analysis a procedure based on two threshold levels was implemented. In the first step the signal map is scanned to find a pixel which signal ( $S[i][j]$ ) exceeds the seed threshold. The threshold value ( $th_{seed} \cdot \sigma[i][j]$ ) is usually expressed in terms of pixel noise what means that a pixel has to have the signal larger than  $th_{seed}$  times the pixel noise to be taken as a seed:

$$S[i][j] > th_{seed} \cdot \sigma[i][j] \quad (3.2)$$

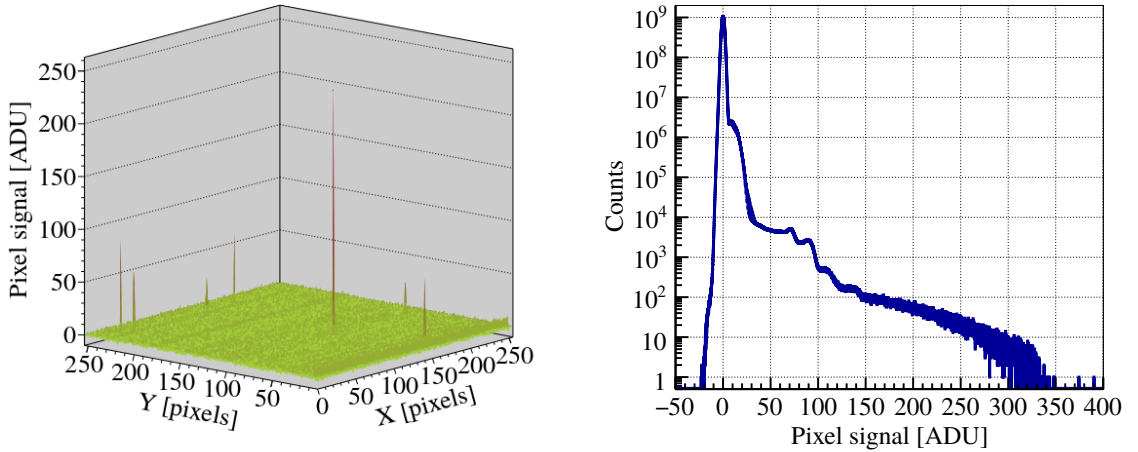
The specific threshold value has to be adjusted depending on the measurement condition or detector performance. It must be large enough to reject noise entries, but at the same time low



(A) Spectrum of the pixel signal  $S[i][j]$ , combined for all pixels in the matrix.

(B) Spectrum of the pixel noise  $\sigma[i][j]$ .

FIGURE 3.5: Plots showing spectra of the pixel signal and the pixel noise for the “calibration” data sample. Obtained with the INTPIX6 detector fabricated on CZ(n) wafer.



(A) Pixel signal  $S[i][j]$  map from a single frame. (B) Pixel signal  $S[i][j]$  spectrum, combined for all pixels in the matrix.

FIGURE 3.6: Plots showing the pixel signal map and the pixel signal spectrum for the “true” data sample taken with the  $^{241}\text{Am}$  radiation source. Obtained with the INTPIX6 detector fabricated on CZ(n) wafer.

enough in order not to lose the particle related hits. Since the INTPIX6 detector show very good noise performance it was easy to separate the signal from the noise and the seed threshold setting was rather arbitrary. For the presented analysis it was typically set to  $th_{\text{seed}} = 10$ .

After finding the seed, all pixels around it are checked with the different threshold condition:

$$S[i][j] > th_{\text{neighbour}} \cdot \sigma[i][j] \quad (3.3)$$

The threshold for the neighbouring pixels  $th_{\text{neighbour}}$  is less restrictive and its typical value in the analysis was  $th_{\text{neighbour}} = 2$  which was found to be an optimum. The value of this parameter has direct influence on the detector energy resolution because too large  $th_{\text{neighbour}}$  increases the amount of the missing energy, whereas its too low value increases the probability for adding a noisy pixel into the cluster.

The searching for neighbours is repeated around any new pixel added into the cluster and ends when there are no more pixels fulfilling the neighbour criteria in the vicinity of the current cluster. When the full cluster is found, it is stored and its main parameters (such as total energy or cluster size) are extracted. After that the procedure returns to search for a new seed pixel in the current frame but excluding all already clustered pixels.

- **Data selection**

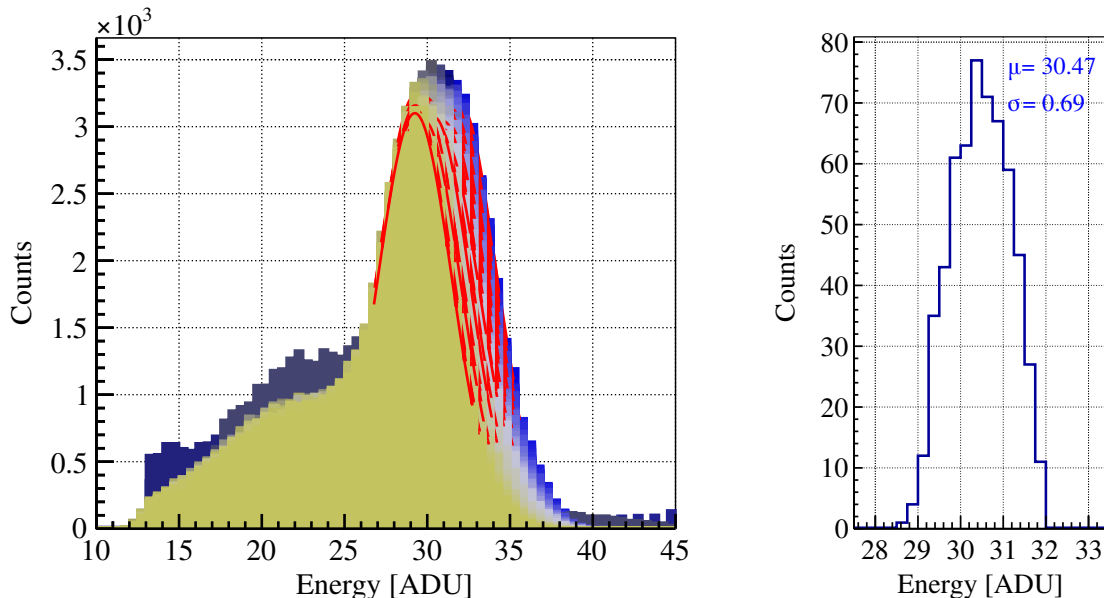
For the clusters reconstructed on the edge of the matrix it may happen that only part of the signal is recorded. Since this would naturally affect the energy reconstruction, all the clusters containing the boarder pixel are discarded from the further analysis.

- **Gain uniforming**

When a representative data set is selected, the cluster energy spectra plots can be drawn and the detector performance may be verified. However, this merges the informations from all pixels in the matrix, which means that any differences between pixels will have negative effect

on the overall performance. Therefore, to obtain the best results, limited only by the inherent noise, one should also apply a correction for the pixel to pixel gain variations or ensure that this variations are negligible. For the INTPIX6 detector a strange behaviour was already observed on the pedestal map (see Fig. 3.4A) where one can notice gradient starting from the bottom left corner (pixel (0,0)) towards the upper right corner (pixel (255,255)). It was also proven that this pattern does not come from the pixels themselves. Benefiting from the fact that the matrix ( $1408 \times 896$  pixels) is much larger than the chosen region of interest ( $256 \times 256$  pixels) it was confirmed that the pattern remains the same irrespective of the chosen region. Therefore this effect had to be attributed to the readout issue. Since the matrix operates in a snapshot mode and all pixels are serialised into a single analog output, each pixel “waits” for a different period of time to be read out. Since the charge information is stored on pixel as a voltage across a capacitor, therefore any leakage current is going to change its amplitude over the time. This mechanism fits perfectly to the observed behaviour where the first read out pixel (0,0), has the highest pedestal, whereas the last one (255, 255) has the lowest.

The described mechanism does not directly implicate the gain variations between pixels. If the leakage currents are constant despite of the voltage across the capacitance, then the absolute measured values will still be affected but after pedestal subtraction it should cancel out, leaving the gain uniform over the whole matrix. Whereas, if the leakage current depends on the voltage level, then for the pixels containing the signal the voltage drop on the capacitance will be different than the voltage drop for the same pixels but without the signal (like during the pedestal measurement). Therefore, it will result in the decrease of the effective gain for pixels waiting longer to be read out.



(A)  $^{55}\text{Fe}$  spectra with the Gaussian fit around the  $^{55}\text{Fe}$  peak (different colors represent different cells). (B)  $^{55}\text{Fe}$  energy peak position distribution.

FIGURE 3.7:  $^{55}\text{Fe}$  spectra and  $^{55}\text{Fe}$  peak position plotted separately for different  $10 \times 10$  pixels cells to confirm the need for per-pixel gain uniforming. Obtained with the INTPIX6 detector fabricated on CZ(n) wafer.



To check which case is valid for the given prototype one needs to perform the measurement with physical signal source, and check if the extracted signal amplitudes vary depending on the hit position. For this purpose the  $^{55}\text{Fe}$  source was used. This source mainly emits soft X-rays of energy  $E_{^{55}\text{Fe}}^{K\alpha} \simeq 5.9\text{ keV}$ , which during top illumination penetrates only several micrometers of the detector. Because of to that, the vast majority of the reconstructed clusters are single pixel clusters, meaning that the whole hit energy is gathered by a single pixel, providing perfect conditions for the single pixel gain estimation.

To obtain statistics high enough to become insensitive to random fluctuations the whole region of interest was divided into a smaller  $10 \times 10$  pixels cells and the measured energy distributions for each cell were processed separately. Fig. 3.7A and Fig. 3.7B shows the  $^{55}\text{Fe}$  spectra and  $^{55}\text{Fe}$  peak position distribution respectively. One can notice that there is a shift in the relative spectra position depending on cell position. It leads to the dispersion of the reconstructed energy peak on the level of 0.68 ADU. The differences between peak positions were then used to estimate the gain correction factors for each pixel. For that purpose a plane function is fitted to the histogram of a normalized nonuniformity in the detector response, with respect to the cell position (shown in the Fig. 3.8).

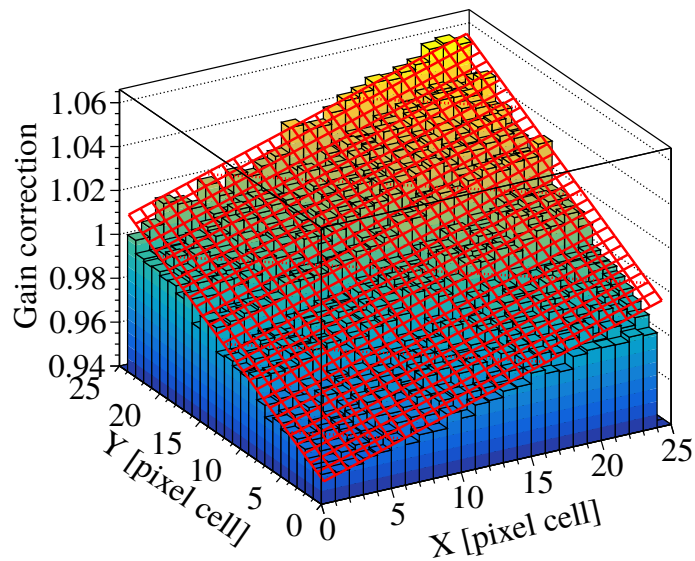
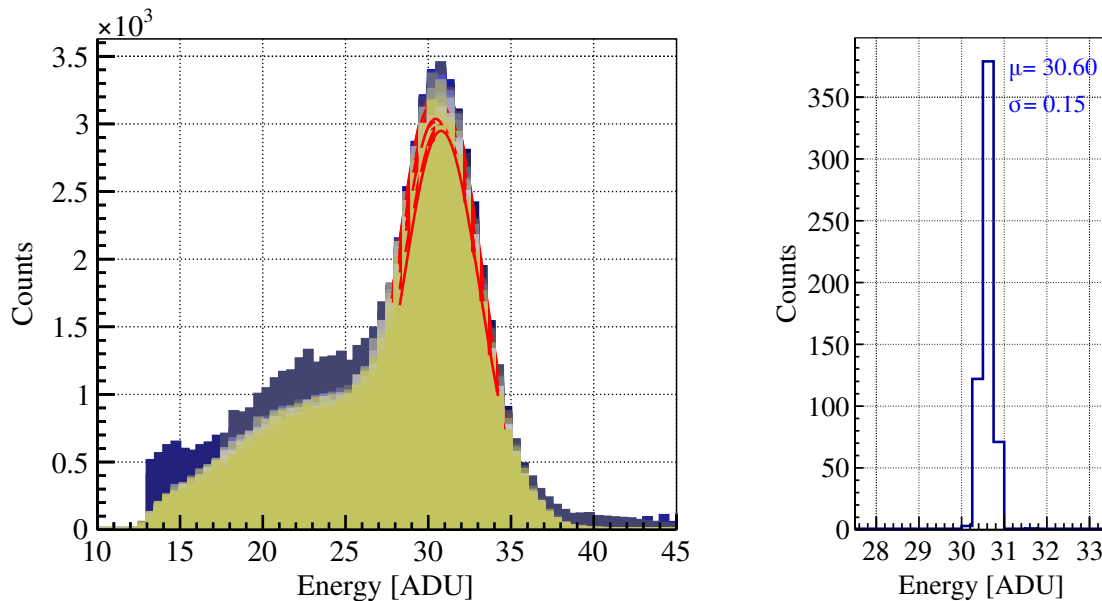


FIGURE 3.8: Normalized non-uniformity of the detector response with respect to the cell position (color bar histogram) with the fitted plane (red grid). Obtained for the INTPIX6 detector fabricated on CZ(n) wafer.

Using the fitted function a gain correction factor was obtained for each pixel. The results after applying the correction factor are shown in Fig. 3.9A and Fig. 3.9B where the spectra for each cell and  $^{55}\text{Fe}$  peak position distribution are presented. Now, independently on the cell position, each spectra is centered around the same mean value and the peak position distribution is much more narrow than before the correction, with the dispersion on the level of 0.15 ADU (4.5 times lower).



(A)  $^{55}\text{Fe}$  spectra with the Gaussian fits around the  $^{55}\text{Fe}$  peak (different colors represent different cells). (B)  $^{55}\text{Fe}$  energy peak position distribution.

FIGURE 3.9:  $^{55}\text{Fe}$  spectra and  $^{55}\text{Fe}$  peak position plotted separately for different  $10 \times 10$  pixels cells after applying the gain uniforming algorithm. Obtained with the INTPIX6 detector fabricated on CZ(n) wafer.

### 3.4 Measurements results

After the analysis flow had been set up, a set of measurements dedicated to characterize the performance of the chip was performed. For this purpose two radioactive sources were used as a signal source:  $^{241}\text{Am}$  and  $^{55}\text{Fe}$ . The  $^{241}\text{Am}$  source was chosen to perform the detector calibration because it has six main, well separated lines distributed over a quite large energy range (covering the energies from around 10 keV up to almost 60 keV).

All measurements (unless otherwise stated) were performed in very similar, stable conditions at ambient temperature of  $23^\circ\text{C}$  with the sensor biased at 100 V and with integration time set to  $10\ \mu\text{s}$ . Moreover, most of the measurements were carried out for two different sensor wafer types: Floating Zone n-type – FZ(n) and Czochralski n-type – CZ(n). For the clarity, all the intermediate results of the analysis process are shown in details for the CZ(n) wafer only, whereas the final conclusions are presented for both assemblies. The complementary plots for FZ(n) are presented in the Appendix A.

### 3.5 Detector calibration

The detector calibration requires the estimation of the conversion ratio from the arbitrary energy units expressed in ADC counts into the absolute energy, usually expressed in electronvolts. In this approach all the fragmentary coefficients such as the mean energy needed for an  $e-h$  pair production, pixel input stage conversion coefficient or readout chain amplification are combined together into one effective conversion ratio  $G$ . Moreover, if radiation source provides

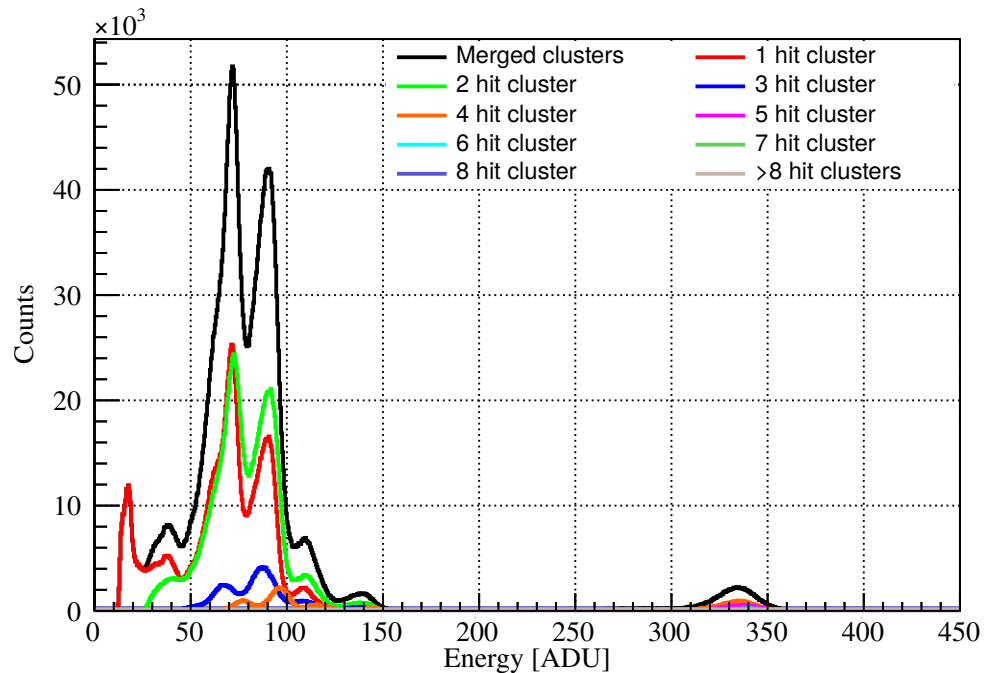


FIGURE 3.10: Combined spectrum shown in black, whereas individual contributions from clusters of certain size presented in different colors.

more than one energy line (within the acceptance of the detector) not only the conversion ratio can be found but also its linearity over certain energy range can be checked.

An example of energy spectrum obtained from the measurement with the  $^{241}\text{Am}$  source is shown in Fig. 3.10. For the more detailed investigation a separate spectrum formed from the data sub-sample containing clusters of given size is drawn with different color, whereas a combined spectrum is drawn in black. It can be noticed that individual contributions from different cluster sizes have slightly shifted peak values. This is very undesired effect because it broadens the width of the combined peak, which defines the noise performance of the detector.

To investigate the scale of this issue and a method to overcome it, a dedicated analysis was prepared basing on ROOT6 libraries. It utilizes an automatic peak finding algorithm followed by fitting a Gaussian function. An sample plot showing the result of its operation is presented in Fig. 3.11. All founded peaks are marked with the red triangles, and a Gaussian fitted to the highest one is plotted with the red curve. The procedure returns the mean  $\mu$  and width  $\sigma$  (standard deviation) of the fitted function for each peak that was found in the given spectrum. All the constituent spectra were analysed separately and the results are shown in Tab. 3.1.

The origin of the observed discrepancies in the peak positions was attributed to the differences in the missing energy. One can imagine that some part of the carriers induced by the incident photon diffused to the pixels that did not have enough signal to exceed the threshold, causing a reduction of the total measured energy. Such variations will be related to the hit position within the pixel, and so also to the cluster size. For example for hits that occur close to the corners of the pixels it is very likely that each of four pixels near this corner will gather enough energy to be treated as a signal and therefore the significant energy loss is not

Peak number →	1		2		3		4		5		6	
Cluster size ↓	$\mu$	$\sigma$	$\mu$	$\sigma$	$\mu$	$\sigma$	$\mu$	$\sigma$	$\mu$	$\sigma$	$\mu$	$\sigma$
1	37.6	6.63	72.5	5.16	91.1	6.67	112.6	6.80	143.7	5.56	—	—
2	38.5	13.7	73.0	6.50	91.1	7.17	111.7	7.74	141.4	7.96	—	—
3	—	—	69.3	6.70	89.0	7.01	108.9	9.70	139.1	7.40	341.5	11.0
4	—	—	76.8	5.40	95.0	5.64	115.0	7.41	143.0	6.11	336.1	10.6
Combined	37.6	10.1	72.7	6.02	91.2	7.20	111.9	7.70	142.2	7.02	338.7	12.0

TABLE 3.1: Peak positions  $\mu$  and their widths  $\sigma$  for the  $^{241}\text{Am}$  spectra measured separately for contributions from different cluster sizes as well as for the combined one.

expected. On the contrary, for a three pixels clusters it seems very likely that some part of signal reaches also the fourth pixel but not large enough to exceed the threshold, therefore all that part of the energy is lost. This is only a qualitative interpretation but it is in a good agreement with the obtained results, where the highest energy is obtained for the four pixel clusters, while the lowest for the three pixel clusters, and values in between for one and two pixel clusters.

It should also be mentioned, that for photons the cluster shape and the missing energy also highly depend on the depth at which the interaction with the sensor took place. The reasoning presented above is mainly valid for a lower X-ray energies for which the induced signal is relatively low and comes almost only from a shallow penetration. For higher energies, it becomes more likely that interaction occurs also deeper inside the sensor. Therefore, carriers may have more time to diffuse, which naturally enlarges the cluster size. Thus, for the high X-ray energies the individual peaks in the spectrum are additionally smeared, by contributions coming from different interaction depths.

Since there are various effects affecting the measured cluster energy, it is hard to give any quantitative correction procedure, but one should have in mind that there are several mechanisms that affect the measured particle energy and the final spectrum quality is determined not only by the noise of the readout chain.

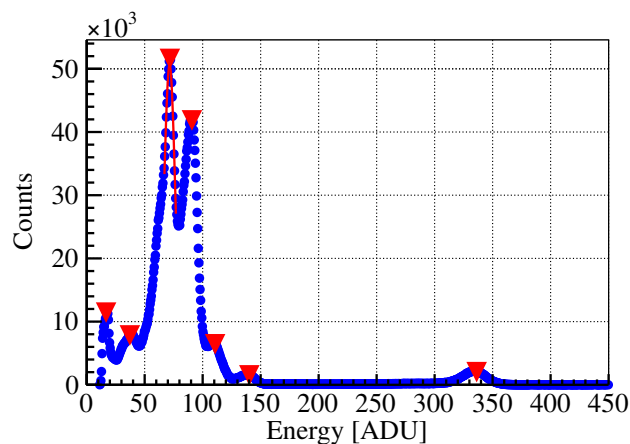


FIGURE 3.11: Result of the peak finding procedure. With the red triangles all found peaks are marked, whereas with the red curve a Gaussian fit to one of them is displayed.

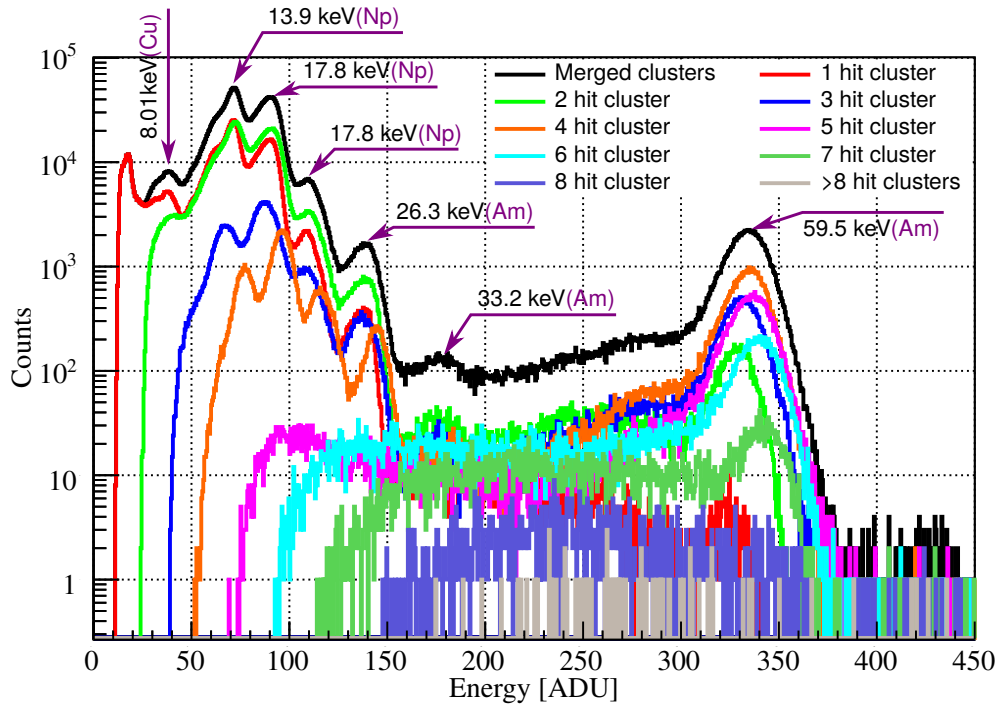


FIGURE 3.12:  $^{241}\text{Am}$  spectrum for CZ(n) wafer with peak attributed to corresponding X-ray energies.

The final  $^{241}\text{Am}$  spectrum for CZ(n) wafer is shown in the Fig. 3.12 with all peaks assigned to the expected X-ray energies. The  $^{241}\text{Am}$  decays into  $^{237}\text{Np}$  which results in six main X-ray energy lines and one characteristic 8.01 keV fluorescence line from copper. After peak identification the calibration curve can be drawn by plotting the measured peak position versus corresponding photon energy. It is shown in Fig. 3.13 together with a linear regression line. The INTPIX6 detector shows good linear behaviour over the whole available energy range with the conversion coefficient  $G = 5.59 \frac{\text{ADU}}{\text{keV}}$ . It is also worth to notice that the y-intercept is equal to  $-2.5$ , which corresponds to the small energy offset below 450 eV.

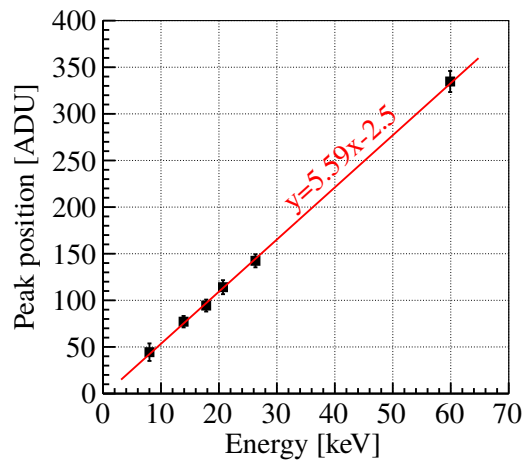


FIGURE 3.13: Calibration curve for INTPIX6 detector showing the peak position in ADC counts versus X-ray energy.

### 3.6 Noise performance

Usually the electronic noise is expressed in terms of voltage and current fluctuations, but for the radiation detector the signal comes directly from the charge induced during the interaction. Therefore, it is very useful to express the detector noise in terms of charge. For that reason a parameter called Equivalent Noise Charge (ENC) was introduced. Equivalent Noise Charge is defined as the amount of charge  $Q_N$ , that introduced to the input of the readout chain as a Dirac delta current pulse  $I(t) = Q_N\delta(t)$  results in the output signal equal to the root mean square value of the readout noise. In other words the ENC is equal to the input charge for which the signal to noise ratio is equal one [17]. Describing the detector noise performance in terms of the ENC allows for direct comparison of different detectors, irrespective of any differences in their designs.

The readout noise distribution is obtained during one of the analysis flow steps (described in Sec. 3.3) and shown in the Fig. 3.5B. The ENC can be calculated by taking the mean pixel noise value of  $\langle\sigma_N\rangle$  together with the previously determined conversion coefficient  $G$  and assuming that 3.6 eV is needed for the e-h pair production:

$$ENC [e^-] = \langle\sigma_N\rangle [ADU] \cdot \frac{1}{G} \left[ \frac{eV}{ADU} \right] \cdot \frac{1}{3.6} \left[ \frac{e^-}{eV} \right] \quad (3.4)$$

The ENC obtained for the CZ(n) wafer type equals to  $73 e^-$ , whereas after applying the same procedure to the data sample taken with the FZ(n) wafer the ENC is even a bit lower on the level of  $70 e^-$ .

There is one more thing concerning the noise performance requiring a supplementary remark. One may already noticed quite a large difference between the pixel noise measured during the calibration which was around 1.5 ADU and widths of the peaks in the  $^{241}Am$  spectrum given in Tab. 3.1 (usually between 6 to 10 ADU). On the first glance this may look suspicious, but one has to remember that the width of the energy peak depends not only on the readout noise. As already mentioned, the whole  $^{241}Am$  spectrum consists of many constituent photon energy levels, therefore it is not possible to extract a single energy line and check its width. Beside that, there is an additional factor coming from the fluctuation of the unmeasured charge (due to its arrival to the pixel that has too low signal amplitude to exceed the threshold). Moreover, for the clusters larger than one pixel, each pixel in the cluster contributes to the overall cluster noise therefore the whole cluster noise is increased.

An additional measurement was performed with the  $^{55}Fe$  source, which has much less complex energy line structure. It has two dominant, closely located  $K_\alpha$  lines at around  $E_{^{55}Fe}^{K_\alpha} \simeq 5.9$  keV and an about ten times less frequent  $K_\beta$  line with the energy of  $E_{^{55}Fe}^{K_\beta} \simeq 6.5$  keV. Therefore, the  $^{55}Fe$  source is much more suitable for estimation of the energy resolution than  $^{241}Am$ . The obtained  $^{55}Fe$  spectrum for the CZ(n) wafer is shown in Fig. 3.14A and Fig. 3.14B, before and after gain correction algorithm application respectively. One can spot the 5% reduction of the peak width thanks to the gain correction. The noise level calculated from the corrected  $^{55}Fe$  peak width corresponds to around  $110 e^-$  which is much closer to the pure pixel noise. This measurement confirms the INTPIX6 detector capabilities in terms of spectroscopy

applications.

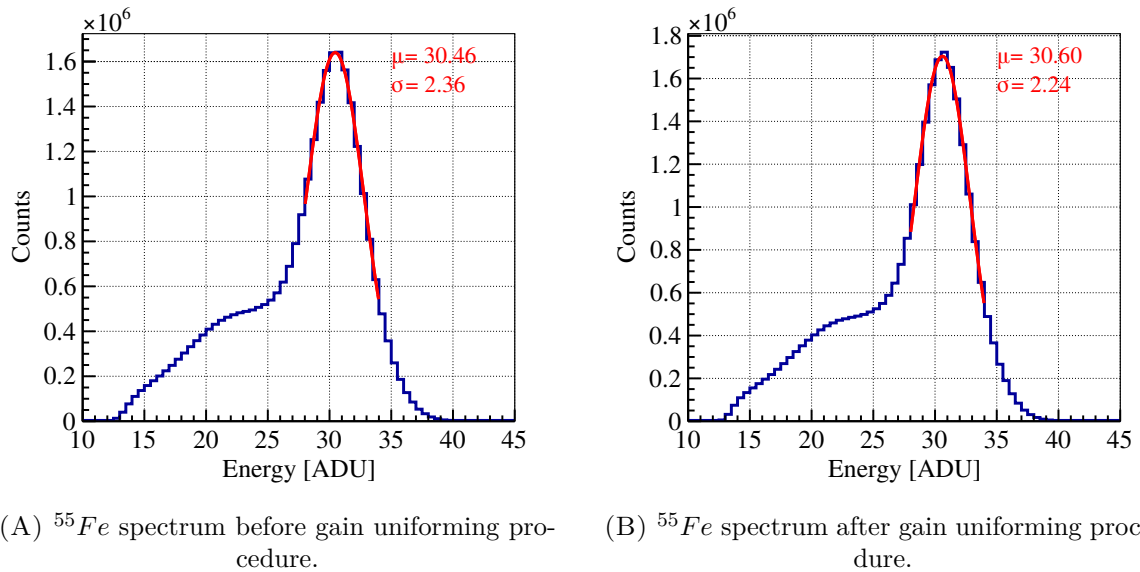


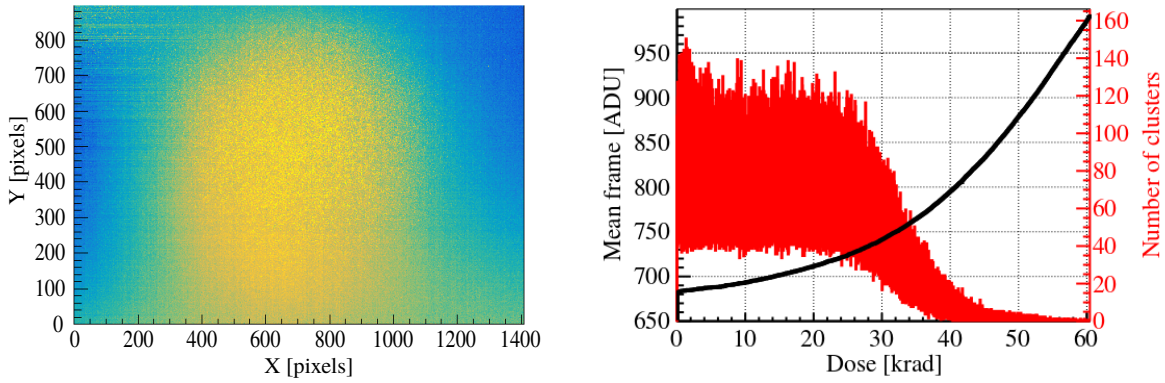
FIGURE 3.14: Spectrum of the  $^{55}\text{Fe}$  source taken with the INTPIX6 CZ(n) detector.

### 3.7 Studies of radiation hardness

To gather a large statistics for detailed studies, a 24 hour long measurement with a high intensity  $^{55}\text{Fe}$  source was carried out. Unfortunately, after this measurement the detector started to behave incomprehensibly. A very high nonuniformity was found on the pedestal map. An example of frame taken after that long measurement is shown in Fig. 3.15A, where an increased pedestal values in the central part of the detector are clearly visible. Since the observed pattern size and shape directly correspond to the used  $^{55}\text{Fe}$  source and it appears exactly at the position of the source placement, the radiation damage was suspected. Because of the existence of a quite thick insulator layer ( $\sim 200$  nm) located just under the electronics the SOI structure is mainly susceptible to the Total Ionisation Dose (TID) effects. Therefore, to confirm the presumptions, a total dose deposited within the buried oxide (BOX) layer needed to be estimated.

The  $^{55}\text{Fe}$  source emits low energy X-rays, which are mainly absorbed within few micrometers of the detector. Before reaching the sensing volume of the detector, they have to pass through the chip passivation layer (of thickness unknown precisely), five layers of metallisation (with nonuniform coverage across the pixel) and the silicon layer with the electronics, so the direct estimation of the deposited dose would be inaccurate. Fortunately, the total dose received by the BOX layer can be also calculated based on the exponential nature of X-ray attenuation and the number of measured X-rays that have reached the sensing volume. As it can be seen in Fig. 3.15A the scale of the radiation damages highly depends on the detector region. Thus, for the estimation of the received dose only a central region was chosen.

The mean number of clusters  $\langle N \rangle$  reconstructed in a single frame (during integration time  $\tau = 10 \mu\text{s}$ ) was around 70. Because of very short radiation length it may be assumed that



(A) The example of row signal map taken with the CZ(n) wafer irradiated up to 60 krad showing the increased pedestal in the central region.

(B) Mean frame (blue) and number of clusters reconstructed in single frame (red) in function of the total dose.

FIGURE 3.15: Plots showing the INTPIX6 CZ(n) detector behaviour during the measurement with the high intensity  $^{55}\text{Fe}$  source.

all photons that have reached the sensing volume have also decayed within it. Therefore, from the number of measured clusters, the intensity at the bottom side of the insulating layer  $I(y = \text{BOX}_{\text{bot}})$  (according to Fig 3.16) can be directly obtained as:

$$I(y = \text{BOX}_{\text{bot}}) = \frac{\langle N \rangle}{\tau} = \frac{70 \text{ particles}}{10 \mu\text{s}} = 7 \frac{\text{particles}}{\mu\text{s}} \quad (3.5)$$

Following the decay law, the intensity  $I(y = \text{BOX}_{\text{top}})$  at the top side of the buried oxide layer may be calculated taking the BOX thickness  $y_{\text{BOX}} = 0.2 \mu\text{m}$  and the radiation length for  $\sim 6 \text{ keV}$  photons in  $\text{SiO}_2$  of  $x_{0_{\text{SiO}_2}} = 55 \mu\text{m}$ :

$$I(y = \text{BOX}_{\text{top}}) = I(y = \text{BOX}_{\text{bot}}) \cdot e^{-\frac{y_{\text{BOX}}}{x_{0_{\text{SiO}_2}}}} \quad (3.6)$$

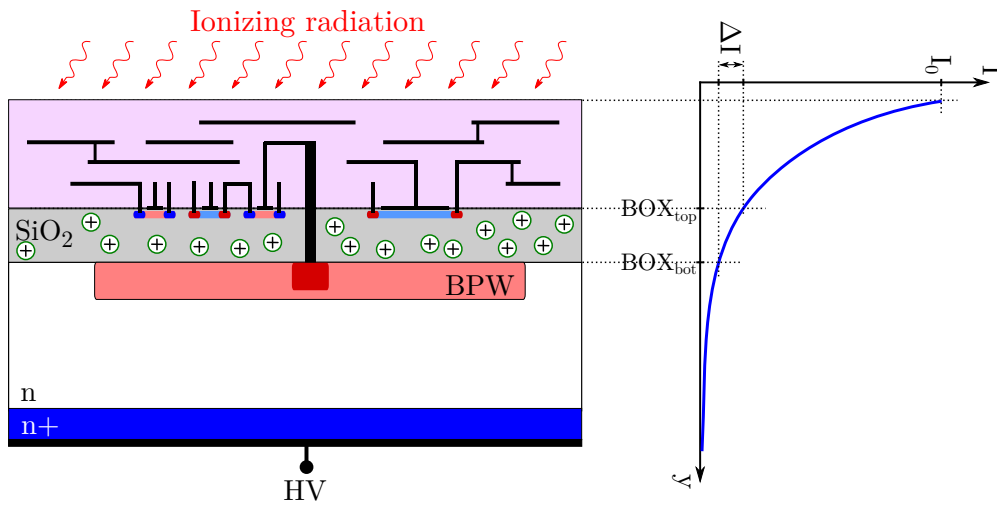


FIGURE 3.16: Sketch of the irradiated SOI structure with the waveform of the incident radiation intensity in function of depth (not to scale).



Which gives the total number of photons attenuated within the insulator layer:

$$\begin{aligned}\Delta I &= I(y = BOX_{top}) - I(y = BOX_{bot}) \\ &= I(y = BOX_{bot}) \left( e^{\frac{x_{BOX}}{x_{SiO_2}}} - 1 \right) \\ &= 0.14 \frac{\text{particles}}{\mu\text{s}}\end{aligned}\quad (3.7)$$

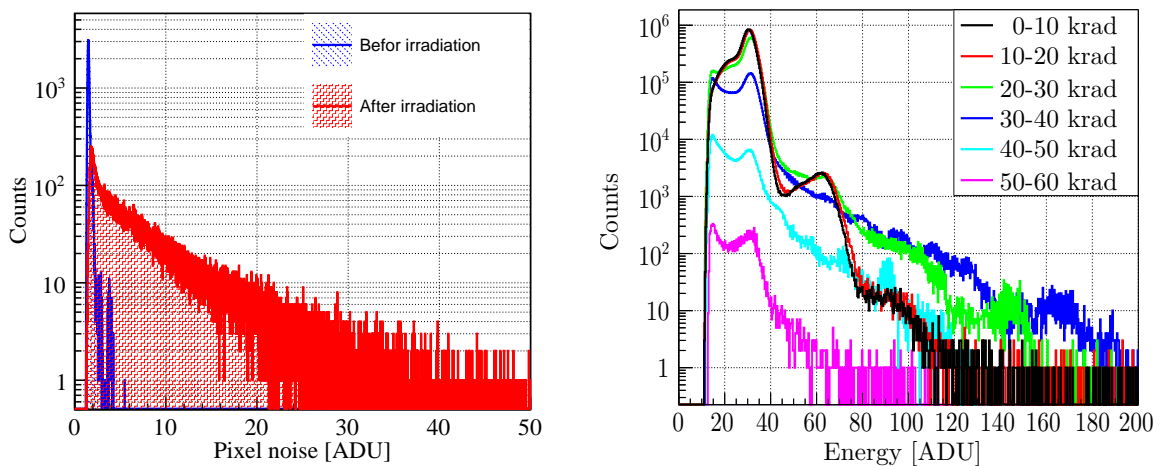
From above, the total irradiation dose  $D_{BOX}$  can be designated as:

$$D_{BOX} = \frac{\Delta I \cdot E_\gamma \cdot t}{m_{BOX}} = 60 \text{ krad} \quad (3.8)$$

where  $t$  is the irradiation time of 24 hours and  $m_{BOX}$  is mass of the considered material volume of 4.16  $\mu\text{g}$ .

The irradiation was performed during the ongoing measurement, therefore the information about the detector performance at different dose levels can be easily extracted. The number of reconstructed clusters per frame and the mean frame value in function of dose are shown in Fig. 3.15B. Since the mean frame is changing significantly during the measurement the analysis flow had to be adopted to this behaviour. Therefore, for this analysis the pedestal value for each pixel was updated continuously to follow the observed trend. Also the bad pixel finding algorithm was adopted to look for noisy pixels not only within the ‘‘calibration’’ data sample, but periodically also in the ‘‘true’’ data during the analysis.

From the observed hit rate it is clear that the detector behaves stable up to about 25 krad, while above this value a significant drop of the detection efficiency is observed. The main reason of this decrease is the growing number of bad pixels. It may be seen from Fig. 3.17A where the pixel noise is shown before and after irradiation. The number of bad (highly fluctuating)



(A) Pixel noise distribution before the irradiation and after receiving 60 krad. (B)  $^{55}\text{Fe}$  spectra shown separately for different dose ranges.

FIGURE 3.17: Comparison of INTPIX6 CZ(n) performance before and after irradiation.

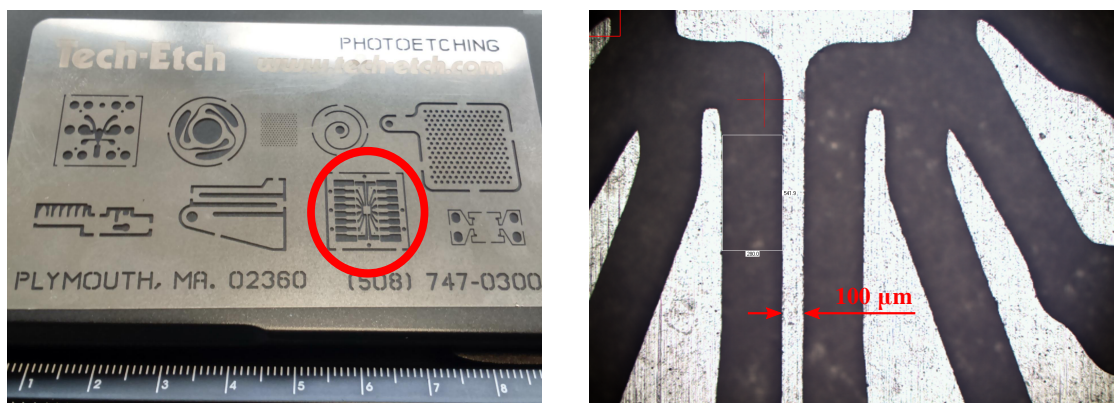
pixels grows with irradiation dose. At certain point their fraction is so high that the cluster searching algorithm, which requires good pixels without signal at the cluster boundary, starts to lose efficiency.

Very similar conclusions can be drawn from the plot shown in Fig. 3.17B where  $^{55}\text{Fe}$  spectra are shown for different dose ranges. The spectra in the plot are done taking clusters of all sizes but at such low energies practically all events are single pixel clusters. It is seen that up to 20 krad the curves are practically not changed with the same efficiency and resolution. The peaks from single, double (or even triple)  $^{55}\text{Fe}$  photon events can be easily identified. For the doses up to 30 krad the main spectrum features are still preserved. For higher doses both the efficiency and the peaks shape deteriorate.

### 3.8 INTPIX6 imaging capabilities

To precisely determinate the imaging capabilities of the detector one should follow the specified methodology. Since in our case, the proper equipment was not available only several, simple measurements were performed to get the rough feeling about INTPIX6 potential. For that purpose the whole ( $1408 \times 896$  pixels) matrix was read out. As a “photographed” object a metal plate with different patterns, shown in Fig. 3.18A, was used. Most of the measurements were taken using the shape with the finest structure, marked by a red circle. An additional independent test was performed with the microscope to recognize dimensions of used structure. The picture of its central part is shown in Fig. 3.18B. The smallest details have the widths of about  $\sim 100 \mu\text{m}$ .

During the measurement the chosen pattern was placed about 2 mm above the detector surface and illuminated using a defocused laser light. Two different wavelengths were used: 660 nm and 1060 nm. Each measurement consisted of 100 individual frames, taken with the integration time of 1000  $\mu\text{s}$ . The final pictures were obtained offline by summing up all frames from a single run.



(A) Global view, showing all available patterns, with the one mostly used marked with red circle.

(B) Picture from microscope taken to determine the pattern dimensions.

FIGURE 3.18: Pictures of a metal mask used to check the imaging capabilities of the INTPIX6 detector.

The examples of obtained images using the FZ(n) wafer type are presented in Fig. 3.19A for which the 660 nm laser was used and in Fig. 3.19B for the 1060 nm laser. It can be immediately noticed that the illumination was nonuniform. This was caused by the problems with defocusing the laser while keeping its intensity high enough. Nevertheless, for both cases the pattern was reconstructed at the very detailed level. One can notice that the picture obtained with the 660 nm laser seems to be slightly sharper which is caused by the very shallow penetration of the 660 nm photons, which gives no time for the induced charges to diffuse before arriving to the sensing electrodes. Whereas 1060 nm photons may penetrate the whole detector thickness, therefore the generated charge diffuses more. This is even more explicit after looking on the picture taken with the 660 nm laser but during the illumination from the backside, which is presented in Fig. 3.20A. The overall shape is still visible but its sharpness is significantly deteriorated, which is directly related to the increased diffusion comparing to the front illumination.

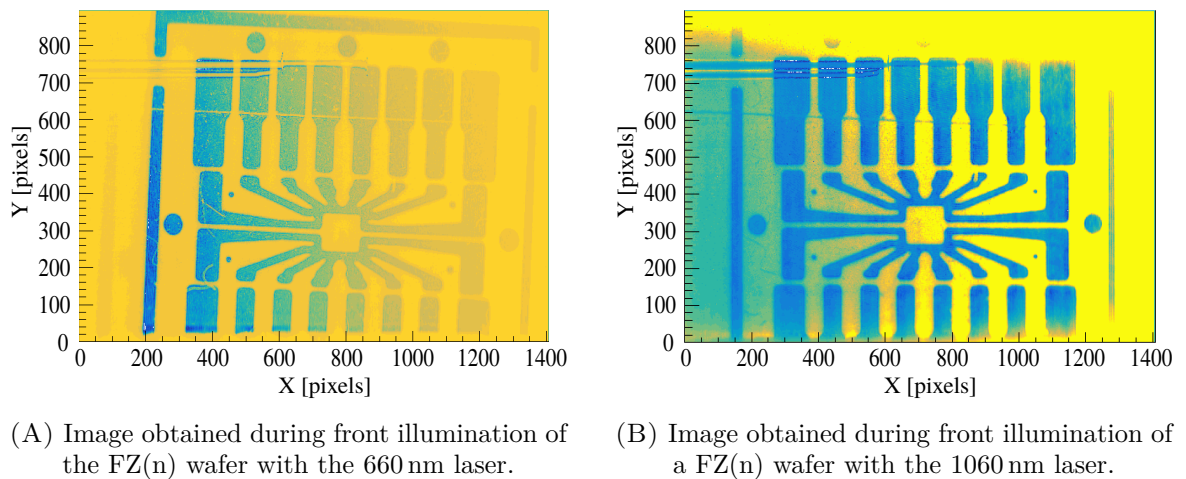


FIGURE 3.19: Images of the test pattern taken with the INTPIX6 detector.

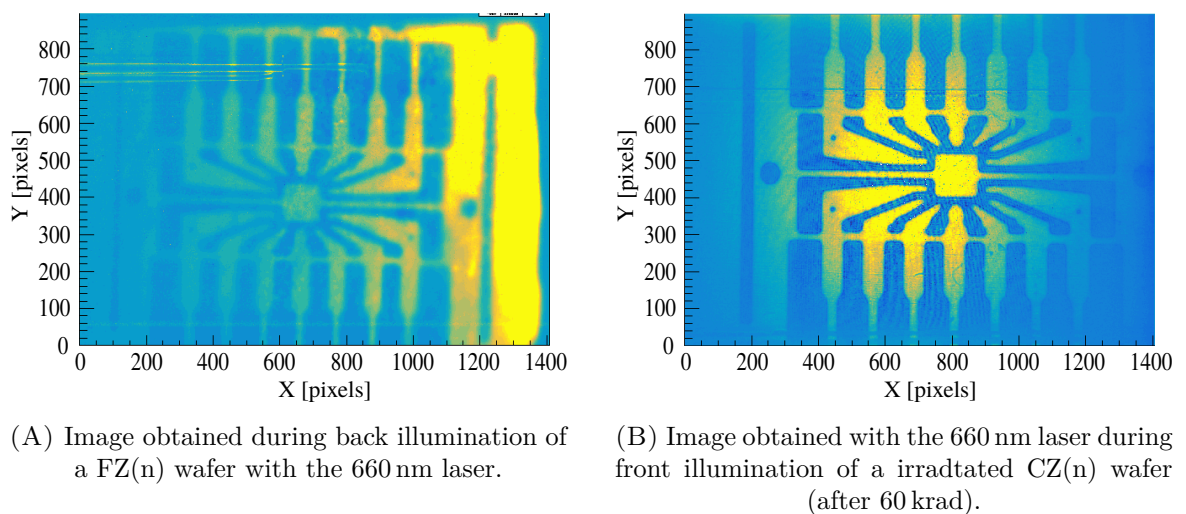


FIGURE 3.20: Images of the test pattern taken with the INTPIX6 detector.

Similar measurement was also performed for the irradiated CZ(n) wafer. Its result is shown in Fig. 3.20B. Regardless the degradation in efficiency and energy resolution a reasonable image quality is still preserved.

### 3.9 INTPIX6 results summary

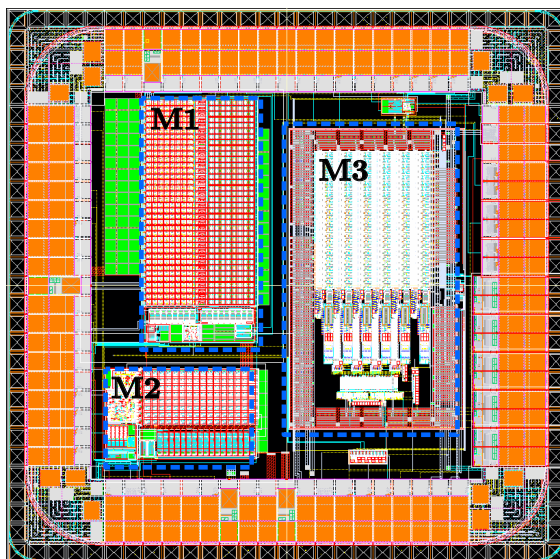
The INTPIX6 monolithic pixel detector performance was studied in detail with the use of two different X-ray sources ( $^{241}\text{Am}$  and  $^{55}\text{Fe}$ ) including its irradiation up to 60krad dose. The ENC of about  $70\text{e}^-$  (pixel noise) or  $110\text{e}^-$  (width of  $^{55}\text{Fe}$  peak) was obtained before the irradiation. The detector showed such a good performance, reflected by its small ENC and negligible number of bad pixels, up to about 25krad dose. Above this value the number of noisy pixels started to increase significantly but the detector was still operational, giving reasonable response to the laser and X-ray signals even after 60krad dose. The presented studies were done for the standard Lapis SOI process. An improvement of radiation hardness is expected from the recent SOI process updates like Lightly Doped Drain (LDD) transistors or double SOI wafer [29].

## Chapter 4

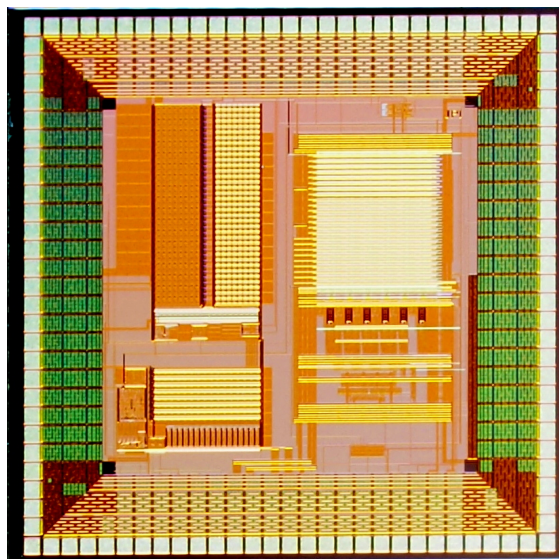
# SOI detector prototype for general studies

After very promising results obtained with the INTPIX6 detector, it was decided to design the SOI device targeting the application in particle physics experiments. Since for high energy particle detectors there is a growing demand on the material budget reduction, a step towards monolithic solutions seems to be a natural direction. However, a lot of R&D work is still required to bring these technologies to the level mature enough to build a reliable, complex detector systems.

Before undertaking a project dedicated to the requirements of a specific detection system a small general purpose test device was designed. It aimed to check the technology capabilities, test different architectures and become familiar with all available structures.



(A) Layout of the final design.



(B) Photograph of the fabricated prototype.

FIGURE 4.1: Layout and photograph of the SOI detector prototype designed for the general studies.

## 4.1 Design overview

The layout of the final design and photograph of the fabricated chip are presented in Fig. 4.1A and Fig. 4.1B. Due to its test purposes, it encompasses several small independent matrices, utilizing different readout approaches. First, main matrix (M1) exploits an integrating type pixels, the second one (M2) contains pixels with shaper and peak-detector (designed without participation of the thesis author), whereas the third one (M3) is a self-triggering matrix with an on-chip digitalization and data serialization. This section will be fully devoted to the first matrix (M1).

The block diagram of the readout electronics of the main matrix is presented in Fig. 4.2, with parts designed by the author of this thesis marked. The heart of the design is a small,  $16 \times 36$  pixel matrix operating in rolling-shutter mode. The matrix is divided into two halves, with different input stage architectures. One part utilizes a simple source-follower (SF) architecture, whereas the second one a charge-sensitive pre-amplifier (CPA). The CPA matrix was further divided into two parts. One, CPA(small), with small ( $5 \mu\text{m} \times 5 \mu\text{m}$ ) sensing diode located in the center of the pixel and the second, CPA(large) with the large sensing diode covering the entire in-pixel electronics. The first approach is suitable for DSOI(p) wafer where there is no need for the additional electronics shielding, whereas the second type is aimed for all standard SOI wafers. The large diode have to cover almost whole pixel area ( $29 \mu\text{m} \times 29 \mu\text{m}$ ). To slightly reduce its capacitance, the sensing implant is having the cut offs in the regions without the active electronics components, which results in its irregular shape.

The readout control block is common for the whole matrix. It is realized according to the rolling-shutter readout mode and provides all steering signals necessary to control the signal

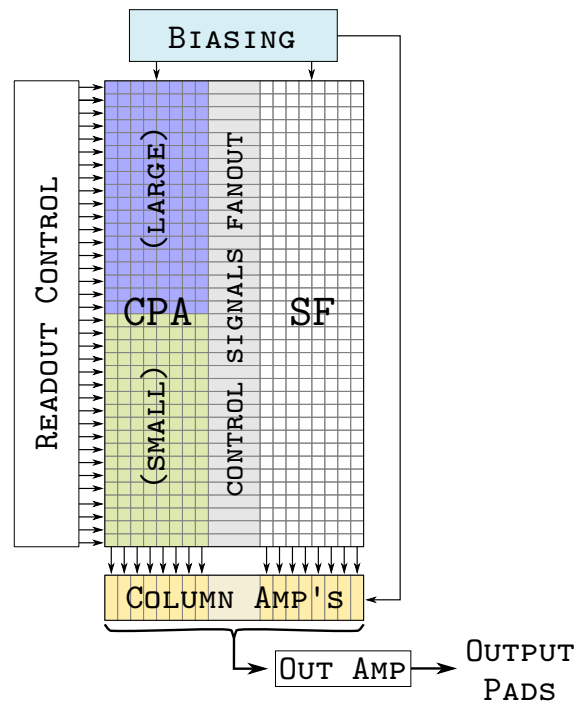


FIGURE 4.2: Block diagram of the main matrix. Blocks designed by the author of the thesis have been marked with the color background.

flow from each pixel towards the output pad. The column amplifiers buffer the charge signal received from pixels and redirect it to the output amplifier which is driving the signal out of the chip.

### 4.1.1 Pixels architecture

#### Source-follower architecture

As already mentioned, two different architectures of pixel electronics were implemented. The source-follower in-pixel circuitry is presented in Fig. 4.3A. The charge sensitive volume is represented by a diode reversely-biased by the high voltage (HV). The sensing node is directly connected to the gate of the nMOS transistor in the source-follower configuration. In this topology the voltage gain is close to unity, which means that any voltage change on the input (which in this case is a gate terminal), will cause almost identical voltage change at the output (source). Since the input node does not have any direct current (DC) path, any charge generated within the active sensor volume  $Q_{IN}$  will be stored across the input node capacitance  $C_{IN}$  leading to the voltage shift  $\Delta V_{SF_{IN}}$  on the input node. For the source-follower, the same voltage shift is observed on its output  $\Delta V_{SF_{OUT}}$ . In this way the charge induced by the radiation is converted into the voltage signal and its amplitude corresponds to the amount of initial charge.

$$\Delta V_{SF_{OUT}} \simeq \Delta V_{SF_{IN}} = \frac{Q_{IN}}{C_{IN}} \quad (4.1)$$

In the next step the signal goes to the two parallel sample and hold blocks formed by a pair of switches and capacitances. Together, they operate in a Correlated Double Sampling (CDS) mode, which means that in the first step (switch  $F_1$  shorted) a baseline voltage (the output voltage level after the reset) is stored on one of the capacitances. Later on, after the integration time, a second sample (switch  $F_2$  shorted) is stored on the second capacitance. This one stores the voltage level corresponding to the baseline plus any signal induced during integration. Thus in an ideal case, the difference between this two samples correspond directly to the input charge.

There are several benefits of using the CDS technique, but it has also some drawbacks. In principle, carrying out two consecutive measurements allows to filter out the low frequency noise component and the shorter the interval between samples the wider suppressed frequency band is. But on the other hand both measurements contribute with their thermal noise which in consequence multiplies the overall noise by the factor of  $\sqrt{2}$ . Therefore, the profits from the usage of the CDS are highly case-dependent. Unfortunately, the provided technology models do not allow for a reliable noise simulation. Nevertheless, since the design was devoted to the test structures it was decided to use the CDS technique. It has also a beneficial side effect, which is the conversion of a single ended into a differential signal, which is much less sensitive to the distortions induced during the readout.

Once both, baseline and signal samples are stored on the capacitances, they are waiting to be read out off the pixel. It occurs when the *READ* signal appears and connects them to the input of a column amplifier located outside the matrix.

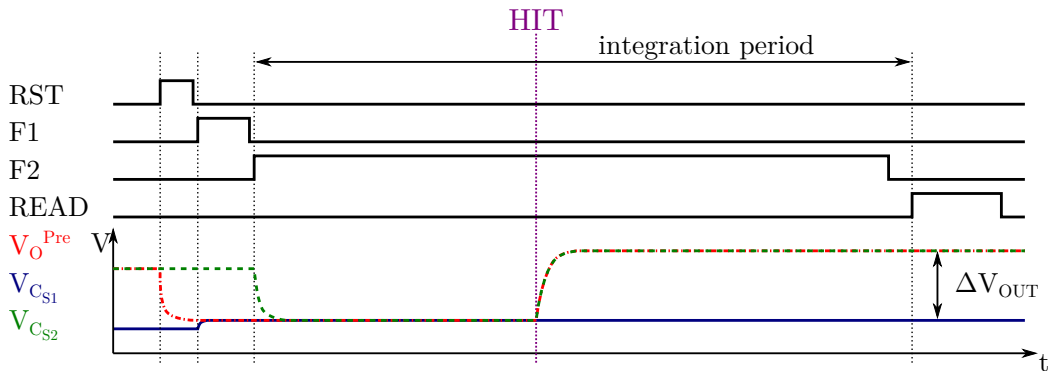
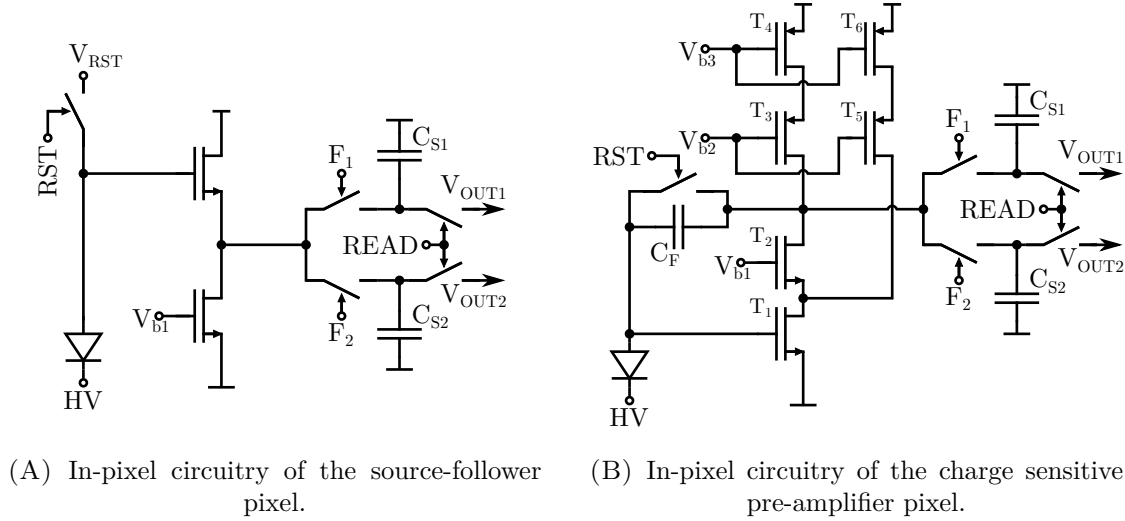


FIGURE 4.3: Schematic diagrams of in-pixel readout electronics with the waveforms of the main signals.

### Charge-sensitive pre-amplifier architecture

The general readout approach in the second type of the pixels (Fig. 4.3B) is similar – the input stage is followed by the CDS block. As already mentioned, instead of a source-follower there is a charge-sensitive pre-amplifier in the input stage. The main advantage of this solution is highly reduced dependence of the output signal magnitude on the input capacitance. This gives the opportunity to amplify the signal in the first stage of the readout chain, suppressing the noise contribution from the subsequent stages.

According to the simple scheme of charge-sensitive pre-amplifier presented in Fig. 4.4 its voltage response  $V_{CPA_{OUT}}$  on the input charge  $Q_{IN}$  can be calculated knowing that the whole injected charge will be divided between  $C_D$  and  $C_F$  capacitances:

$$Q_{IN} = Q_D + Q_F \quad (4.2)$$



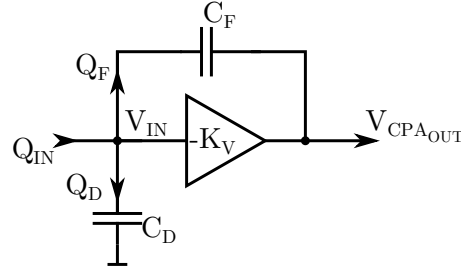


FIGURE 4.4: Simple scheme of the charge-sensitive pre-amplifier.

Using the fact that voltage across the capacitance is given by  $V = \frac{Q}{C}$  and the pre-amplifier assures  $V_{CPA_{OUT}} = -K_V \cdot V_{IN}$ , we get:

$$\begin{aligned} Q_{IN} &= V_{IN}C_D + (V_{IN} - V_{CPA_{OUT}})C_F \\ &= V_{IN}(C_D + (K_V + 1)C_F) \\ &= -\frac{V_{CPA_{OUT}}}{K_V}(C_D + (K_V + 1)C_F) \end{aligned} \quad (4.3)$$

Which finally leads to:

$$V_{CPA_{OUT}} = -\frac{Q_{IN}}{C_F + \frac{C_F + C_D}{K_V}} \xrightarrow{K_V \rightarrow \infty} \frac{Q_{IN}}{C_F} \quad (4.4)$$

where  $C_F$  is the feedback capacitance,  $C_D$  is the detector capacitance and  $K_V$  is the open-loop voltage gain of the pre-amplifier. This directly shows that when the high gain of the pre-amplifier is assured the output signal amplitude becomes independent from the usually dominating detector capacitance and depends only in the  $C_F$  value.

For the pre-amplifier a telescopic cascode architecture was chosen. In this configuration voltage gain is given by [35]:

$$K_V = g_{m1} \cdot (r_{ds2}(1 + g_{m2}r_{ds1}) || r_{ds3}(1 + g_{m3}r_{ds4})) \quad (4.5)$$

where  $g_{mX}$  is a transconductance of  $X$ -th transistor and  $r_{dsX}$  is its small-signal drain-source resistance. To obtain a high  $K_V$  value the additional current source (formed by  $T_5 + T_6$ ) was introduced which increases the input transistor transconductance  $g_{m1}$ , without lowering the main current source resistance ( $r_{ds3}(1 + g_{m3}r_{ds4})$ ).

### Feedback capacitance in CPA

To fully utilize the charge sensitivity of the pre-amplifier for a small input charge detection (below 100 aC) one has to provide a small feedback capacitance  $C_F$ . According to equation 4.4 the value of  $C_F$  determines the charge to voltage conversion ratio, the smaller feedback capacitance is the larger output voltage amplitude. For example, to obtain a 100 mV signal from the 100 aC of input charge, the capacitance  $C_F$  should be 1 fF. Unfortunately, it is not

easy to implement such a small capacitance. The smallest standard MIM (metal-insulator-metal) capacitor available in the used technology is 37.5 fF, which is far too much for this application.

The easiest method to lower the capacitance is connecting several capacitors in series, since the total capacitance is equal to the reciprocal of the sum of the reciprocals of their individual capacitances. But in this particular case it will mean that to obtain a value around 1 fF one has to use a series of about 37 minimal capacitors. This of course is not suitable for the pixel design where the available area is highly limited.

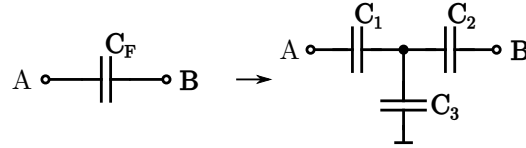


FIGURE 4.5: T-shape capacitor structure, used to minimise the feedback capacitance.

Another solution is a “T-shape” capacitor structure, shown in Fig. 4.5. In this approach the capacitance seen between terminals A and B is given by:

$$C_{AB} = \frac{C_1 C_2}{C_1 + C_2 + C_3} \quad (4.6)$$

Which for  $C_1 = C_2$  simplifies to:

$$C_{AB} = \frac{C_1}{2 + \frac{C_3}{C_1}} \quad (4.7)$$

This shows how the effective feedback capacitance may be reduced by keeping a high  $\frac{C_3}{C_1}$  ratio. According to the above example, using the “T-shape” structure with minimal size  $C_1$  and  $C_2$  capacitors, to get the 1 fF feedback capacitance, the  $C_3$  has to be about 35 times larger than  $C_1$ . This means that total capacitance needed in both presented approaches is exactly the same, but implementing a single large capacitance requires much less area than 35 independent ones. This is mainly because each single capacitor needs a special boundary treatment, which has a significant impact on its area.

Another way to produce a small capacitance is a custom plate capacitor formed by two metal layers. But since it is not a standardized structure available from the component library provided by the vendor, its value may vary significantly.

The consistency of the feedback capacitance over the whole pixel matrix is very important factor. In the ideal case one expects exactly the same response of each pixel in the matrix. However, during the chip production every single component of the whole design is subjected to a mismatch variation. Since the feedback capacitance has direct influence on the output signal magnitude, its variation immediately deteriorates the chip performance. The component parameters fluctuations are described by the technology vendor. For the capacitance it mainly depends on its dimensions, the larger the capacitance, the smaller its relative capacitance variation.

To estimate the spread of the feedback capacitance for these two approaches let us consider the case in which  $n$ -folded reduction of a minimal available capacitance ( $C_{min}$ ) is obtained using the smallest area. For the series capacitance connection this means a chain of  $n$   $C_{min}$  capacitances. Thus:

$$\frac{1}{C_{F_{Series}}} = \frac{1}{C_1} + \frac{1}{C_2} + \dots + \frac{1}{C_n} \quad (4.8)$$

and for  $C_1 = C_2 = \dots = C_n = C_{min}$  it simplifies to:

$$C_{F_{Series}} = \frac{C_{min}}{n} \quad (4.9)$$

Assuming that each single capacitance in the chain has its own uncertainty  $\Delta C_{min}$  and contributes to the resultant uncertainty  $\Delta C_{F_{Series}}$  according to the error propagation law, one gets:

$$\Delta C_{F_{Series}} = \frac{\Delta C_{min}}{\sqrt{n}} \quad (4.10)$$

Concerning the same assumptions for the second approach, according to equation 4.6 one has to implement  $C_1 = C_2 = C_{min}$  and  $C_3 = (n - 2)C_{min}$ . The total capacitance  $C_{F_{Tshape}}$  is then equal:

$$\begin{aligned} C_{F_{Tshape}} &= \frac{C_1 C_2}{C_1 + C_2 + C_3} \\ &= \frac{C_{min}^2}{2C_{min} + (n - 2)C_{min}} = \frac{C_{min}}{n} \end{aligned} \quad (4.11)$$

To estimate its spread  $\Delta C_{F_{Tshape}}$ , one needs to make an additional assumption on the uncertainty of  $C_3$  capacitance. Taking the worst case scenario for  $C_3$  let us assume a constant relative uncertainty which means that  $\Delta C_3$  will be equal to  $\sqrt{n - 2}\Delta C_{min}$ . Following the uncertainty propagation law:

$$\begin{aligned} \Delta C_{F_{Tshape}} &= \sqrt{\Delta C_1^2 \left( \frac{\partial C_{F_{Tshape}}}{\partial C_1} \right)^2 + \Delta C_2^2 \left( \frac{\partial C_{F_{Tshape}}}{\partial C_2} \right)^2 + \Delta C_3^2 \left( \frac{\partial C_{F_{Tshape}}}{\partial C_3} \right)^2} \\ &= \sqrt{\Delta C_1^2 \left( \frac{C_2(C_1 + C_2 + C_3) - C_1 C_2}{(C_1 + C_2 + C_3)^2} \right)^2 + \Delta C_2^2 \left( \frac{C_1(C_1 + C_2 + C_3) - C_1 C_2}{(C_1 + C_2 + C_3)^2} \right)^2 + \Delta C_3^2 \left( \frac{-C_1 C_2}{(C_1 + C_2 + C_3)^2} \right)^2} \\ &= \sqrt{\Delta C_1^2 \left( \frac{C_2(C_2 + C_3)}{(C_1 + C_2 + C_3)^2} \right)^2 + \Delta C_2^2 \left( \frac{C_1(C_1 + C_3)}{(C_1 + C_2 + C_3)^2} \right)^2 + \Delta C_3^2 \left( \frac{C_1 C_2}{(C_1 + C_2 + C_3)^2} \right)^2} \\ &= \sqrt{\Delta C_{min}^2 \left( \frac{C_{min}^2(n - 1)}{(nC_{min})^2} \right)^2 + \Delta C_{min}^2 \left( \frac{C_{min}^2(n - 1)}{(nC_{min})^2} \right)^2 + (n - 2)\Delta C_{min}^2 \left( \frac{C_{min}^2}{(nC_{min})^2} \right)^2} \\ &= \sqrt{\Delta C_{min}^2 \left[ 2 \left( \frac{n - 1}{n^2} \right)^2 + \frac{n - 2}{n^4} \right]} = \Delta C_{min} \sqrt{\frac{2n - 3}{n^3}} \end{aligned} \quad (4.12)$$

Comparing the results obtained for both solutions its clearly visible that the second method provides smaller mismatch of the capacitance, for all allowed  $n$  values ( $n > 2$ )

$$\Delta C_{min} \sqrt{\frac{2n-3}{n^3}} < \frac{\Delta C_{min}}{\sqrt{n}} \quad (4.13)$$

$$\Delta C_{F_{Tshape}} < \Delta C_{F_{Series}}$$

Therefore, since the T-shape approach provides a better matching and is less area consuming it was implemented in the design. Moreover, the  $C_3$  capacitance was divided into two parallel capacitors: one always connected  $C_{3a}$  and second one  $C_{3b}$  which may be optionally added. Such a solution allows for different gain selection. Final values of  $C_{3a}$  and  $C_{3b}$  were dictated by the available area and they were set to  $C_{3a} = 75$  fF and  $C_{3b} = 187.5$  fF, which results in 4.17 fF of the feedback capacitance in the high gain mode and 9.375 fF in the low gain mode. Besides that, one has to remember that there are always some parasitic capacitances, formed within a transistor structure or between the interconnection wiring, adding up to the effective capacitance. Unfortunately, the precise tool for the parasitic capacitance extraction was not available, but basing on the experience from other technologies the total parasitic feedback capacitance should not be larger than few femtofarads.

### Switches in CPA

Another very sensitive part of the presented architecture is the reset of input stage. Since in the integrating type pixels there is no DC connection between the input and output nodes, the proper operating point of the input transistor has to be set during the resetting phase. Thus in this architecture the reset is done by a switch shorting the output of the pre-amplifier to its input (*RST* switch in Fig. 4.3B). Such a solution not only ensures that the charge gathered in the input node during the previous cycle is removed, but it also sets the appropriate self-consistent operating point of the pre-amplifier.

In CMOS technology switches are usually implemented as a two transistor structure called the transmission gate (or T-gate) shown in Fig. 4.6. It consists of a pair of pMOS and nMOS transistors, where source of the nMOS is connected with the drain of pMOS forming an input node, and *vice-versa* for the output node. The gates are connected to the digital steering signal, opposite for the pMOS and nMOS. Therefore, either in both transistors are “on” or both of them are “off”.

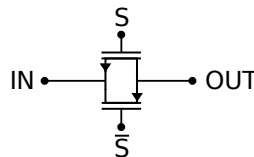


FIGURE 4.6: Schematic of the transmission gate controlled by the steering signal  $S$  and its negation  $\bar{S}$ .

A pair of nMOS and pMOS transistors is needed to allow the switch operation in the whole available voltage range since a single nMOS transistor is not able to transmit the voltages close

to the supply voltage ( $V_{DD}$ ), whereas a pMOS can not transmit voltages close to the ground ( $V_{SS}$ ). It is so, because they are not able to form a channel when the gate-source voltage ( $V_{GS}$ ) is below the threshold voltage. Nevertheless in some cases, when the full voltage swing is not required, a single nMOS or pMOS transistor may be used as a switch. This was exactly the case in the presented design where the input voltage range was already limited from the bottom by the  $V_{GS}$  of the input transistor, thus for the resetting a single pMOS transistor was sufficient.

Another issue connected with CMOS transistors used as switches, is a charge injection occurring during switching them off. This is particularly crucial for the presented design since any charge injected into the input node is processed in the exactly same way as the input charge generated in the sensor. Thus this issue needs to be studied carefully. Once a switch transistor is turned on a channel is created by the electrons (nMOS) or holes (pMOS) induced by the gate voltage. It allows for an easy current flow between source and drain so their potentials are equalized. When the transistor switches off the charges gathered within the channel are no longer attracted, the channel is shrinking and so charges move out through the drain and source terminals. Thus it produces a tiny current flowing into the nodes connected to these terminals. If that node has any DC path, it will just pass through without any long-term consequences, but if that node is only AC coupled the injected charge will remain there. This issue is schematically shown in Fig. 4.7A.

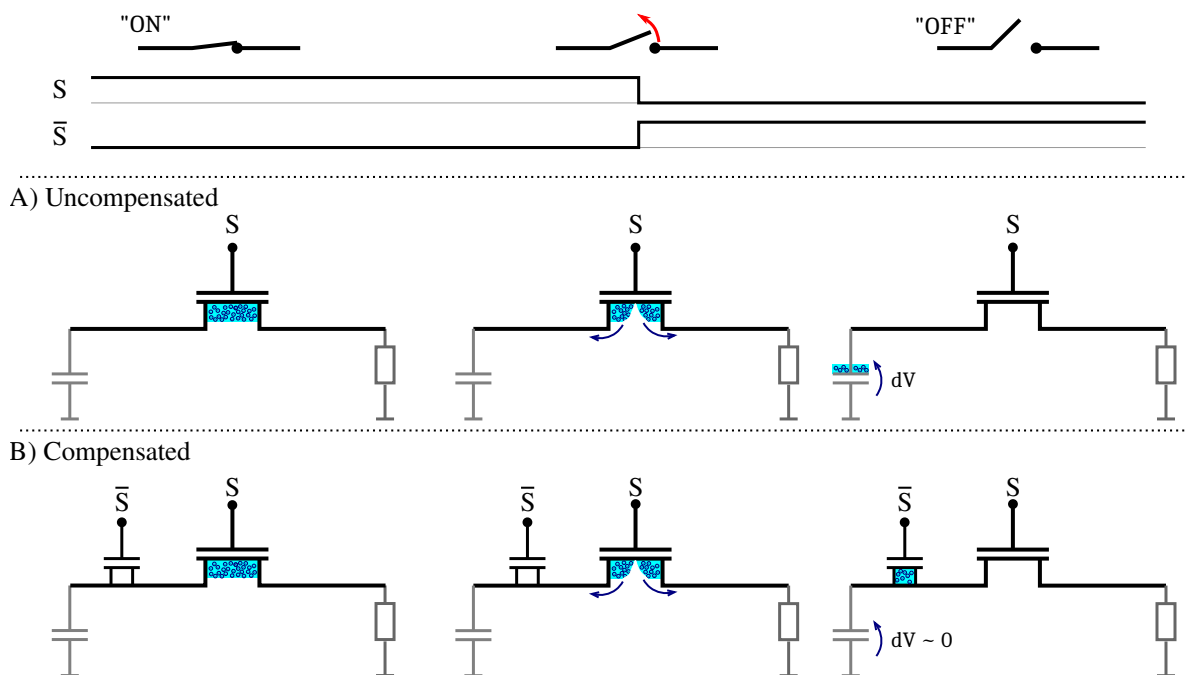


FIGURE 4.7: Sketch showing the charge injection during switching off the transistor. The first case (A) presents the uncompensated switch, whereas in the second case (B) a dummy transistor is added to minimise the issue.

Since in the presented design the reset switch is connected between the output and the input of the pre-amplifier some charge will be injected into these two nodes. The charge injection into the output can be neglected since there is a DC current flowing from the power supply

line, through this node to the ground. Unfortunately, it is not the case for the input node, which after reset is only capacitively coupled with the rest of the circuitry. Moreover, since this is the input of the charge-sensitive pre-amplifier it will respond to the charge injection exactly in the same way as to the charge induced in the sensor and thus its performance may be deteriorated.

It is hard to overcome this issue since it is not obvious how the charge will be divided between the drain and source terminal. In principle the division should be proportional to the total capacitances seen on these nodes but there are several factors that also contribute to the final division factor, for example the switching time. Beside that, the amount of charge in the channel is also not constant, it highly depends on the input signal level, since it defines the gate-source voltage.

It is almost impossible to control this issue precisely but there are few solutions that may reduce its impact. Usually a dummy transistor controlled by a reverse signal is added into the sensitive node. Therefore, at the same time when the switch is turning off and injects the charge, the dummy transistor is switching on and pulls this charge to form its own channel (Fig. 4.7B). Since it is hard to determine the amount of injected charge usually an assumption of equal division is used and thus the size of the dummy transistor is two times smaller (to form two times shorter channel). The main advantage of this solution is that both the switching transistor and the dummy transistor are seeing exactly the same input voltage (same  $V_{GS}$ ) therefore the dependence from the input signal is suppressed.

### 4.1.2 Column amplifier

During the matrix readout phase the signal from each pixel in a given row is redirected to a separate column amplifier. The global picture of the readout scheme is shown in Fig. 4.8A. The column amplifier together with the storage capacitances located in the pixel form a fully-differential switched capacitor amplifier. The main purpose of this device is buffering the signal and shifting its common mode voltage to half of the supply voltage, which maximizes the output voltage range.

The working principle of the amplifier in this configuration is presented in Fig. 4.8B (for simplicity a single-ended version is presented). Switched capacitor circuits base on transferring the charge gathered on the capacitance by switching it between different nodes, thus their operation is divided into non-overlapping phases. In the first phase ( $\phi_1$ ) the amplifier circuit is reset by shorting the output of the amplifier with its input, which removes all the charge gathered across the feedback capacitance  $C_F$ . At the same time the input voltage  $V_{in}$  is stored on the  $C_{IN}$  capacitance (which corresponds to the charge  $Q_{in} = \frac{V_{in}}{C_{IN}}$ ). After that, in the second phase ( $\phi_2$ ) the  $C_1$  capacitance is switched to the input of the amplifier. Assuming the infinite open loop gain of the amplifier, all the charge stored previously on  $C_1$  will now flow to the  $C_F$  capacitance, which will result in the output voltage equal to:

$$V_{out} = -\frac{Q_{in}}{C_F} = -V_{in} \cdot \frac{C_{IN}}{C_F} \quad (4.14)$$

Following this relation a voltage gain in this amplifier configuration is defined by:

$$K_V = \frac{V_{out}}{V_{in}} = -\frac{C_{IN}}{C_F} \quad (4.15)$$

Therefore, such a configuration allows not only for the signal buffering but also for its amplification and this opportunity was utilized in the final design. By switching on and off an additional capacitance into the feedback there are two possible gain settings: unity gain and multiplication by a factor of two.

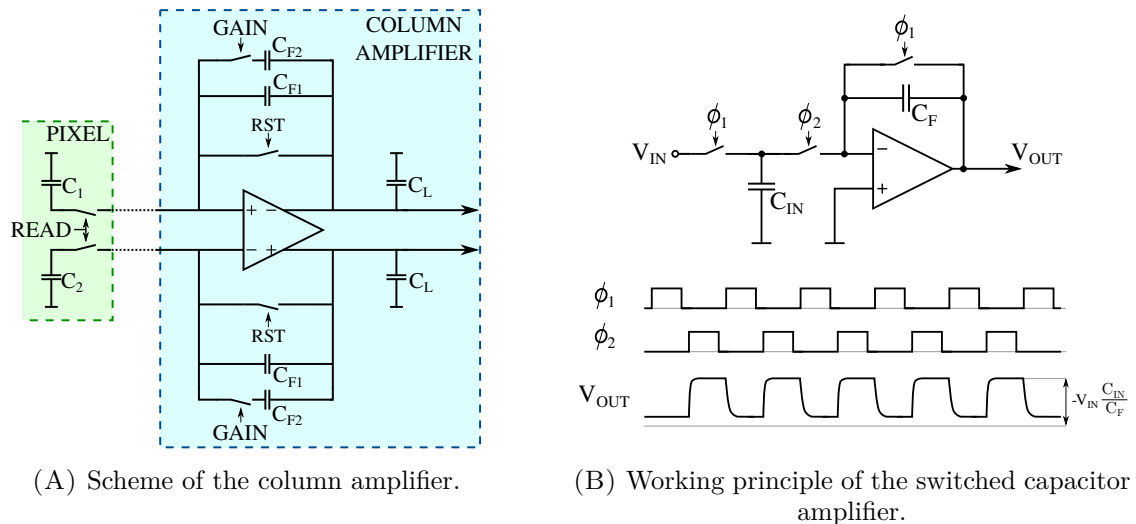


FIGURE 4.8: Scheme and working principle of the column amplifier.

The core of each column amplifier is designed exploiting the fully-differential Recycling Folded Cascode (RFC) amplifier architecture and is presented in Fig. 4.9. This architecture is an improved version of a classic Folded Cascode (FC) which allows for the power consumption reduction by a factor of two, maintaining its performance on the same level. A detailed description of the RFC amplifier architecture and the comparison with its predecessor can be found in [36, 37].

To assure a proper voltage levels on the output of the fully-differential amplifiers an additional circuitry called Common Mode Feedback (CMFB) is required. It sets the averaged output voltage ( $V_{CM} = \frac{V_{out+} + V_{out-}}{2}$ ) to the desired voltage level, which is usually a half of the supply voltage since such a condition allows for the maximum output voltage range. There are numerous CMFB circuits with their own pros and cons. In the presented design a switched capacitor CMFB architecture was utilized (shown in Fig. 4.9). The main advantage of this solution is no static power consumption as well as no limitations in terms of the output voltage levels. On the other hand it requires an additional steering signals and does not provide continuous output signal so the output voltage has to be sampled within a certain time period. But in this particular case when the whole column amplifier is already based on a switched capacitor approach all these restrictions already exist. Therefore a phase control signals may be shared between these two circuits. A wider discussion on the switched capacitor CMFB can found in [38].

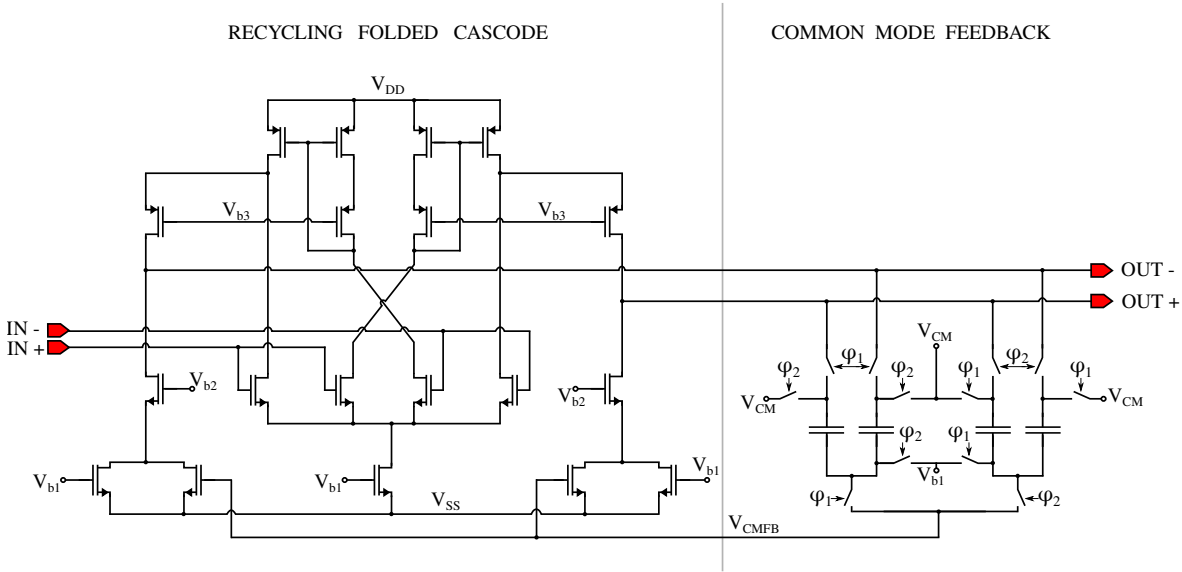


FIGURE 4.9: Schematic view of the fully-differential recycling folded cascode architecture with the capacitive common mode feedback circuitry implemented in column amplifier.

## 4.2 Simulations

To ensure the proper behaviour of the designed circuits numerous simulations were performed, starting from the individual analysis of each single component of the readout chain and ending with a complete simulation of the whole design. It has to be pointed out that the used technology is still being in the development phase, therefore the simulation models provided by the vendor are not precisely tuned, and some of the possible issues may not show up in the simulations. For example it was not possible to perform the Monte-Carlo simulation for estimation of the pixel-to-pixel component mismatch, that may cause a gain variations. Nevertheless, each cell passed a series of simulations which includes: transient simulations showing

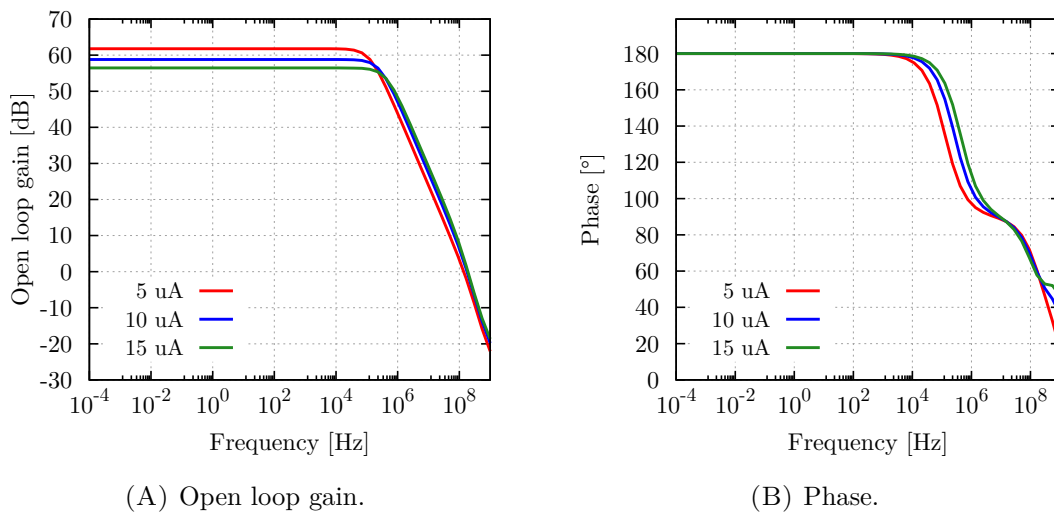


FIGURE 4.10: Pre-amplifier AC characteristics.



the circuitry behaviour over the time, AC simulations that allows to ensure the amplifier stability and estimate its parameters, as well as DC simulations necessary to check the transistors operating points.

The pre-amplifier AC characteristics showing its open loop gain and the output signal phase are presented in the Fig. 4.10. One can see a minor dependence on the biasing current, with the expected trend towards slightly faster response at the expense of the power consumption. The stability summary showing the basic amplifier parameters as: gain, phase margin and gain-bandwidth product is presented in Tab. 4.1. It shows a gain of around 60 dB which is a reasonable value for a single stage amplifier, whereas the phase margin is around  $60^\circ$  which is enough to ensure its stability.

Biasing current [uA]	Gain [dB]	Phase margin [ $^\circ$ ]	Gain-bandwidth product [MHz]
5	61.8	66.4	138
10	58.8	58.4	178
15	56.5	56.0	191

TABLE 4.1: Pre-amplifier stability summary.

To evaluate the charge sensitivity of the pre-amplifier and its input dynamic range a series of transient simulations of the pre-amplifier response to input charge injection was performed. The combined results together with fitted regression lines are shown in Fig. 4.11. Results are presented for both high and low gain modes of the pre-amplifier and the linear regions have been marked with dark and light gray respectively. The input charge dynamic range is from  $-1.8$  fC up to  $2.5$  fC for the high gain and from  $-4$  fC to  $7$  fC for the low gain. It covers both signal polarities because the fabrication on different substrate wafer types was foreseen. Nevertheless, there is a small asymmetry towards the positive input charges because p-type Double SOI wafer was the primary choice.

Beside that, the charge to voltage conversion ratio can be obtained from the fitted functions:

$$\Delta V_{out}^H [V] = Q_{in} \cdot 0.2422 \left[ \frac{V}{fC} \right] + 0.0025 [V] \quad \text{at high gain,} \quad (4.16)$$

$$\Delta V_{out}^L [V] = Q_{in} \cdot 0.1111 \left[ \frac{V}{fC} \right] + 0.0014 [V] \quad \text{at low gain.} \quad (4.17)$$

They also show a negligible constant offset values (at the level of millivolts), but the simulations do not take into account any sensor-related effects, such as leakage current, so there is no reason for any offset. Simulated values of charge conversion ratios are respectively  $G^H = 0.2422 \left[ \frac{V}{fC} \right]$  for the high gain mode and  $G^L = 0.1111 \left[ \frac{V}{fC} \right]$  for the low gain. Assuming the theoretical relation given by Eq. 4.4 and taking the final values of the feedback capacitance as  $4.17$  fF in the high gain mode and  $9.375$  fF in the low gain mode, one can compare the simulation results with the theoretical expectations. The calculated conversion ratios are:  $G_{th}^H = 0.2398 \left[ \frac{V}{fC} \right]$  and  $G_{th}^L = 0.1067 \left[ \frac{V}{fC} \right]$  respectively, which is in a very good agreement with the simulations.

Similar simulations were performed for the column amplifier. Its AC characteristics are

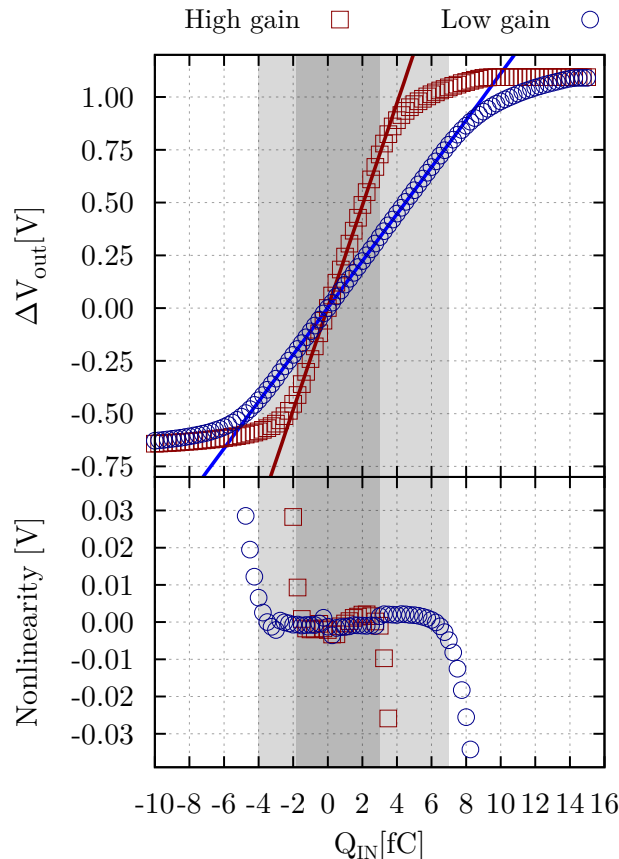


FIGURE 4.11: Pre-amplifier response to the input charge  $Q_{IN}$  injection.  $\Delta V_{out}$  represents the relative output voltage change, whereas nonlinearity represents the deviation from the fitted regression line.

shown in Fig. 4.12 and the obtained parameters in the Tab. 4.2. Here also a consistent behaviour over the biasing current setting is observed. The open loop gain is on the similar level as in the pre-amplifier, which is expected since column amplifier also incorporates single cascoded amplifying stage. The stability of this device is very good with the phase margin over  $90^\circ$ , whereas its gain-bandwidth product is much lower due to much higher output capacitance.

Biasing current [uA]	Gain [dB]	Phase margin [°]	Gain-bandwidth products [MHz]
5	58.0	91	4.2
10	58.4	92	4.8
20	59.9	91	5.8

TABLE 4.2: Column amplifier stability summary.

To check the input dynamic range of the column amplifier, similarly to the previous case, a set of transient simulations with different input voltage amplitudes was executed. The combined results are shown in Fig. 4.13. Since it is a fully differential amplifier the input signal is given by a voltage difference on its two input terminals  $V_{in} = V_{in}^+ - V_{in}^-$ . Because both  $V_{in}^+$  and  $V_{in}^-$  may vary from 0 to 1.8 V (supply voltage), the effective input voltage range is from  $-1.8$  to  $1.8$  V.

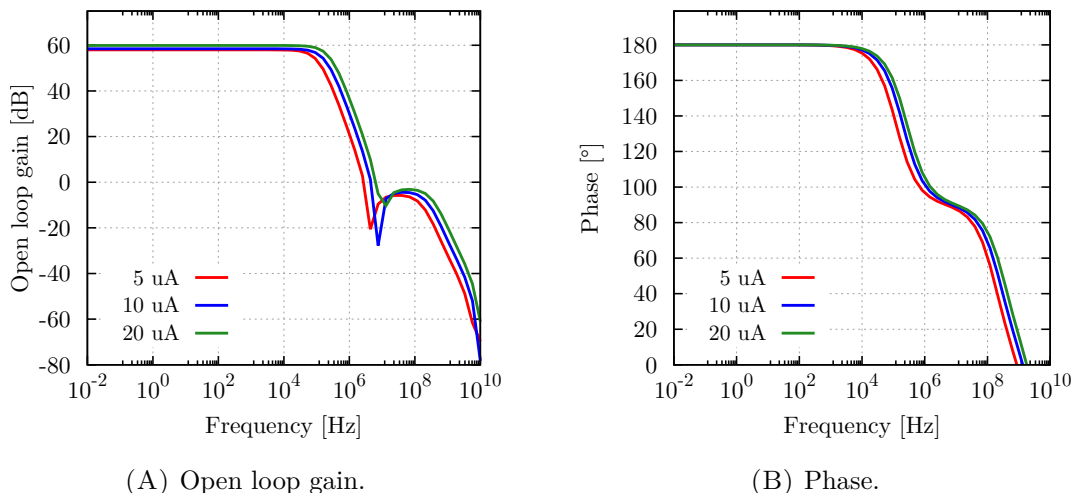


FIGURE 4.12: Column amplifier AC characteristics.

As mentioned earlier two different working modes of the column amplifier were implemented: buffering (unity gain) and amplifying (doubling the signal). The simulated gain can be extracted from the fitted functions:

$$\Delta V_{out}^{Buf} = V_{in} \cdot 0.994 \quad \text{buffering mode,} \quad (4.18)$$

$$\Delta V_{out}^{Amp} = V_{in} \cdot 1.978 \quad \text{amplifying mode.} \quad (4.19)$$

The simulated gains of  $G^{Buf} = 0.994 \left[ \frac{V}{V} \right]$  for the buffering mode and  $G^{Amp} = 1.978 \left[ \frac{V}{V} \right]$  for the amplifying mode are in very good agreement with the design assumptions. Moreover, the simulated offset was negligible (on the order of several microvolts). The input dynamic range, for which the amplifier response remains linear, was determined as  $[-1.1 : 1.1]$  and  $[-0.55 : 0.55]$  respectively and is marked with a dark and light gray boxes.

Usually the noise performance of the readout chain (especially the input stage) is also a subject of a detailed simulations. Unfortunately, provided technology parametrization does not allow for a reliable noise simulation thus the noise optimisation was not possible.

### 4.3 Measurements setup

After finishing the design and simulation phase, the project was sent for fabrication and the extensive work on the measurement setup preparation had began. A dedicated readout system had to be prepared from the scratch, which means: design of the printed circuit board (PCB), selection of a readout control hardware platform and development of appropriate firmware, as well as the development of a data acquisition software (DAQ). The author of this thesis was developing the DAQ, whereas other tasks were entrusted to other members of the group.

The main purpose of the PCB design was to provide a set of appropriate biasing voltages and currents, retrieve the analog output signal from the chip and digitize it, as well as assure the communication with the chip necessary to control its behaviour. Since this required incorporation of quite a lot of electronics it has been decided to split the PCB design into two

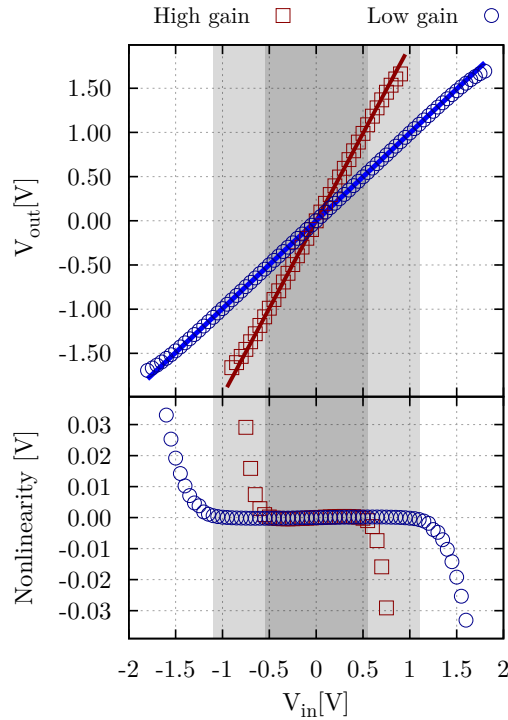


FIGURE 4.13: Column amplifier response on the input voltage change, where  $V_{in} = V_{in}^+ - V_{in}^-$  and  $V_{out} = V_{out}^+ - V_{out}^-$ . Nonlinearity represents the deviation from the fitted regression line.

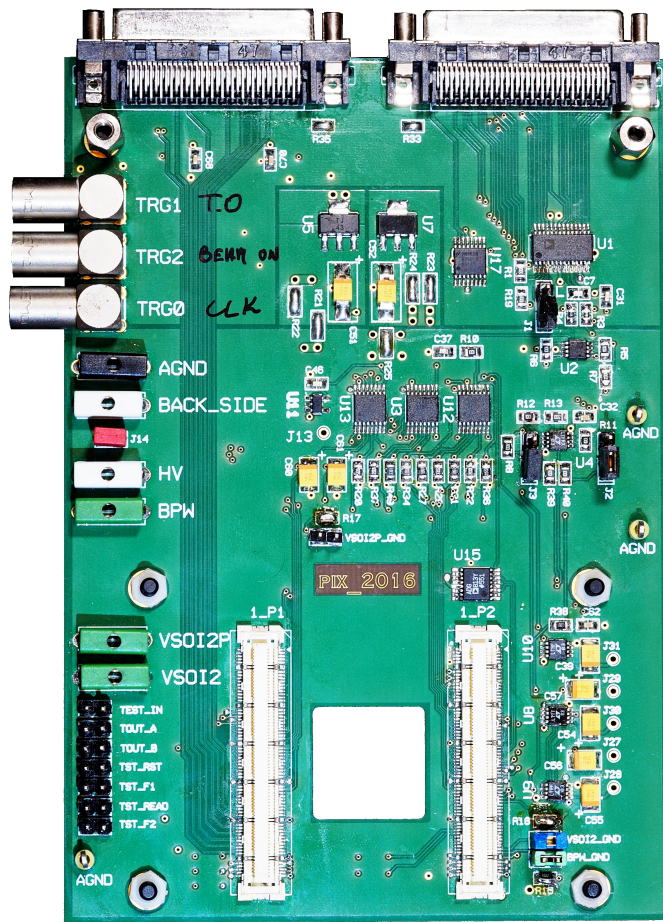
boards. The “mother” board containing all functional circuitry, and the second small “mezzanine” board with the chip glued and bonded to it. This solution gives a lot of flexibility in terms of the number of potentially tested assemblies, since it does not require the unnecessary multiplication of all of the “mother” board electronics, which highly reduces the overall costs.

The photographs of the manufactured and assembled PCB boards are shown in Fig. 4.14. The final design incorporates a 16-channel digital to analog (DAC) converter (*DAC128S085*) with voltage buffers and voltage to current converters for biasing the chip. The analog signal information from the chip is being retrieved by a fully differential instrumentation amplifier which drives a high speed 12-bit differential analog to digital (ADC) converter (*AD9235BRUZ*). The digitized information is sent further through the VHDCI connectors that assure the communication between the readout control system and the “mother” board.

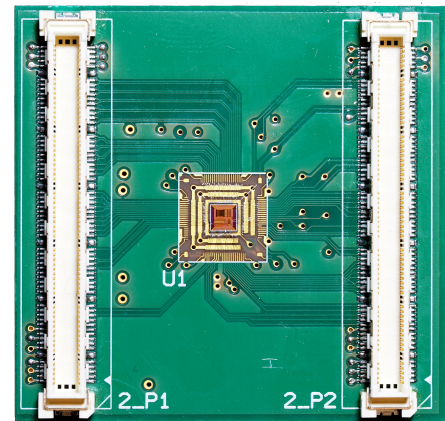
The readout control system bases on the commercially available Genesys Virtex-5 FPGA Development Board, which gives a possibility to include a lot of functionalities within the FPGA firmware. Thus, the FPGA provides the digital steering signals for the chip and readout board, controls ADC operation, buffers the digitized data and forms the data frame structure. Moreover, a TCP/IP protocol was implemented in the FPGA firmware to allow the efficient data transfer between the control board and PC via the Ethernet connection.

### 4.3.1 Data acquisition software

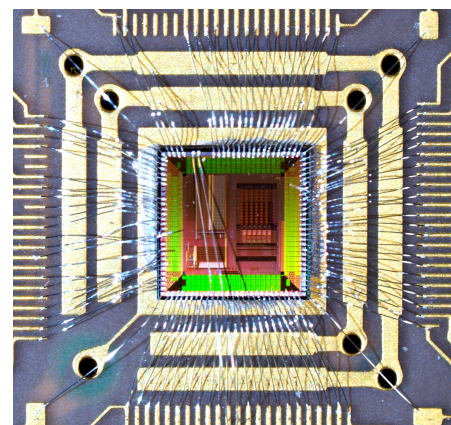
As mentioned earlier, the dedicated data acquisition software was developed by the author of the thesis. Since it has to have quite a wide range of functionality it was written in C++



(A) “Mother” board.



(B) “Mezzanine” board.



(C) Close-up on bonded chip.

FIGURE 4.14: Photographies of readout boards with all the components soldered and chip bonded.

exploiting existing libraries from the ROOT Data Analysis Software and Boost [39]. The software was responsible for controlling the FPGA operation, so a set of basic commands understood by the FPGA was introduced. They allow for setting a desired conditions for the detector operation (as biasing currents and voltages levels, on-chip electronics settings like for example amplifiers gains, and so on). Beside that, they allow for the measurement flow control through the commands starting, stopping or pausing the ongoing measurement. Since the whole communication was done through the Ethernet connection the implementation of TCP/IP socket was necessary. Along that, the integration with another detection system, the beam-test telescope [40], was also needed. To allow a synchronous operation of these two systems a separate TCP socket was implemented to listen and interpret the commands broadcasted by the telescope control software.

The software was also intended to receive the row data coming from the FPGA and store them. For that purpose a ROOT TTree structure was incorporated. Thus all the row data are stored in separate TTree leaves containing the informations about the signal amplitude on each pixel in a given frame, the frame ordinal number and the time-stamp attached to it.

Moreover, each tree contains also some basic information about the settings used during the measurements. Beside that, for easy measurements tracking an automatic log file was created, containing the summary information for each run.

To increase the utility of the DAQ control software a Graphical User Interface (GUI), based also on the ROOT libraries, was added. It provides all the functionality required from the detector user point of view. There is a possibility to set all the biasing levels, chip settings, number of frames to be taken or the output file name. Moreover, within a GUI there is a separate section that allows for the basic online data quality monitoring. Every  $n$ -th frame (where  $n$  can be set) is displayed on the user interface and also a mean frame value is calculated and shown on a separate plot. Thus, an immediate check of the detector behaviour is possible.

Even if all these side amenities provide a very useful features, they should not affect the main purpose of a DAQ software which is of course receiving and saving the data. Therefore, to not limit a data link throughput, by involving significant fraction of computation time into the side tasks, a multi-threading was implemented. Once a separate thread is created for the data socket, its performance is no longer affected by the other software parts. In the final version of the DAQ separate threads were assigned also to the data monitoring features, GUI and telescope socket, which allows for its fluent operation, regardless of the conditions.

## 4.4 Data analysis software

The functionality expected from the data analysis software for the SOI detector designed in Cracow was very similar to the one for the INTPIX6 detector. Since the data analysis software for the INTPIX6 had been already well developed and its operation verified the core of the software was reused. Only minor changes were needed to adapt the system to a slightly different input data format and detector geometry. Whereas all the algorithms for pedestal and noise calculation, signal extraction and clusterization remained the same.

The whole analysis flow is also very similar to the one already introduced for the INTPIX6 detector in section 3.3. Thus only a brief reminder will be presented here with the focus on the parts that are different.

In the first step the data file is loaded. After that, in the INTPIX6 software the bad frames are rejected, but for this system there are no issues affecting the data quality during the data acquisition, thus this step is omitted. Directly after loading the data file the pedestal and noise are calculated for each pixel in the matrix, using the “calibration” sample (no signal source). Later on a true data sample is processed. For each frame the signal is extracted from the raw data and hits are formed using the two threshold clusterization method. The default setting for the thresholds was  $6\sigma$  for the seed and  $2\sigma$  for the neighbours. Before creating the final hits sample, cuts are applied to rejects all clusters touching the detector borders. In the end the processed hits informations are stored in the output data file and basic plots (as pedestal and noise distributions, hit energy spectra) are displayed. In the INTPIX6 software there was also a procedure for the pixel gain calibration, but since the matrix size in our prototype is much smaller it does not show similar misbehaviour, and thus this step was skipped in the analysis flow.

## 4.5 Spotted issues

There were several issues spotted during the measurements. Thus to assure the reliability of the presented results, it is necessary to clearly introduce all of them. For this reason some of the measurement results have to be shown already in this paragraph, without the in-depth examination which is presented in subsequent sections.

First of all an unexpected behaviour was noticed during applying a high voltage to the back plane of the DSOI(p) wafer. As it can be seen in Fig. 4.15A the current consumption starts to rise significantly after exceeding  $-50$  V, preventing further depletion development. Using the information from other measurements it can be concluded that it happens at about  $150\ \mu\text{m}$ , far before reaching the full depletion, since the full sensor thickness is two times larger. Designed detectors allow for the high voltage application either directly to the backside metallisation or through the contacts located on top of the sensor, but according to the presented results the issue is present independently from the polarization method. It should be also noticed that the pedestal shown in Fig. 4.15B does not follow the trend observed for the current consumption. This means that this issue is not related with the increased leakage from the sensor matrix volume, whereas it took place at some part of the detector located outside the matrix. The origin of such behaviour is not known, but most probably it is attributed to the problems during the production or handling of this type of wafer, since it was found also on different prototypes.

Another observation is that the energy spectra taken with the CPA matrix on the DSOI(p) wafer deteriorates significantly after exceeding  $-50$  V of back bias. It may be connected with the previous issue, but it is not straightforward since it is observed only in the sub-matrix with the large sensing implant, whereas the one with small diode seems to be insensitive. Plots showing this behaviour are presented in Fig. 4.16. As it can be seen, a significant degradation of the spectra sharpness is visible only for the CPA(large) at  $-60$  V (Fig. 4.16D). Moreover, similar lost of performance does not reveal in the pixel noise (Fig. 4.15C) or the change of the

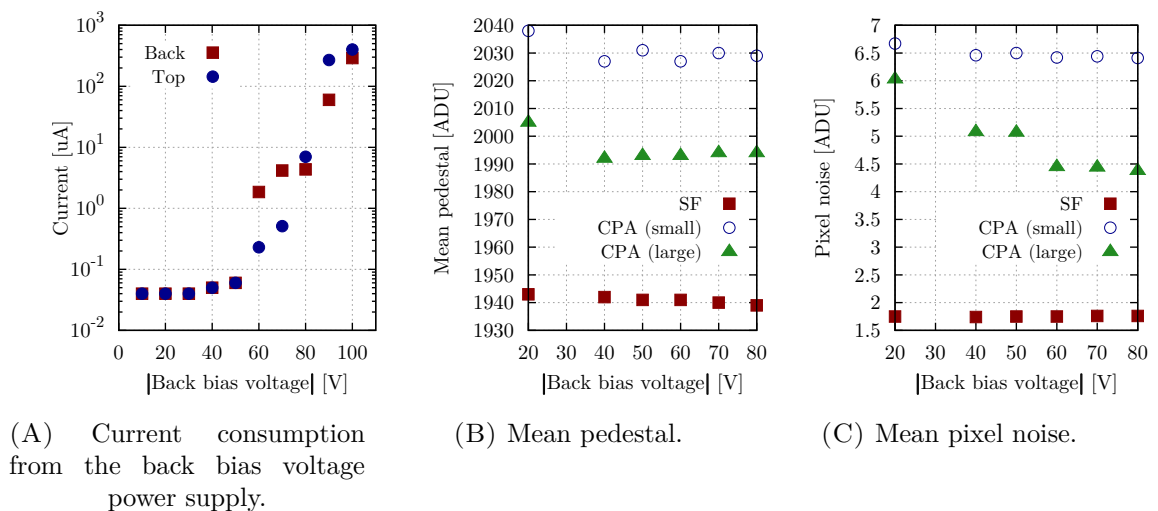
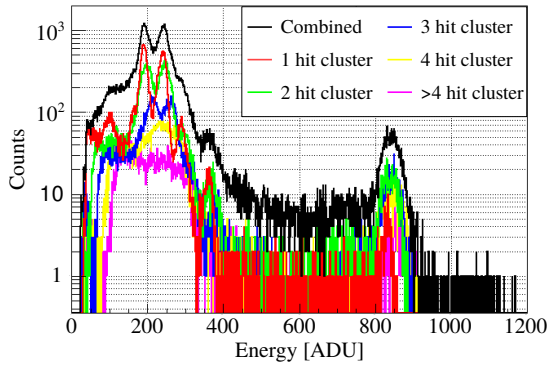
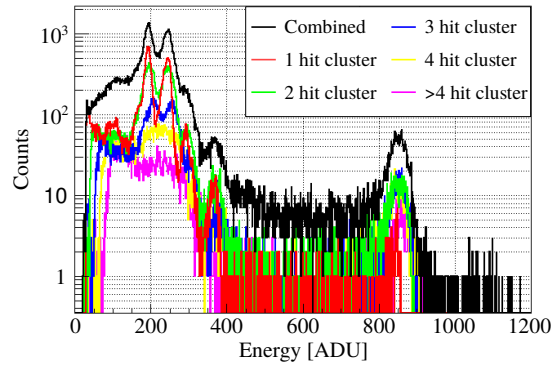


FIGURE 4.15: Results from the DSOI(p) wafer showing the unexpected detector behaviour.

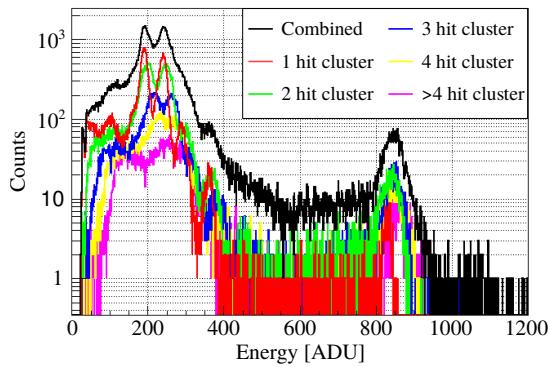
pedestal (Fig. 4.15B). The baseline is stable across the whole back bias range, whereas the pixel noise (for this matrix only) is even improving with the increase of the bias voltage.



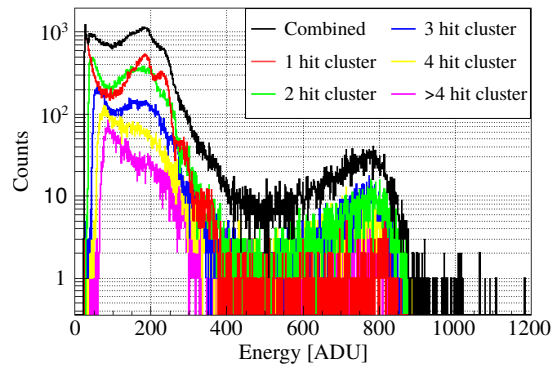
(A) CPA(small),  $-40$  V of back bias.



(B) CPA(large),  $-40$  V of back bias.

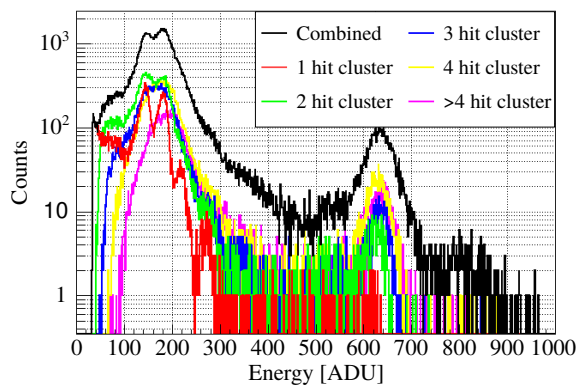


(C) CPA(small),  $-60$  V of back bias.

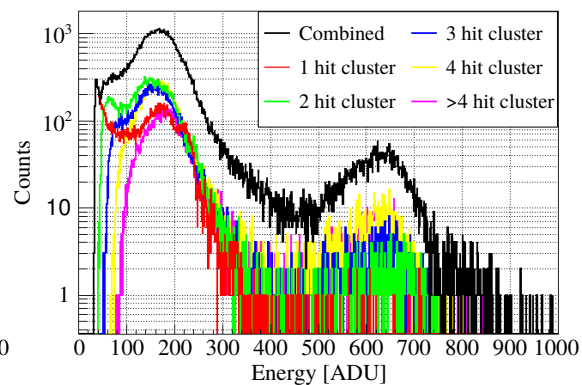


(D) CPA(large),  $-60$  V of back bias.

FIGURE 4.16: Example of  $^{241}\text{Am}$  spectra taken with the prototype fabricated on DSOI(p) wafer. Different colours represent individual contributions from given cluster sizes, whereas black curve shows the combined spectrum.



(A) FZ(n) wafer, CPA(small) sub-matrix.



(B) FZ(n) wafer, CPA(large) sub-matrix.

FIGURE 4.17: Example of  $^{241}\text{Am}$  spectra showing the divergent behaviour of sub-matrices that differ only in the sensing implant size (both at  $70$  V of back bias).



A similar unexpected behaviour of the CPA(large) sub-matrix is observed also on the FZ(n) wafer. Contrary to the theoretical expectation pixels with the small diode show good spectra quality, whereas the sub-matrix with the large one shows a blurred image as presented in Fig. 4.17. Similarly to the DSOI(p) wafer no major difference in the pixel noise is observed comparing these two sensor geometries. Other than for the DSOI(p) wafer, for the FZ(n) such behaviour persists for the whole back bias voltage range, from 10 V up to 200 V (which is far above full depletion).

Summarizing the main issues found during the measurements, the incomprehensible performance of the CPA(large) sub-matrix has been spotted. Thus the results will be presented mainly for the SF and CPA(small) sub-matrices. Moreover, when comparing the outcomes for different wafers, one has to remember that the full depletion of the DSOI(p) sensor was not possible, which may complicate drawing of the final conclusions.

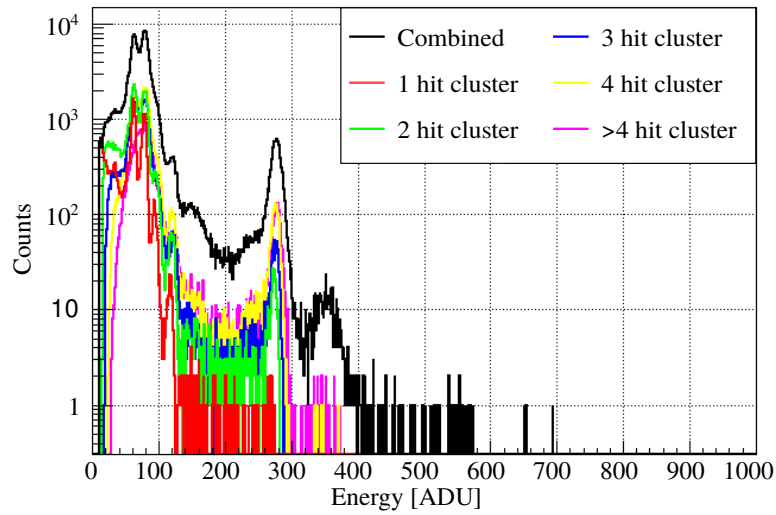
## 4.6 Radioactive source measurements

Similarly to the INTPIX6 detector measurements, the  $^{241}\text{Am}$  source was used to calibrate the detector. Since the presented device is sensitive to the visible light, all the measurements have been carried out within a light-sealed box. If not specified otherwise, the results for the FZ(n) wafer are presented for the back bias voltage set to 70 V, whereas for the DSOI(p) to  $-50$  V.

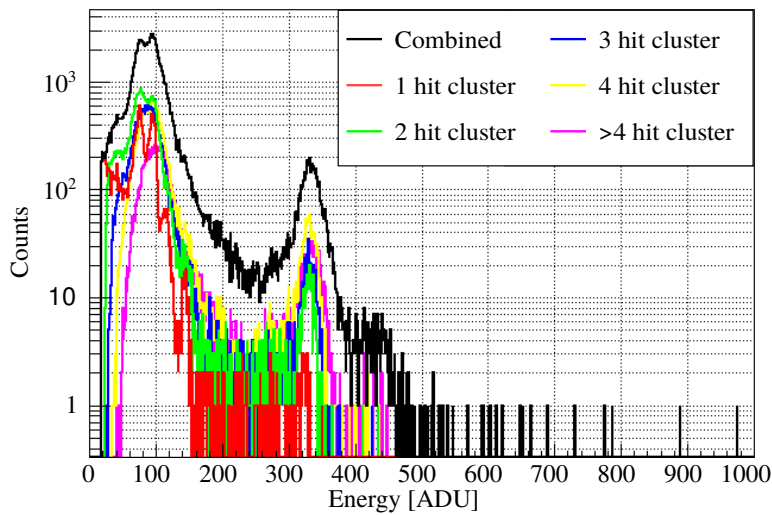
The example of  $^{241}\text{Am}$  spectra for both FZ(n) and DSOI(p) wafers, for each readout architecture and two different pre-amplifier gain settings are presented in Fig. 4.18 and Fig. 4.19 respectively. Different colors represent contributions from different cluster sizes, whereas the black curve shows the combined result. For consistency the energy scale is the same for all cases except the SF matrix for the DSOI(p) where the signal is almost order of magnitude lower. It is clearly visible that the obtained results are highly dependent on the substrate wafer.

Source-followers behave much better on the FZ(n) wafer (Fig. 4.18A) than on the DSOI(p) (Fig. 4.19A). For the FZ(n) wafer all expected energy lines are clearly distinguishable both on the combined spectra and on the individual ones. This is not the case for the DSOI(p) where only highest energy line (59.5 keV) is well separated. Nevertheless, such a behaviour was expected since the DSOI(p) is characterized by much larger pixel capacitance, what directly reduces the signal amplitude (which is also visible comparing these two plots).

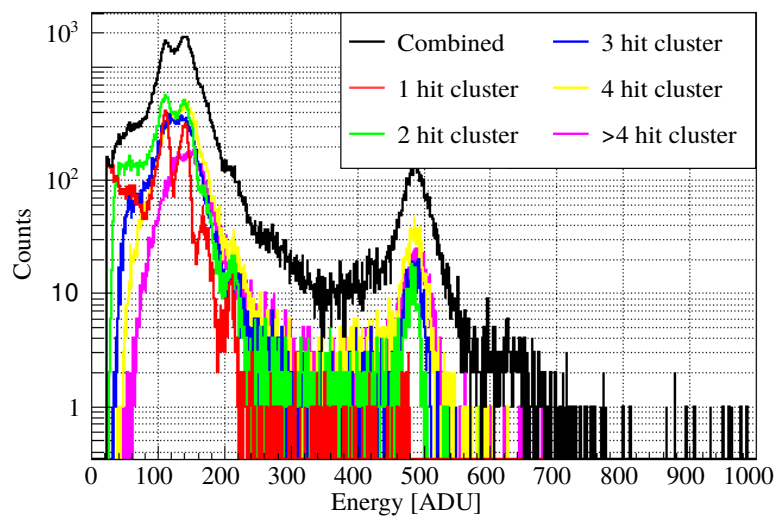
The situation is completely different for the CPA architecture, where the results obtained with the DSOI(p) (Fig. 4.19B and Fig. 4.19C) are not deteriorated. All energy lines are well separated for both low and high pixel gain settings. An unexpected behaviour is observed for the FZ(n) wafer (Fig. 4.18B and Fig. 4.18C), for which the spectra quality seems to be decreased. Moreover, comparing the peak positions, also for this architecture the pixel gain seems to be wafer dependent. Independently from the pre-amplifier gain setting the measurements show that for the FZ(n) wafer the pixel gain is lower than for the DSOI(p), which should not be the case. In principle, the pixel gain in this architecture should be independent from the wafer type, since it is determined only by the feedback capacitance (which obviously should



(A) FZ(n) wafer, SF sub-matrix.

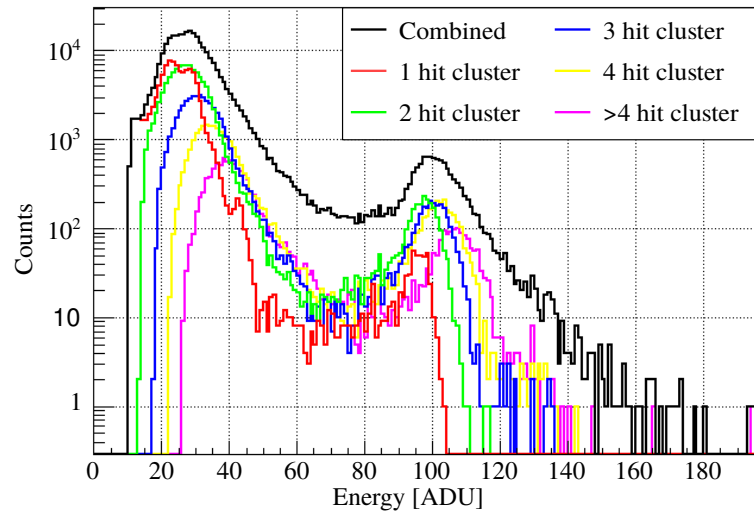


(B) FZ(n) wafer, CPA(small) sub-matrix, low pre-amplifier gain.

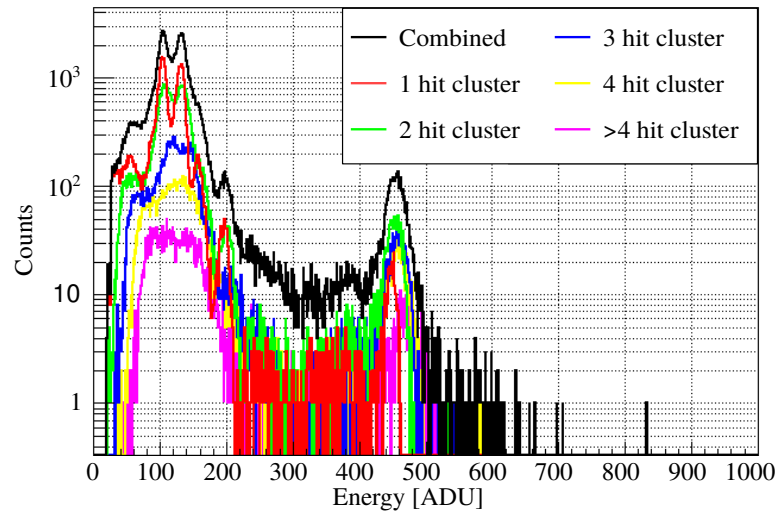


(C) FZ(n) wafer, CPA(small) sub-matrix, high pre-amplifier gain.

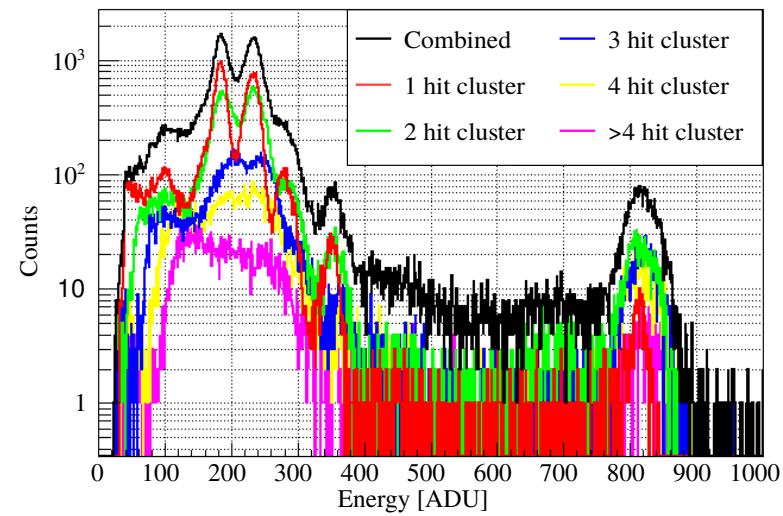
FIGURE 4.18: The examples of  $^{241}\text{Am}$  spectra taken with INTPIX6 FZ(n).



(A) DSOI(p) wafer, SF sub-matrix.



(B) DSOI(p) wafer, CPA(small) sub-matrix, low pre-amplifier gain.

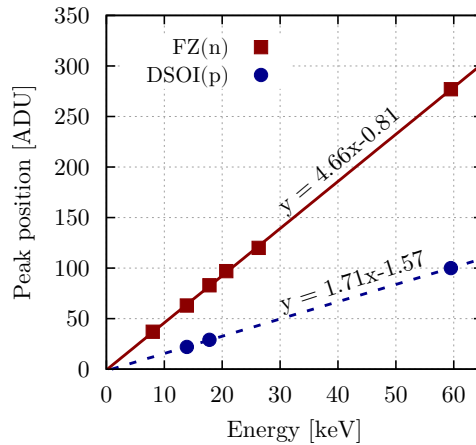


(C) DSOI(p) wafer, CPA(small) sub-matrix, high pre-amplifier gain.

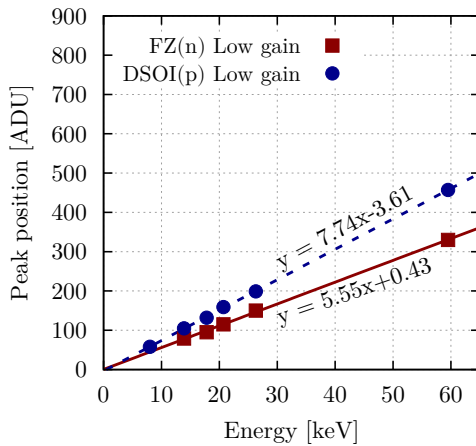
FIGURE 4.19: The examples of  $^{241}\text{Am}$  spectra taken with INTPIX6 DSOI(p).

be independent from the substrate wafer). Since such a behaviour was observed perpetually for all the measurements, its origin had to be investigated.

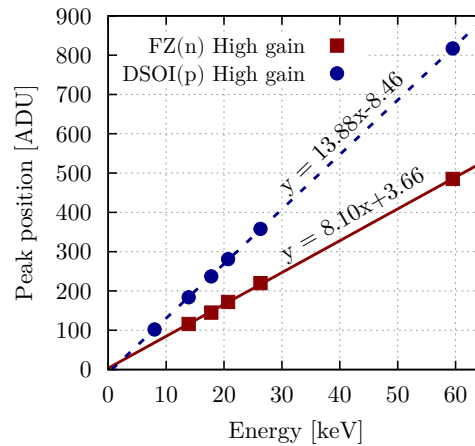
To examine this issue quantitatively the calibration plots for each configuration can be used, which are presented in Fig. 4.20 together with the fitted regression lines. First of all, it is worth to notice that all fitted curves are passing close to the origin, which is expected. Beside that, the linear coefficients ( $A_x$ ) can be translated into the charge to voltage conversion ratio of the input stage. For that purpose the voltage gain of the whole readout chain behind the input stage has to be estimated and the voltage corresponding to one ADC unit has to be known. The latter is determined by the ADC configuration and its value may be taken from the data sheet. In our case  $1 \text{ ADU} = 488 \mu\text{V}$  ( $G_{ADC} = \frac{488}{1} \left[ \frac{\mu\text{V}}{\text{ADU}} \right]$ ). The determination of the former is much more complex since it depends both on the PCB design as well as the chip design. In first approximation the amplification on PCB was set to unity ( $G_{PCB} = 1 \left[ \frac{\text{V}}{\text{V}} \right]$ ) and also the on-chip column amplifier gain was set to unity. However, because of slight differences in the in-pixel signal storage capacitances between the SF and CPA architectures, the effective gain of the column amplifier differs. Basing on the design it is equal to unity for CPA matrix



(A) Source-Follower.



(B) CPA(small) with low gain setting.



(C) CPA(small) with high gain setting.

FIGURE 4.20: Calibration curves for detector prototype designed in Cracow.

( $G_{chip}^{CPA} = 1 \left[ \frac{V}{V} \right]$ ), whereas for the SF matrix  $G_{chip}^{SF} = 0.9 \left[ \frac{V}{V} \right]$ . Assuming that 3.6 eV is needed to produce one electron-hole pair, one can obtain the charge to voltage conversion ratios ( $G_x$ ) for each configuration, according to:

$$G_x \left[ \frac{V}{fC} \right] = A_x \left[ \frac{ADU}{eV} \right] \cdot 3.6 \left[ \frac{eV}{e^-} \right] \cdot 6241.5 \left[ \frac{e^-}{fC} \right] \cdot G_{chip} \left[ \frac{V}{V} \right] \cdot G_{PCB} \left[ \frac{V}{V} \right] \cdot G_{ADC} \left[ \frac{V}{ADU} \right] \quad (4.20)$$

The combined results of the measured and simulated charge to voltage conversion ratios for each configuration are presented in Tab. 4.3. Now the high discrepancy of the results obtained for the charge pre-amplifiers on different wafers is clearly visible. Beside that, for both wafers and both gain settings there is also a significant deviation from the values expected from the simulations.

Architecture	Gain	FZ(n)	DSOI(p)	Sim
SF	—	0.0460	0.0169	—
CPA	Low	0.0609	0.0849	0.1111
	High	0.0888	0.1522	0.2422

TABLE 4.3: Measured and simulated charge to voltage conversion ratios of the input stage for different architectures and wafers, given in  $\left[ \frac{V}{fC} \right]$ .

The conversion ratios are directly determined by the capacitances in the input stage (total input capacitance in case of the SF architecture and feedback capacitance for the CPA – as described in Sec. 4.1). Therefore, from the measured conversion ratios one can calculate the experimental values of the corresponding capacitances ( $C_{IN}$  and  $C_F$ ). It can be done according to the equations 4.1 and 4.4 introduced previously.

The resulting capacitances are presented in Tab. 4.4. First of all, basing on the results for the SF matrix it is clear that introducing an additional Middle Si layer (DSOI(p) case) highly increases the detector capacitance. This is not obvious, since in the standard approach the sensor capacitance is usually determined by the plate capacitor formed between the sensing implant and the back plane (or the end of the depletion zone for not fully depleted devices). Whereas, here the origin has to be different, since even taking into account different thicknesses of the depletion depths for these two sensors, such a difference can not be explained.

Architecture	Gain	FZ(n)	DSOI(p)	Sim
SF	—	21.75	59.26	—
CPA	Low	16.43	11.78	9.38
	High	11.26	6.57	4.17

TABLE 4.4: Experimentally estimated and intended capacitances determining the gain of input stage (total input capacitance for SF architecture and feedback capacitance for CPA) for different wafers, given in  $[fF]$ .

To estimate the total input capacitance of the detector fabricated on the standard SOI structure, one has to take into account also the coupling between the sensing implantation and the electronics. As presented in Fig. 4.21A in the standard SOI the parasitic capacitances

to the transistors diffusion layer appear. Since the distance between the sensing implant and transistor layer is usually few orders of magnitude lower than the distance to the back plane, these capacitances provide a significant contribution to the total capacitance. Thus for the standard SOI, to determine the total capacitance of the input node one has to take into account the dispersed capacitance to the electronics, the coupling to the back plane, as well as the gate capacitance of the input transistor.

The situation looks different for the Double SOI wafers, where the Middle Si layer separates the sensing implant from the electronics, as sketched in Fig. 4.21B. Thus in this case instead of the dispersed capacitance to the electronics one has to take into account the coupling between the sensing implant and the Middle Si. Its contribution is even more pronounced since the Middle Si covers almost the whole sensor area. Moreover, the insulator thickness separating appropriate layers is usually lower in the Double SOI case, which further emphasise the differences. This explains qualitatively the significant difference in the total input capacitance observed for the SF matrix.

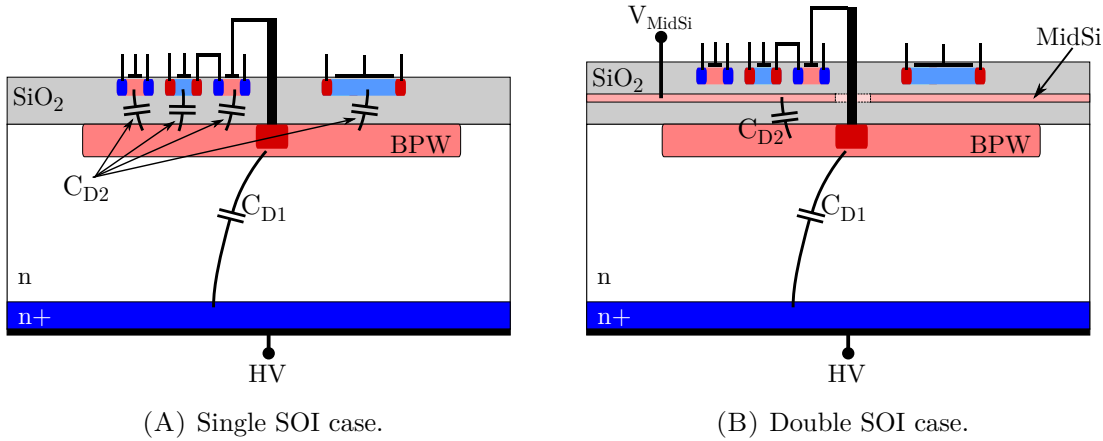


FIGURE 4.21: Elementary sensor parasitic capacitances contributing to the total input capacitance.

The precise estimation of the parasitic coupling between the sensing implant and electronics ( $C_D^{par}$ ) is impossible without a proper tools, but one can try to estimate it assuming that each component forms a plate capacitor with the BPW layer:

$$C_D^{par} = \epsilon_0 \epsilon_r \frac{A}{d} \quad (4.21)$$

where:  $\epsilon_0$  and  $\epsilon_r$  are vacuum permittivity and relative permittivity of the insulator layer,  $A$  is the plate area and  $d$  is the distance between plates. The electronics active area can be taken directly from the layout, whereas the thickness of the silicon dioxide separating the electronics layer from the handling wafer is unfortunately not known precisely. According to the basic specification of the wafers it should be around 150 nm. This gives a  $C_D^{par}$  of about 7.5 fF for the standard SOI case. The input transistor gate capacitance is around 10 fF, which gives in total 17.5 fF. Taking into account the parasitic capacitance coming from the electronics interconnection, which should add several femtofarads, it agrees very well with the measured value of 21.75 fF.

For the Double SOI the effective plate area of the parasitic contribution is imposed by the BPW layer size. Thus for this wafer the coupling between BPW layer and the Middle Si gives above 40 fF. Including 10 fF from the input transistor and the interconnections it also matches the measured 59.26 fF.

Now moving to the puzzling behaviour of the charge pre-amplifiers, one may suspect that it originates in insufficient open loop gain, since its high value is required to become independent from the input node capacitance. But in such a case the larger the detector capacitance the higher signal deterioration should be observed. As already presented, based on the results for the SF matrix, the sensor capacitance for the DSOI(p) is much larger than for the FZ(n), thus eventual signal degradation would mostly appear on the DSOI(p) wafer. Since the effect is completely opposite and what's more, there are no differences between the sub-matrices with small and large sensing node, the open loop gain of the pre-amplifier has to be large enough. Therefore the spotted issue most probably originates in the discrepancy in the feedback capacitance.

One can notice that for the DSOI(p) wafer the difference between the designed capacitance and the measured one is almost identical for both low and high pre-amplifier gain settings. This additional 2.4 fF can be attributed to the parasitic capacitance introduced by the electronics interconnections. Unfortunately, since the used technology is not fully parametrized, the parasitic extraction tool can not be used to anticipate its value, but several femtofarads are expected.

Even if the situation seems to be clear for the DSOI(p) wafer, it does not explain the further capacitance increase for the single SOI. In principle the parasitic capacitance coming from the interconnections should not depend on the substrate, thus there has to be an additional factor revealing only on the single SOI wafer. Also in this case the difference between simulation and measurements is very similar independently from the gain settings, which means that most probably it also comes from some parasitic capacitance parallel to the feedback capacitance. Subtracting 2.4 fF coming from the interconnections, there is still about 4.7 fF from unknown source. Having in mind the differences between the standard SOI and Double SOI spotted with the SF matrix one can find out that similar mechanism may cause the observed behaviour. Since in the standard SOI there is a significant coupling between the electronics layer and the sensing implantation, all of the source and drain terminals belonging to the pre-amplifier output node are forming a capacitance parallel to the feedback capacitance, as it is presented in Fig. 4.22. Its value obtained by a rough estimation is around 3 fF. Now, concerning the Double SOI there is no direct coupling between the electronics layer and sensing node since they are shielded by the Middle Si layer, thus there is no additional capacitance between the input and output of the pre-amplifier. So finally, after taking into account all the discussed effects, the outcomes from the  $^{241}\text{Am}$  source measurement results that looked a bit strange on the first glance, can be fully understood. Moreover, they have provided an important knowledge about the SOI technology for future designs.

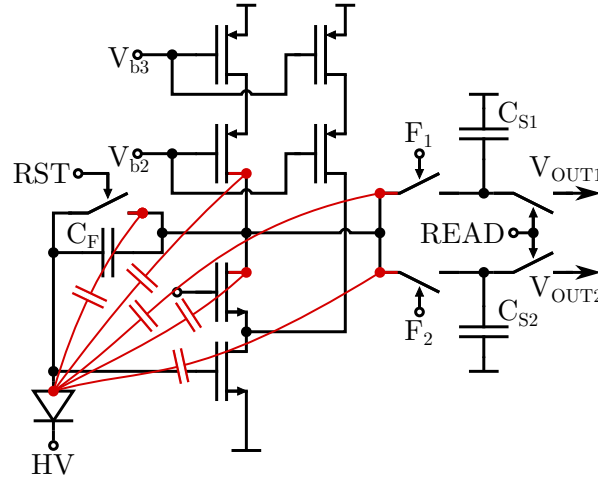


FIGURE 4.22: Parasitic capacitances between the sensing node and pre-amplifier output influencing its charge to voltage conversion coefficient.

#### 4.6.1 Energy resolution

Once having the energy calibration done, the measured pixel noise given in the arbitrary *ADU* units can be recalculated into the ENC (introduced in Sec. 3.6 on page 44). The example of pixel noise spectra for both the FZ(n) and DSOI(p) wafers are shown in Fig. 4.23 separately for all sub-matrices, with the mean values (after boundary pixel rejection) given in the legend. Since for the most conclusive sub-matrices (SF and CPA(small)) the noise dependence from the back bias voltage was marginal (as shown in Fig. 4.15C), the results will be presented only for the default conditions. These are 70 V for the FZ(n) wafer (its full depletion voltage) and  $-50$  V for the DSOI(p) (highest voltage without strange leakage occurrence).

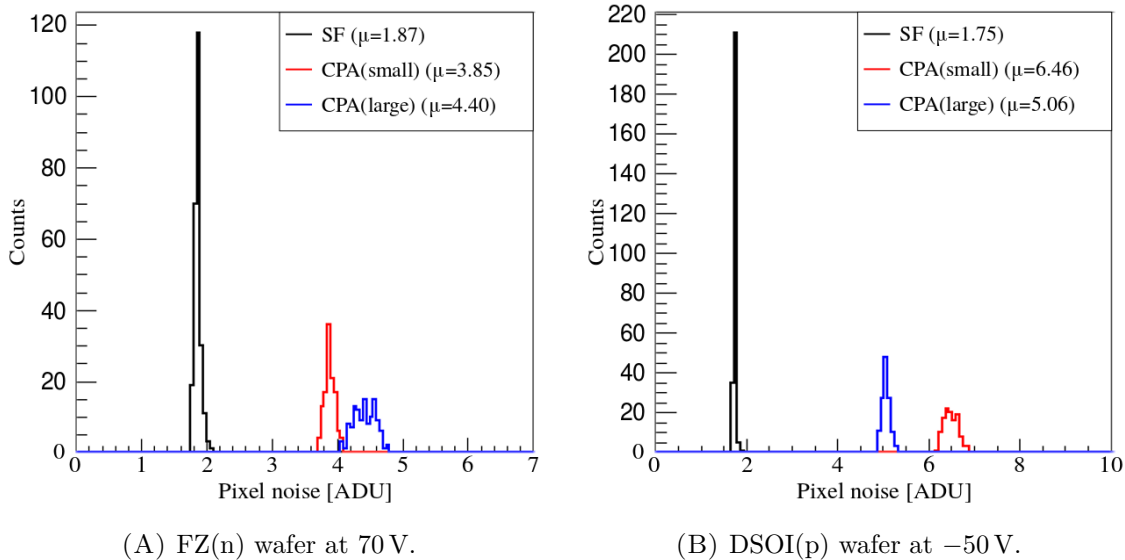


FIGURE 4.23: Example of pixel noise spectra for each sub-matrix.

The mean pixel noise values for all different cases are summarized in Tab. 4.5 for consistency, whereas much more conclusive values of the corresponding ENC are presented in



Tab. 4.6. The results for the CPA(large) on the FZ(n) wafer are marker with red to remind that these values may not be representative because of the issue spotted on this sensor geometry (introduced in Sec. 4.5).

Wafer	Pre-amp Gain	SF	CPA(small)	CPA(large)
FZ(n)	low	1.87	3.19	<b>3.13</b>
	high		3.85	<b>4.40</b>
DSOI(p)	low	1.75	4.54	3.79
	high		6.46	5.06

TABLE 4.5: Mean pixel noise given in ADU (FZ(n) wafer at 70 V, DSOI(p) wafer at  $-50$  V).

Wafer	Pre-amp Gain	SF	CPA(small)	CPA(large)
FZ(n)	low	111	160	<b>157</b>
	high		132	<b>150</b>
DSOI(p)	low	284	163	136
	high		129	101

TABLE 4.6: ENC values for all sub-matrices on different wafers, given in electrons (FZ(n) wafer at 70 V, DSOI(p) wafer at  $-50$  V).

As one can see for the FZ(n) wafer the best performing sub-matrix is the one with the source-follower in the input stage having the ENC of 111 electrons. The CPA architecture with high gain behaves slightly worse, with about 20 electrons more. On the DSOI(p) wafer the SF performance is highly degraded, which is naturally driven by much higher sensor capacitance. With this substrate the usage of charge pre-amplifier architecture is much more beneficial. The noise performance of the CPA(small) seems to be almost independent on the wafer showing roughly the same ENC value of about  $130 e^-$  for the high gain and  $160 e^-$  for low.

In spite of the incomprehensible behaviour of the CPA(large) sub-matrix on the DSOI(p) wafer after exceeding  $-50$  V, for lower back bias voltages this architecture provides the best energy resolution with the ENC of  $101 e^-$  for the high gain. It is not clear why there is such a difference in favour of the large collection diode and unfortunately it can not be cross-checked with the results from the FZ(n) wafer.

Beside the conclusions regarding the best performing architecture, it is worth to notice almost a constant difference in ENC of about  $30 e^-$  between the low and high pre-amplifier gain setting for all conclusive results for the CPA architecture. This suggests that a significant amount of noise comes from the readout electronics located after the pre-amplifier. Thus, if the signal becomes amplified in the input stage the relative influence from the further noise sources becomes less substantial.

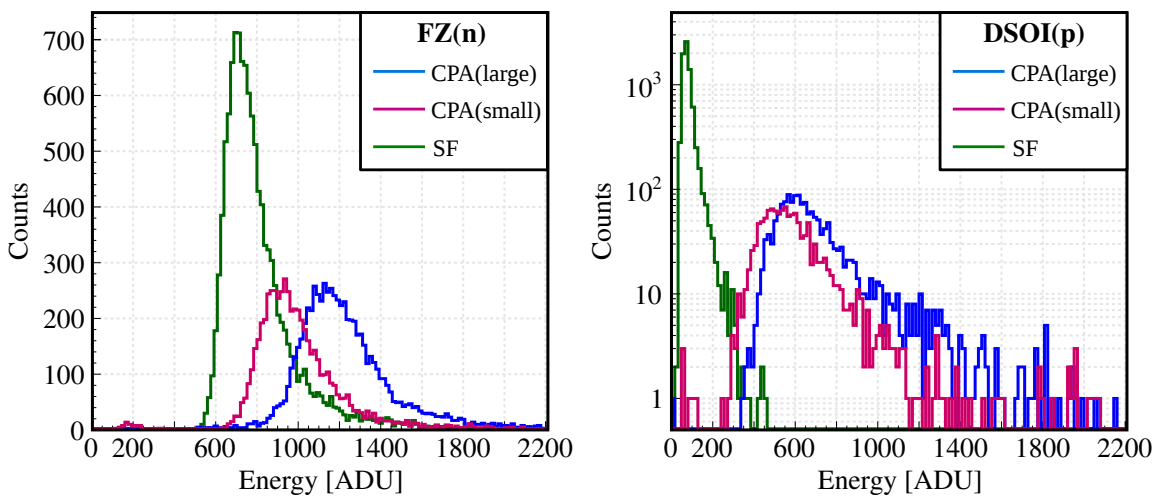
Summarizing, the observed performance providing the ENC values close to  $100 e^-$  is a very good result, especially taking into account that it was obtained with a test device. What is even more promising, it seems that there is still quite a lot of room for further improvements in terms of the energy resolution, since all of the noise sources after the input stage may be further suppressed by a proper readout electronics design.

## 4.7 Spatial resolution

Beside the spectroscopy capabilities, for some applications the spatial resolution and tracking potential are of the main interest, as for example in the vertex detector of high energy physics experiment. The spatial resolution usually depends on the precision of the charge measurement (at least for non-binary readouts), but the overall tracking performance is a way more complex subject. Thus, the separate studies, aimed to verify the spatial resolution of the presented device, were performed by the other member of the group [41]. Despite the results are not directly obtained by the author of this thesis, it is worth to quote the most relevant results to get thorough overview of the detector performance.

The studies of the spatial resolution were performed in CERN SPS North Area at H6 beam line in collaboration with the CLICdp group. For that purpose a pion beam of 120 GeV was used. The examples of energy spectra from the beam tests are presented in Fig. 4.24A and Fig. 4.24B for the FZ(n) and DSOI(p) wafer respectively. At 120 GeV pions can be treated as the minimum ionising particles (MIP), thus the energy distributions undergo the Landau distribution (or precisely speaking the convolution of Landau and Gaussian functions).

Since for the MIP-like particles ionisation takes place along their whole path within the sensor, they can be used to study the depletion depth. For that purpose a set of measurements with different back bias voltages were performed. The combined results are shown in Fig 4.25, where the most probable value (MPV) of the measured energy is plotted in a function of the square root of back bias voltage. As it can be seen for the FZ(n) wafer the measured energy grows proportionally to the depletion depth and saturates at around 70 V, when the full depletion is reached. Thus, for the FZ(n) wafer the full depletion voltage is 70 V. Knowing the full depletion voltage and the sensor thickness one can estimate the substrate resistivity according to equation 1.11 (introduced on page 7). Obtained resistivity is around 12.3 k $\Omega$ cm, which is much higher than 2 k $\Omega$ cm declared by the manufacturer.



(A) FZ(n) wafer at 130 V.

(B) DSOI(p) wafer at  $-70$  V.

FIGURE 4.24: Examples of energy spectra from the beam test data. Obtained with 120 GeV pions. Plots from [41].

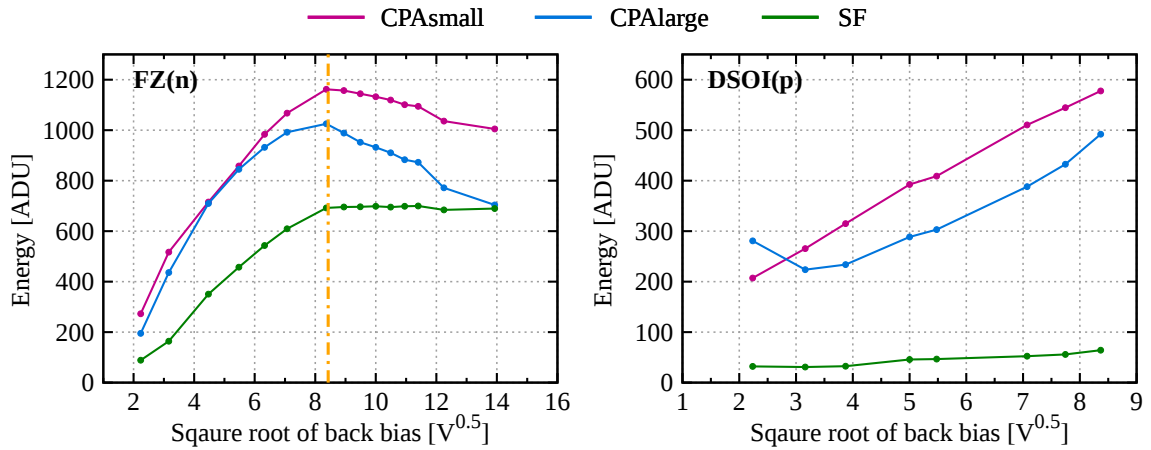


FIGURE 4.25: Most probable value of energy deposited by 120 GeV pions in function of square root of back bias voltage. Plots from [41].

One can also notice that the most probable energy value literally saturates after 70 V only for the SF sub-matrix, whereas for the both CPA sub-matrices it starts to decrease slightly. Unfortunately, the origin of such behaviour was not found.

In case of the Double SOI, it is clear that the full depletion has not been reached, since there is no plateau region. Assuming that the amount of charge induced per travelled distance is the same for both wafers, and taking into account the measured charge to voltage conversion ratios, one can conclude that the DSOI(p) wafer can be depleted up to about 150  $\mu\text{m}$ .

Finally, the spatial resolution in function of back bias voltage is presented in Fig 4.26. For the FZ(n) wafer all matrices show a very good performance, with the resolutions below 3  $\mu\text{m}$  after the full depletion. The best result is obtained with the SF sub-matrix which reaches  $\sim 2.3 \mu\text{m}$  at 100 V.

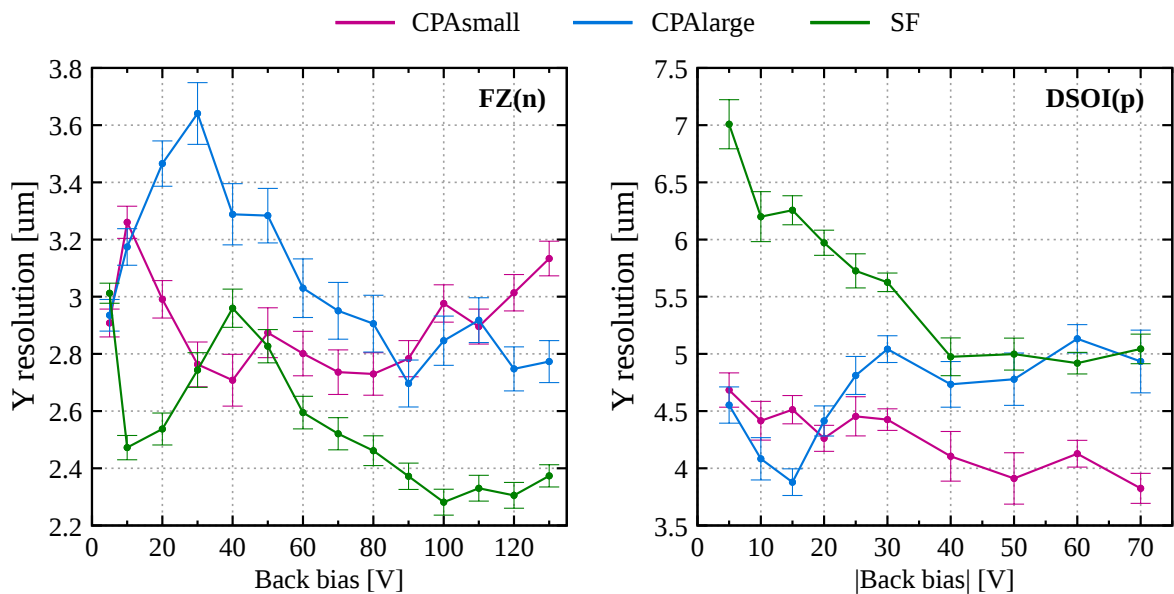


FIGURE 4.26: Plots showing the spatial resolution in function of back bias voltage, separately for each sub-matrix and wafer type. Plots from [41].

For the Double SOI the results are slightly worse. The performance of SF matrix on the DSOI(p) is naturally deteriorated by the high sensor capacitance. Whereas the spatial resolution of the CPA architecture (which is much less sensitive to the increased sensor capacitance) fluctuate between 4 and 5  $\mu\text{m}$ . The direct comparison between these two wafers is not straightforward. One has to remember that there is a significant difference in the input signal amplitude between the FZ(n) and DSOI(p), in favour of the first one. This is caused by the problems with full depletion of the DSOI(p) sensor.

## Chapter 5

# CLIPS detector design

After the very promising results obtained with the first detector it was decided to design a next one, however no longer a general purpose test device, but this time targeting a specific application. Since group of AGH University has been already involved in several designs of detectors for high energy physics experiments, it was a natural direction. The choice fell on the vertex detector for the Compact Linear Collider (CLIC) experiment. Since it is a lepton collider, the main weakness of the SOI devices, which is the poor TID radiation hardness, is not an issue. The radiation levels even for the vertex detector (located closest to the interaction point) are low enough.

CLIC is currently during advanced R&D phase and so there are intensive searches for novel solutions able to fulfil its demanding specifications. The SOI seems to be a very attractive technology for the tracking devices, since there are almost no limitations in terms of pixel granularity and so a very fine spatial resolution can be achieved. Thanks to its monolithic nature the SOI detectors come ahead the growing demands on the material budget limitation. Moreover, there is a full CMOS process available, which is necessary to provide all the functionality required from the on-chip readout electronics. Beside that, currently there is no device which is able to simultaneously meet all the requirements set for the CLIC vertex detector, so it is a good opportunity for developing a state-of-the-art detection system.

The main requirements for a single plane of the CLIC vertex detector are presented in Tab. 5.1. To fulfil all of them simultaneously, substantial modifications have to be implemented comparing to the previous design. First of all, a single point resolution below  $3\ \mu\text{m}$  has to be obtained with much thinner sensor. Moreover, in the first design the measurement of the arrival time was not considered, thus an additional functionality has to be added. There are also strong restrictions on the power consumption because of the cooling system based only on the air flow. Fortunately, there is a relatively long time (about 20 ms) between very short (156 ns) bunch trains. Such a low train repetition rate allows to highly decrease the overall

Material budget	$0.2\%X_0$ ( $<150\ \mu\text{m}$ of silicon)
Spatial resolution	$3\ \mu\text{m}$
Time stamping (time resolution)	10 ns ( $10/\sqrt{12}$ ns)
Power consumption	$50\ \text{mW cm}^{-2}$

TABLE 5.1: Requirements for the single plane of CLIC vertex detector ( $X_0$  stands for the radiation length).

power consumption by the so-called power pulsing, which means that the most of the readout electronics is switched on only for a short time when the collisions take place. To provide a detector able to meet these requirements the design of the CLIPS (CLIC Pixel SOI) chip has been started.

## 5.1 CLIPS detector overview

Similarly to the previous design, also here few different approaches have been implemented. The chip comprise three different, fully independent matrices (see Fig. 5.1). Beside that there is a slow control block, common for the whole chip, and a test structure which allows for deeper investigation of the in-pixel electronics performance. Thanks to much larger chip area, comparing to the design described in the previous section, the size of each matrix is significantly bigger. Now they consists of  $64 \times 64$  pixels, which should be very beneficial in terms of the boundary effects suppression as well as the better statistics.

The differences between the matrices are minor and mostly refer to the modification of sensor layout or pre-amplifier feedback capacitance. Thus, at first a general overview of the design will be presented, while the variations between the matrices will be discussed later.

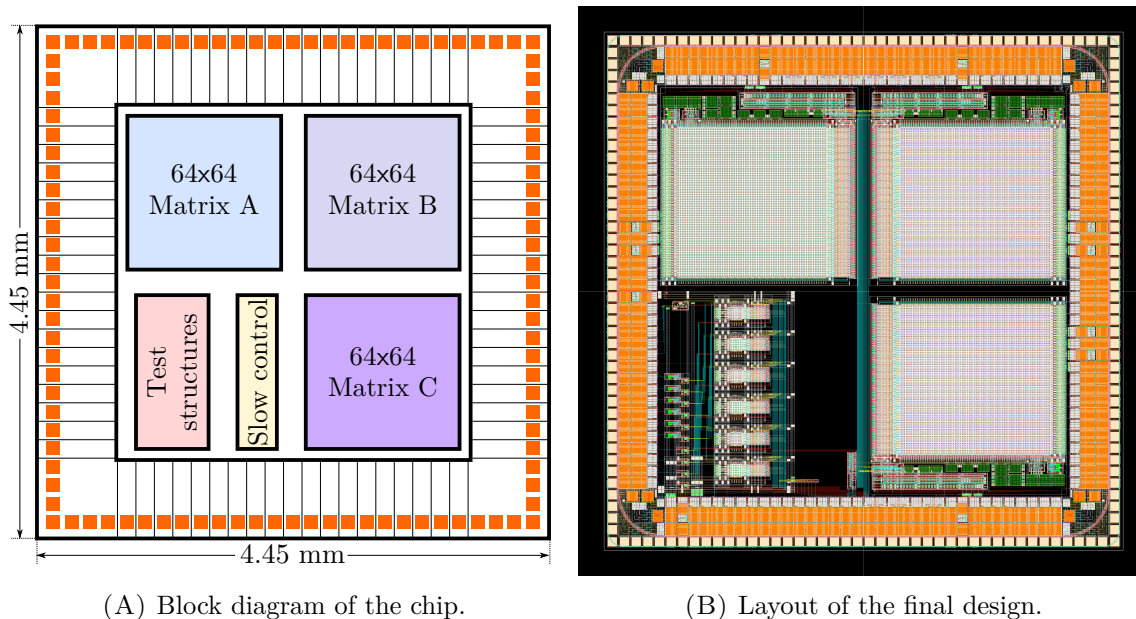


FIGURE 5.1: Block diagram and layout of the CLIPS detector.

## 5.2 Pixel design

Thinning the sensor down to  $100 - 150 \mu\text{m}$  highly suppresses the charge diffusion within a sensor volume. Thus the charge sharing between neighbouring pixels is also limited. Unfortunately to obtain a good spatial resolution it is essential to have the signal divided between several pixels. For this reason, to maintain the resolution obtained with the previous design, the pixel size should be decreased. The aim was to reduce it to  $20 \mu\text{m} \times 20 \mu\text{m}$ , but it directly introduced a high limitation on area available for the in-pixel circuitry. Despite the reduction

of available area, additional functionality of the particle Time-of-Arrival (ToA) measurement needed to be implemented. This extorts the usage of nonstandard solutions, providing a desired functionality, but limiting the utilized area. The overview of CLIPS in-pixel circuitry is shown in Fig. 5.2, where the different functional blocks are highlighted with different colors.

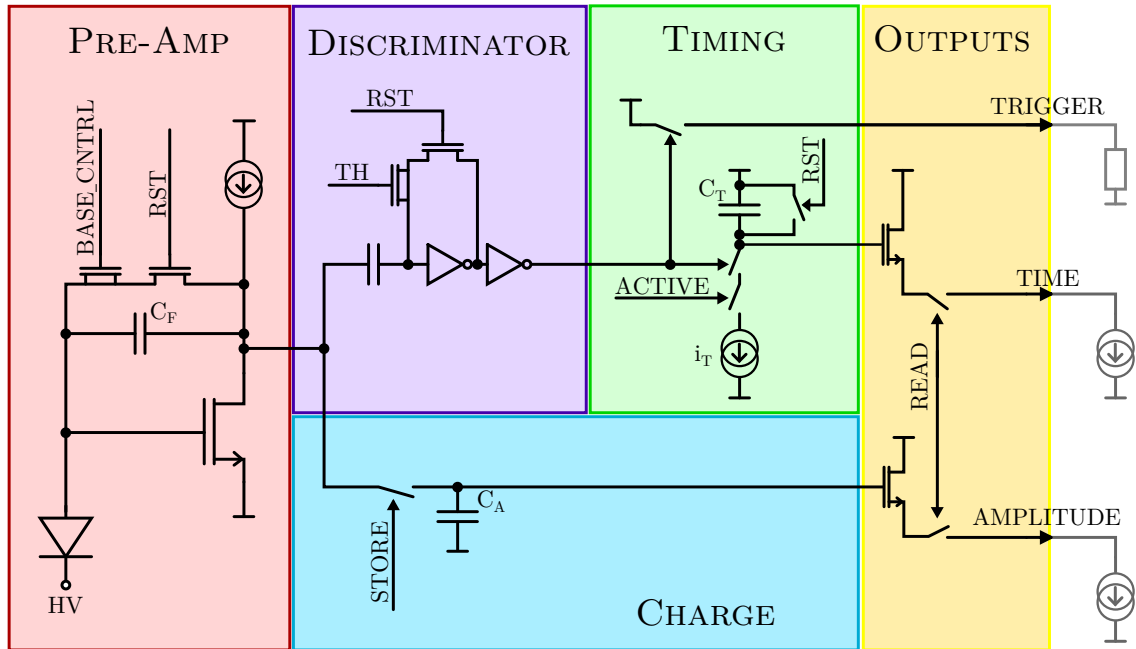


FIGURE 5.2: CLIPS pixel schematic.

### 5.2.1 Pre-amplifier

Due to the mentioned area limitations, the pre-amplifier had to be simplified even further in comparison with the design described in previous section. The telescopic cascode architecture was replaced by a simple common source configuration. This reduces the total number of required transistors, but also has a negative impact on the pre-amplifier performance. The stability simulation results comprising both, the open loop gain and output signal phase are shown in Fig. 5.3. Comparing to the previous prototype, the open loop gain of the CLIPS pre-amplifier has decreased (to the level of about 40 dB) because it is no longer boosted by the gain of cascode transistor. Thus, according to equation 4.4 (on page 55), the contribution from the sensor capacitance to the overall charge to voltage conversion ratio of the input stage can not be fully neglected. Even though, with the gain value above 100 it should be large enough to significantly suppress its influence. The total capacitance of the input node is estimated to be below 30 fF, even for the worst case scenario. Therefore, its contribution to the overall charge to voltage conversion ratio should not exceed the equivalent of additional 0.3 fF in feedback capacitance. A broader discussion on the feedback capacitance will be presented in separate section dedicated to the differences between matrices, since there are several approaches regarding its implementation.

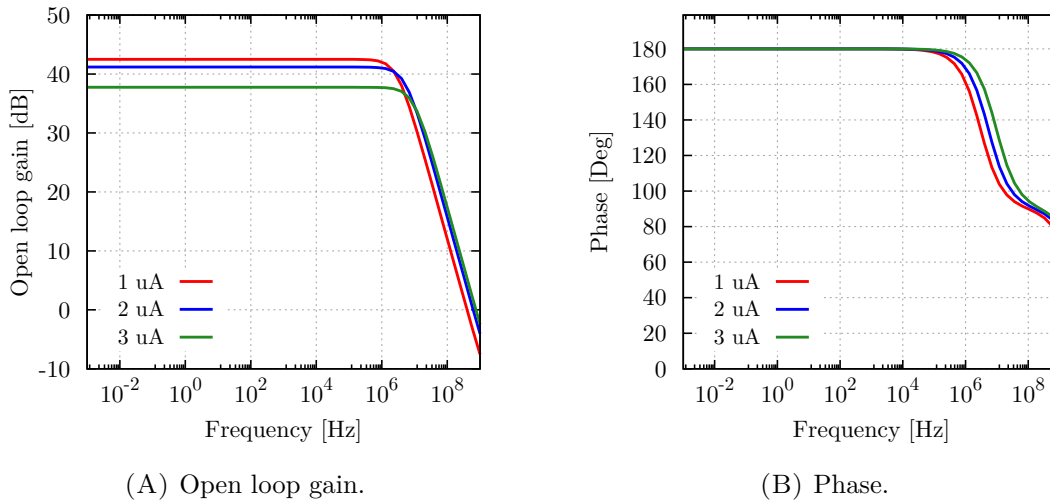


FIGURE 5.3: AC characteristics of the CLIPS pre-amplifier.

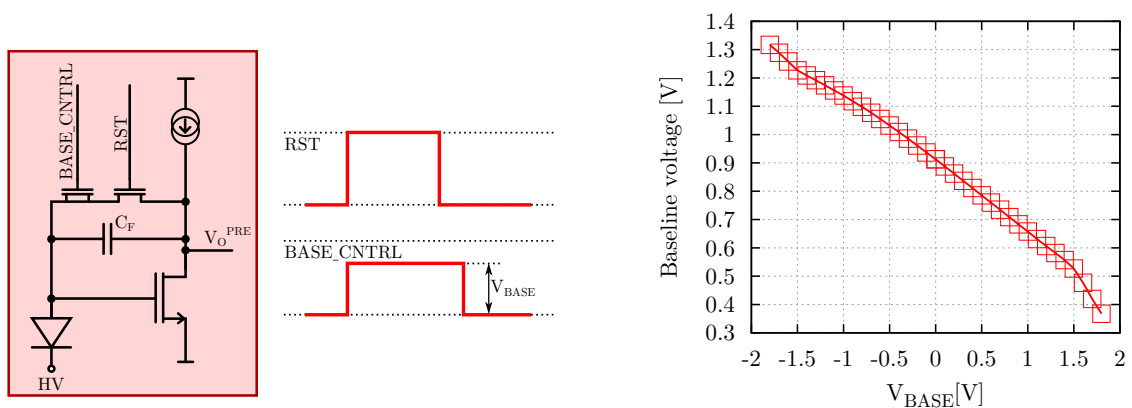
### 5.2.2 Baseline adjustment

The DSOI(p) wafer has been chosen as a primary substrate, mainly due to its radiation hardness potential. Thus the input stage electronics was optimised for the p-type sensor. But since the foundry may also deliver chips fabricated on other substrates, it was very desired to provide the flexibility in terms of the input signal polarity. It can be achieved by setting the baseline in the middle of the available output voltage range, but this solution is strongly limiting the input dynamic range. Therefore it is much more desired to have the possibility of setting an adequate baseline voltage depending on the sensor type.

For that reason, a novel baseline voltage adjustment technique was implemented. It uses the effect of charge injection from the transistors working as a switch, which is usually very undesirable. This issue has been already discussed in Sec. 4.1.1 (on page 58), together with a possible solutions for the suppression of this effect. Here the idea of having a dummy transistor which “consumes” the redundant charge has been pushed further. Since the charge injected from the reset switch into the input node changes the baseline value, instead of minimising this effect one can exploit it. In the resetting branch, which is shown in Fig. 5.4A, an independent *BASE\_CNTRL* signal is connected to the gate of the dummy transistor instead of negated reset signal ( $\overline{RST}$ ). Since the amount of the charge injected from the transistor channel depends on the gate-source voltage, the charge injection can be controlled by the *BASE\_CNTRL* signal amplitude ( $V_{BASE}$ ). Ensuring that the dummy switch closes (or opens) just after the reset phase it directly changes the baseline voltage value ( $V_O^{PRE}$ ).

The simulation results showing a baseline voltage ( $V_O^{PRE}$ ) in function of *BASE\_CNTRL* signal amplitude ( $V_{BASE}$ ) are presented in Fig. 5.4B. The positive  $V_{BASE}$  values correspond to the *BASE\_CNTRL* signal polarity opposite the *RST* polarity, whereas the negative values to the same polarity of both signals. One can see that the proposed mechanism can be used to change the baseline voltage in a broad range, from roughly 0.4 V up to 1.3 V, which covers most of the output dynamic range.





(A) Pre-amplifier scheme, with waveforms of steering signal used for baseline adjustment. (B) Baseline voltage level ( $V_O^{PRE}$ ) in function of  $V_{BASE}$  amplitude.

FIGURE 5.4: Baseline adjustment system.

The most important feature of the proposed solution is that it provides the new functionality without any additional power and area consumption. However, it does not allow for an independent baseline setting of each pixel, only common for the entire matrix, thus any pixel to pixel baseline variation can not be compensated.

### 5.2.3 Charge measurement

The charge measurement is done based on the same concept as in the design described in previous section, in which the voltage level on the output of the pre-amplifier directly corresponds to the amount of charge injected to its input. Since in the input stage there is a charge-sensitive pre-amplifier, the charge to voltage conversion ratio is mainly determined by the feedback capacitance. In this design it was desired to have as large conversion ratio as possible. This was driven by two reasons, first of all, as already mentioned, it is planned to thin down the sensor, and so the expected input signal is only about 1 fC. Beside that the measurements of the first prototype show that the higher signal on the pre-amplifier output, the better signal to noise ratio. Moreover, in terms of the discriminator performance, it is also very desired to have as high voltage signal from the pre-amplifier as possible. Thus to maximize the charge to voltage conversion ratio several different approaches of the feedback capacitance were implemented.

The simulated voltage response of the pre-amplifier in function of injected charge is presented in Fig. 5.5. The results are shown for the default readout electronics configuration (for the details see the section 5.4, where the differences between matrices are explained). The voltage change on the pre-amplifier output and on the pixel output (after the output buffer) are shown separately. The simulated charge to voltage conversion ratio for the default configuration is about  $0.5 \frac{V}{fC}$ , but one has to remember that it does not include parasitic components, which can not be neglected. The linear dynamic range for the input charge is around 1 fC and it is limited from the top by the voltage swing on the output of the pre-amplifier, whereas from the bottom by the output buffer.

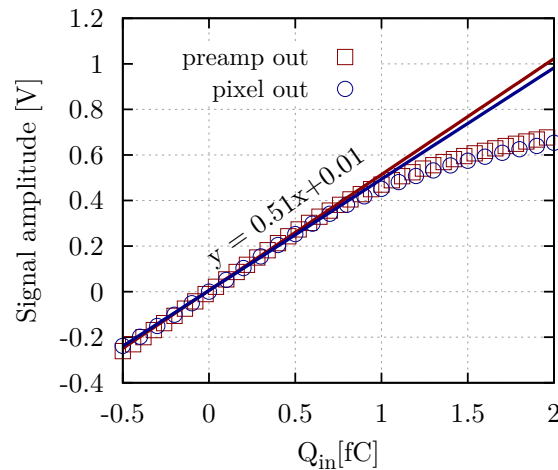


FIGURE 5.5: CLIPS pixel response to the injected charge, measured directly on the pre-amplifier output *preamp out* and on the pixel output *pixel out* (after the in-pixel buffer).

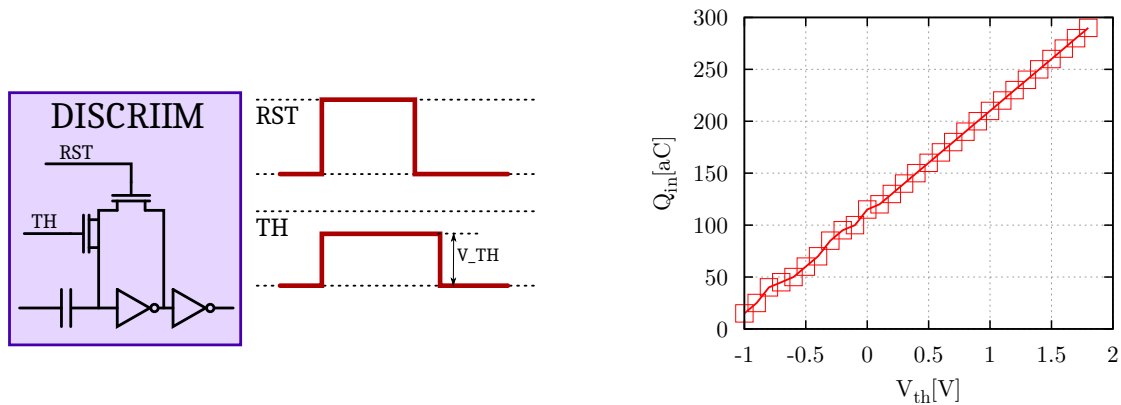
As one can notice from Fig. 5.2, the sample and hold block has changed in comparison to the previous design. The CDS is no longer utilized, only a single switch and capacitance is implemented due to the area limitations.

#### 5.2.4 Discriminator and Time-of-Arrival measurement

To provide the functionality of Time-of-Arrival measurement, it was necessary to add discriminator to the in-pixel circuitry. Unfortunately, the commonly used solutions are too complex to fit into the  $20\ \mu\text{m} \times 20\ \mu\text{m}$  pixel. Thus just a chain of two inverters capacitively coupled to the pre-amplifier output are utilized for that purpose (already introduced in another SOI detector [42]). During the reset phase the input of the first inverter is being shorted with its output, thus it is set to a semi-stable transition state where both nMOS and pMOS transistors are conducting. Therefore, a small voltage change on its input will be enough for the transition from this undefined state into a well defined high or low state (depending on the input signal polarity). Such a solution itself would be highly unpredictable since in principle it may go out from the semi-stable state on any voltage fluctuation. But one can notice that after the reset, the input node of the first inverter does not have any dc-connection, thus to ensure its initial state a charge injection mechanism can be exploited (similar as for the baseline setting). Moreover, it can be also used for the threshold voltage adjustment, since the amount of injected charge directly corresponds to the minimum amplitude of the input signal needed to change the inverter state.

This mechanism is schematically presented in Fig. 5.6A. Similarly to the baseline adjustment, the discrimination threshold level is set by changing the voltage step amplitude ( $V_{TH}$ ) of the *TH* signal. The simulation results showing the discrimination levels expressed in the input charge in function of  $V_{TH}$  are shown in Fig. 5.6B. The positive  $V_{TH}$  corresponds to the situation when both *RST* and *TH* signals have the same polarity, whereas the negative values

mean that the  $TH$  polarity is opposite. The results are presented for the default pixel configuration. In these conditions the threshold can be set from zero up to 0.3 fC, which is around 30% of the expected input charge.



(A) Discriminator circuitry, with waveforms of steering signal used for threshold adjustment.

(B) Minimal input signal needed to trigger the discriminator in function of  $V_{TH}$ .

FIGURE 5.6: Sketch showing the working principle of discriminator circuitry and its simulated threshold values.

Same as for the baseline, only a global discrimination level can be set. There was no space for independent fine tuning on single pixel level. Since the amount of charge in the transistor channel depends on its width and length, any fluctuation of these parameters during the production will result in the dispersion of the threshold level over the matrix. This may be the main issue of the proposed solution. Unfortunately, it can not be verified by the simulations since the technology vendor does not provide necessary Monte-Carlo models. Thus only the measurements of the fabricated devices may show how big are the pixel-to-pixel threshold variations and how they affect the overall timing performance.

Beside the discrimination, a circuitry able to register the particle arrival time is needed. The standard approach is to implement a counter in each pixel and store the ToA information in digital form. But for relatively large technology size (which 200 nm process certainly is, when thinking about the digital circuitry) this solution would consume too much area to fit within pixel. Moreover, it also requires the distribution of a fast clock over the whole matrix, which is very unfavourable in terms of the analog circuitry performance. Therefore a different technique of ToA measurement had to be utilized.

A circuitry responsible for recording the particle arrival time is presented in Fig. 5.7. The ToA information is stored in the analog form, as a voltage across the  $C_T$  capacitance. The basic principle of the proposed solution is as follows. After the reset phase both plates of  $C_T$  capacitance are set to the power supply voltage ( $V_{DD}$ ). If the discriminator (*DISCRIM*) fires during the *ACTIVE* phase, both switches will start to conduct and so the  $C_T$  capacitance starts to be charged with a constant current  $i_T$ . This will result in a linear voltage drop at the bottom plate of the capacitance ( $V_T^{PIX}$ ). Charging will stop when the *ACTIVE* time finish, and so the voltage level stored on the  $C_T$  capacitance will correspond to the ToA.

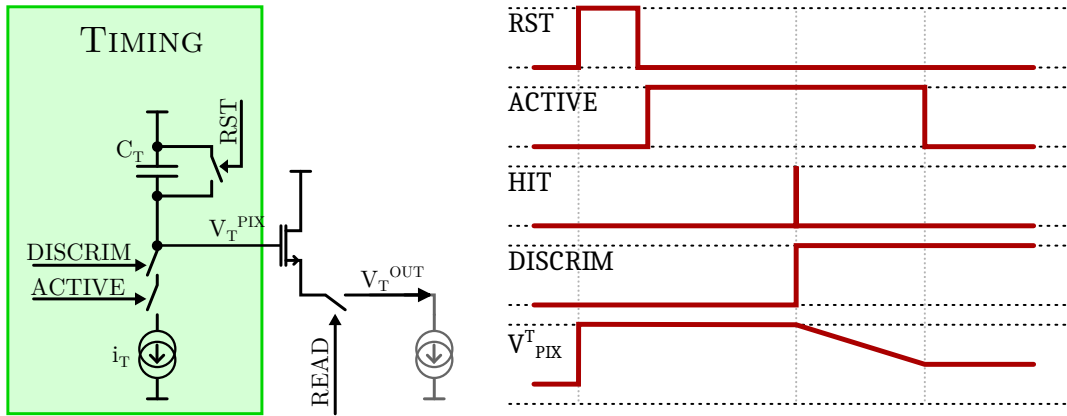


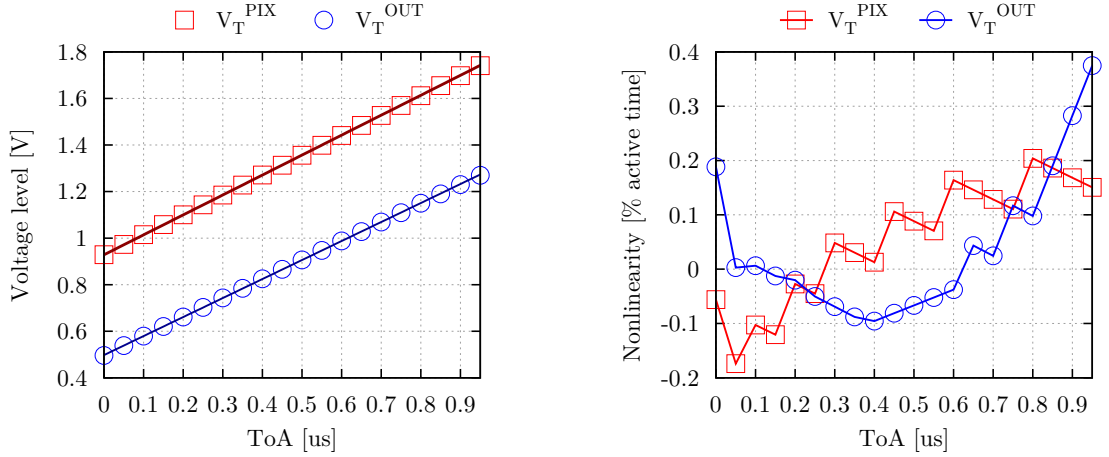
FIGURE 5.7: The scheme of the timing block, with waveforms showing its operation.

Proposed mechanism of ToA measurement is very flexible regarding the integration phase duration. One only needs to set the desired *ACTIVE* length ( $\tau_A$ ) and proper  $i_T$  current. The voltage across the  $C_T$  capacitance is given by  $V = \frac{Q}{C_T}$ , where  $Q = i_T \cdot \tau_A$ , so the current needs to be set to  $i_T = \frac{V \cdot C_T}{\tau_A}$ . Of course the  $i_T$  current can not be infinitely low, because of the technical implementation limitations. Thus for the long integration time a large  $C_T$  capacitance is desired. Fortunately it is not the case for the CLIC experiment where the *ACTIVE* window (train duration) is only around 160 ns. In the final design the  $C_T$  capacitance is 105 fF, which allows to extend the *ACTIVE* time to several dozen of microseconds, which will be beneficial for the tests on the beam.

The simulation results showing the voltage level on the bottom plate of the  $C_T$  capacitance ( $V_T^{PIX}$ ) as well as the corresponding voltage on the output of the pixel ( $V_T^{OUT}$ ) in function of hit arrival time are shown in Fig. 5.8A, together with the fitted linear regression lines. The simulation was performed for 1  $\mu$ s long *ACTIVE* time.

The precision of the time measurement is restricted by the  $V_T^{OUT}$  voltage fluctuation. The shorter the integration time the larger  $i_T$  current can be set and so the voltage change per the time unit will be larger. This means that  $V_T^{OUT}$  voltage fluctuation will be less harmful to the time measurement accuracy. In other words, one can determine the relative ToA precision given in the percentage of the *ACTIVE* time, as shown in Fig. 5.8B. One can notice that the relative non-linearity is below 0.5%, which corresponds to 5 ns for the 1  $\mu$ s long *ACTIVE* time and should improve even further to  $\sim 1$  ns for the targeted conditions.

Unfortunately, this is not the only source of the inaccuracy of the ToA measurement. One has to take into account also the promptness of the discriminator response, which highly depends on the input charge as well as on the discrimination level. The simulation results showing the difference between the reconstructed ToA and true ToA in function of relative input signal (input charge  $Q_{in}$  divided by the threshold charge  $Q_{th}$ ) are shown in Fig. 5.9. On the first glance the differences seem to be quite significant, but even for a very conservative seed threshold the expected signal should exceeded it at least ten times. Moreover, the constant offset can be subtracted and so the expected discrepancy is in order of single nanoseconds.



(A) Simulated  $V_T^{PIX}$  and  $V_T^{OUT}$  voltage levels in function of hit arrival time with fitted linear regression lines.

(B) Relative differences between obtained ToA and fitted linear regression line in function of hit time.

FIGURE 5.8: Simulation results showing the operation of the timing block.

Beside that, this issue may be further reduced on the analysis level. Thanks to the accurate information about the input charge one may apply an offline timing correction.

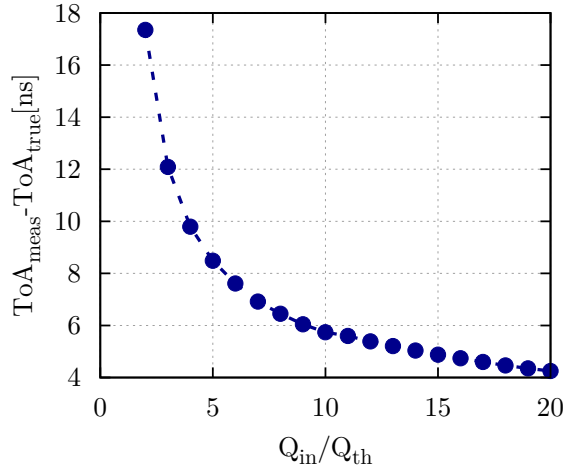


FIGURE 5.9: Difference between reconstructed and true ToA in function of injected charge to threshold charge ratio  $Q_{in}/Q_{th}$ .

Except for the mentioned issues, a significant pixel-to-pixel fluctuations are expected, since there are multiple factors that will affect the time reconstruction. Any deviation of the  $C_T$  capacitance or  $i_T$  current will directly affect the timing performance. In addition it is also indirectly dependent on the threshold voltage fluctuations, as well as on the charge to voltage conversion ratio of the input stage. Thus to neglect all these factors, an individual timing calibration is foreseen for each pixel in the matrix and a suitable functionality has been implemented in the design.

It should also be noticed, that the ToA is always measured with respect to the falling

edge of the *ACTIVE* time (end of integration phase), so to get the full ToA information, the accurate knowledge of the end of the *ACTIVE* time is also needed. For that reason *ACTIVE* signal is synchronized with the external clock, and the time corresponding to the rising and falling edges of *ACTIVE* signal is stored in the global time domain (in the units of external clock cycles). It is done by a dedicated periphery circuit, because these values are the same for the whole matrix, as described in the following section.

### 5.3 Readout control and periphery circuitry

Contrary to the previous design, the CLIPS detector operates in a snapshot mode, which is driven by the application specification. According to the experiment requirements, the device has to be sensitive only for 160 ns after which there is about 20 ms for the readout. Therefore the large dead time of this operation mode is not an issue.

The periphery circuitry, which supports the matrix operation is schematically presented on the block diagram in Fig. 5.10. There are several digital control blocks (marked with green background), providing steering signals for the proper pixel operation and controlling the signal flow. Beside that, there are few analog blocks (yellow background), such as buffers driving analog signals out of the chip and biasing circuitry assuring proper voltages and currents.

For the periphery circuitry only a basic concept, essential to understand the general chip operation, is presented, since the author of this thesis was not the main designer of the digital part.

The matrix operation is triggered by the *Reset Control* block that generates the *INIT* signal (start of new frame acquisition) after receiving the positive feedback information from the *Readout Control* block (*READ\_DONE*) or after receiving the external reset pulse (*EXTERNAL\_RST*). The *INIT* signal is passed to the *Time Control* and *Matrix Control* blocks. The latter is responsible for providing all steering signals necessary to set up pixels in the matrix. It ensures the proper timing for resetting the pre-amplifier and discriminator, as well as controls the baseline and threshold adjustment. After the matrix is set up it sends the *ACTIVE* signal to the *Time Control* circuitry. This block has two main purposes. First of all, it controls the global time counter and stores the *ToA\_REFERENCE* time (the coarse timing information assigned to the whole frame). Secondly, it synchronizes the internal *ACTIVE* signal with the global time domain, which is essential to refer the fine in-pixel timing to the global frame time. The synchronized *ACTIVE* signal is next sent to the matrix which becomes sensitive for its duration. After that the *Readout Control* block takes over and starts to process the time and amplitude informations from each pixel towards the output pads. For that purpose, in the first step the output signals from all pixels in a given row are passed to the *Column Buffers*. After that, the initially buffered signals are serialized and one by one sent out of the chip. There are separate output buffers for the time and amplitude informations thus both analog signals are sent out in parallel. After 64 cycles, when the whole row is processed, the next one is being connected to the column buffers and the procedure repeats until the last row. Once the whole matrix is read out the *Readout Control* sends the *READ\_DONE* information and the acquisition of the next frame may start.

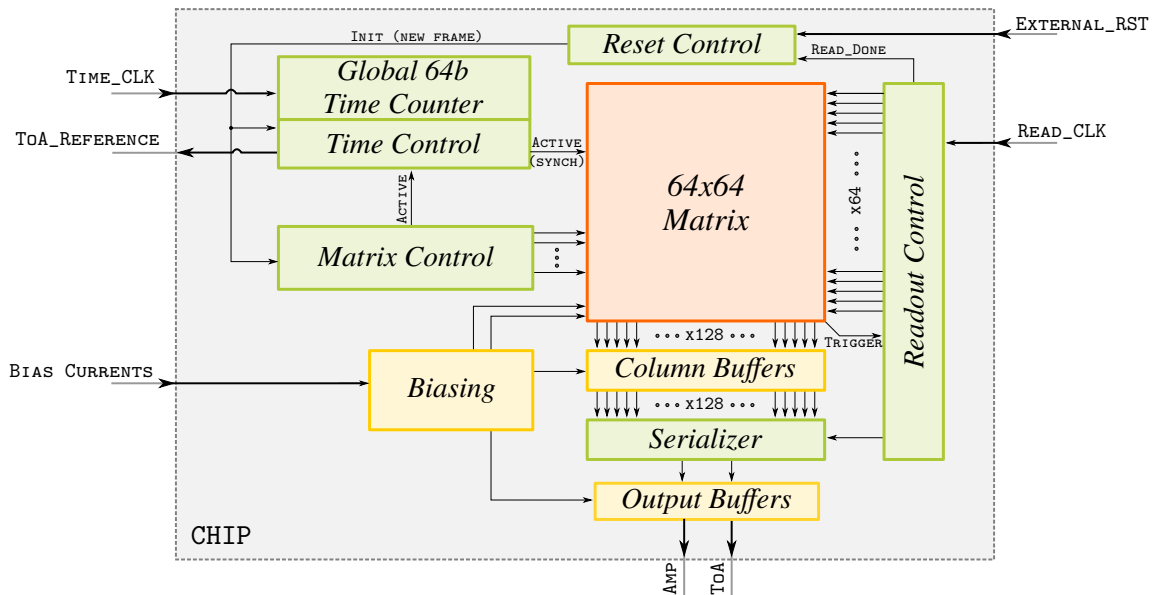


FIGURE 5.10: Block diagram showing periphery circuitry of CLIPS electronics. Analog blocks are filled with yellow color, whereas digital with green.

To increase the testability of the designed detector an additional *TRIGGER* signal is sent out from the matrix. It indicates whether a hit was detected during the *ACTIVE* time window. Therefore the *Readout Control* block may decide to not read the “empty” frame and instead start the next acquisition immediately. This should be highly beneficial in terms of the number of recorded events per measurement time, since the time needed to read out the whole frame (around  $120\ \mu\text{s}$ ) will be usually much longer than the *ACTIVE* time.

As already mentioned, all three matrices included in the design are fully independent, which means that each of them has a separate set of peripheral circuitry. This allows for simultaneous tests of all three matrices, as long as the readout board is able to cope with them simultaneously.

## 5.4 Matrix variants

Contrary to the first design, the differences between matrices are not connected with different readout electronics architectures, but rather with variations in the technical realization of certain components. They concern either the sensing diode design or the feedback capacitance implementation, which are the most sensitive parts of the design and determine the final performance. Overall, four different approaches were implemented. According to Fig. 5.1, Matrix A and B consist of exactly the same readout electronics, with the default feedback capacitance implementation, whereas matrix C was splitted into two halves, with non-standard feedback realisation.

### 5.4.1 Sensor design

The basic sensing node design, used in Matrix A, is presented in Fig. 5.11A. It consists of an octagonal *BPW* layer, formed on the base of  $8\ \mu\text{m} \times 8\ \mu\text{m}$  square, and small highly doped *p+*

region for the interconnection ohmic contact. The  $p+$  implantation and the connection via are slightly off-centered due to the difficulties with fitting all the circuitry into the  $20\ \mu\text{m} \times 20\ \mu\text{m}$  square. However, since it is entirely encircled by the well centered  $BWP$  layer it should not introduce any major asymmetry in the electric field.

For Matrices B and C the sensor design is slightly different (Fig. 5.11B). Beside the sensing diode (which is exactly the same as in the basic design) there is a  $BNW$  ring around each pixel. It has been advised by other users of this technology that with such small pixel pitch there may be a problem with pixel separation on the sensor level. Thus to investigate if the issue really exists and to ensure the proper operation of at least two matrices they have been equipped with this separation ring.

Regarding the sensor design, it should be pointed out that the presented schemes are valid for the  $n$  type substrate, whereas for the  $p$  type substrates the implantations are reversed. In other words, the  $BPW$  layer always represents the implantation opposite to the substrate type, whereas the  $BNW$  layer represents the implantation of the same type as the substrate.

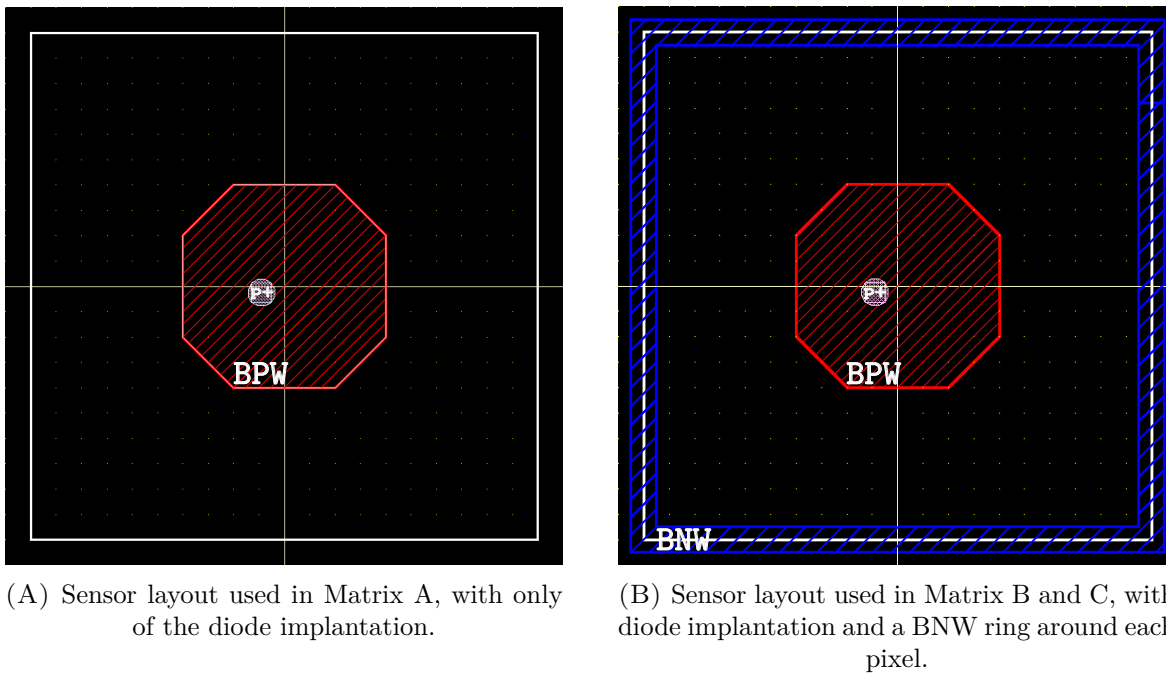


FIGURE 5.11: CLIPS sensor layouts.

#### 5.4.2 Feedback circuitry

To achieve high sensitivity for input charges far below 1 fC, a high charge to voltage conversion ratio in the input stage is essential. Therefore, a further reduction of the feedback capacitance, comparing to the previous design, was needed. Unfortunately, it was not possible with previously used “T-shape” capacitor structure, especially with significantly decreased pixel area.

To obtain an effective capacitance of about 1 fF the “T-shape” structure was still exploited, but the MIM capacitances (which minimum available value of 37.5 fF was the limiting factor) have been replaced by transistors, as presented in Fig. 5.12. This solution has two main



advantages. First of all, the gate capacitance of a smallest available transistor is much lower than the smallest MIM-cap, but also it is much less area consuming, which are both very desired for the presented design. The capacitance of the transistor is mainly determined by the coupling between its gate and channel, which means that its value highly depends on gate-source voltage. Therefore to effectively use a transistor as a capacitance one has to ensure its proper operating point, where the channel is well established. Fortunately the voltage levels on “A” and “B” terminals are limited by the input stage design, and they should not drop below 0.6 V. Thus, one has only ensure the ground potential on the internal node of the “T-shape” structure to get  $V_{GS} \geq 0.6$  V, which is above the transistor threshold voltage. It was realised by an additional transistor in the diode-like connection to the ground.

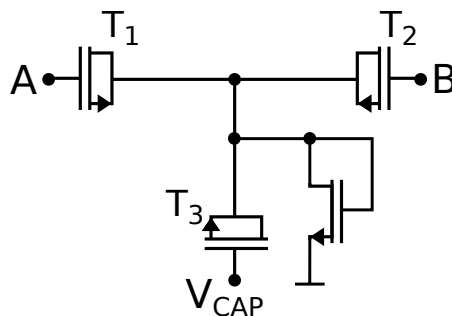


FIGURE 5.12: Scheme of the transistor-based “T-shape” capacitor structure.

Moreover, according to Fig.5.12, the gate of the  $T_3$  transistor has been connected to an external voltage source ( $V_{CAP}$ ). Since the total capacitance of transistor depends on the voltage across gate and source, the total feedback capacitance can be tuned by changing  $V_{CAP}$  potential. In the submitted chip, the  $T_1$  and  $T_2$  were of the same size and had  $C_{GTOTAL}^{T1} = C_{GTOTAL}^{T2} \simeq 6$  fF, whereas  $C_{GTOTAL}^{T3}$  can vary between 15 fF and 55 fF for different  $V_{CAP}$  voltages. According to equation 4.6 (on page 56) this leads to effective feedback capacitance between 0.5 fF and 1.5 fF. The T-shape approach has been assumed as a basic solution and implemented in Matrices A and B.

Since the parasitic capacitance can play a dominant role, even with the layout optimized very carefully, two different solutions have been applied in Matrix C design. Its bottom half was equipped with a custom capacitance, formed by the interconnection metallization layer and appropriate path guidance. According to the technology specification its capacitance should correspond to 1 fF. In case of the second half of Matrix C, the intended feedback capacitance has been totally removed, so it will be fully determined by the parasitic couplings.

The main issue with these two solutions could be a high pixel-to-pixel capacitance variation, which will cause the dispersion of the pixels conversion ratios. It is highly undesired effect, but since the matrix provide the precise charge measurement it allows for pixel-level calibration. Thus, the negative influence of the discrepancies between pixel may significantly alleviated.

## 5.5 Current status and future intentions

First prototypes of CLIPS detector have been already fabricated. The photography of received chips is presented in Fig. 5.13, where the basic building blocks (introduced in Fig. 5.1A) can be easily distinguished with the bare eye. In the near future a detailed characterization of this chip is foreseen. It is planned to perform similar measurements as for the first detector prototype. These are the studies with the radioactive sources, aimed to calibrate the device and estimate the ENC, as well as the beam tests dedicated to the spatial and timing resolution evaluation.

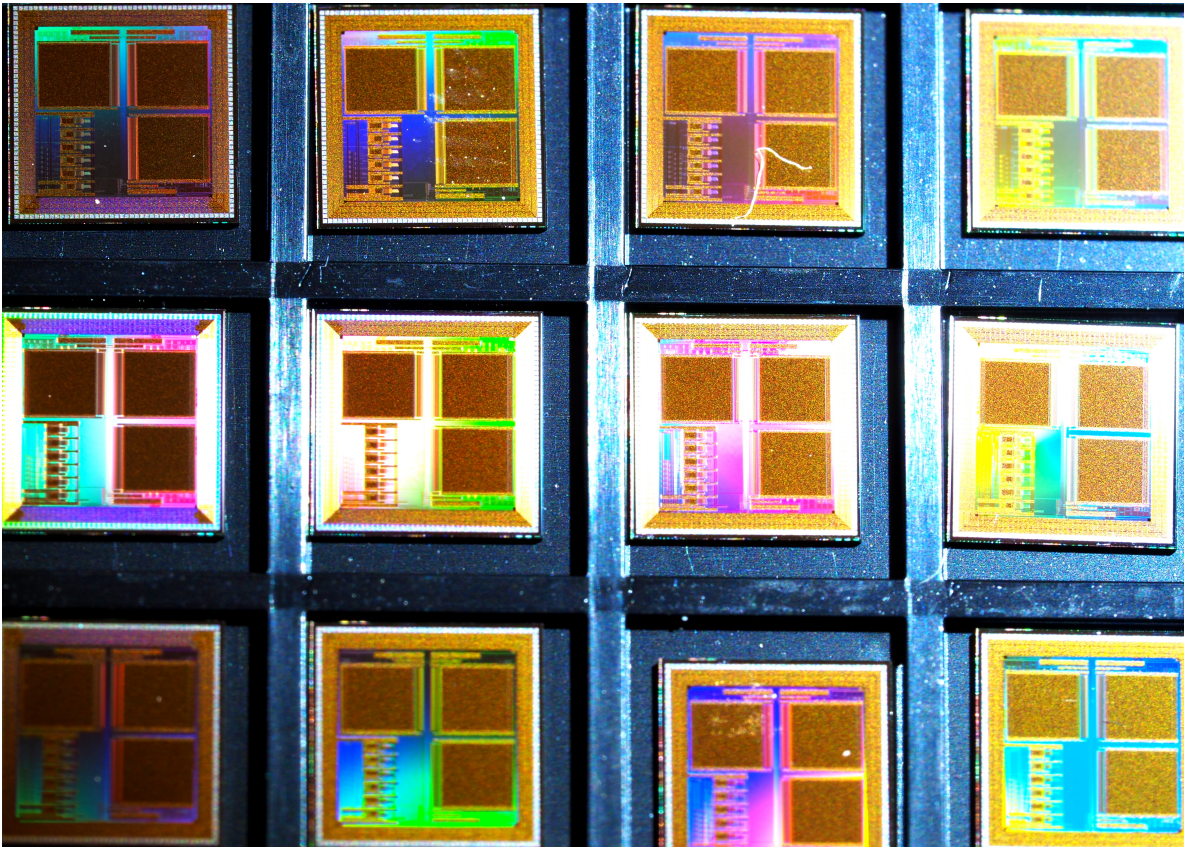


FIGURE 5.13: Photography of fabricated CLIPS prototypes.

However, before starting the measurements a completely new readout system has to be developed. There are major differences between the first detector prototype and the CLIPS detector, so it is not possible to reuse the previous setup. Thus, currently a dedicated PCB is being designed and its integration with the modular test system for the silicon sensor R&D (CARIBOU – Control and Readout Itk BOard [43]) is foreseen. Depending on the measurement results the decision about the future development will be taken.

# Conclusions

The goal of this thesis was the research and development on monolithic pixel detectors fabricated in the Lapis 200 nm SOI CMOS technology. The work was devoted to verify its capabilities in terms of the usage for ionizing radiation detection, mainly for the future high energy physics experiments. For that purpose author of the thesis designed several monolithic pixel detector prototypes, prepared appropriate measurement setups, developed the data acquisition system, performed different kinds of measurements and analysed the obtained results to characterize the prototype devices.

Thanks to the close collaboration with the Japanese group working on the same technology, author of this thesis was able to measure several prototypes of large area integrating type monolithic pixel detector INTPIX6 developed at KEK. The tested prototypes have shown a very good energy resolution, with the ENC calculated from the pixel noise of about  $70 e^-$ . One prototype has been irradiated up to 60 krad, but its good performance was maintained only up to 25 krad, what has revealed the SOI main weakness, which definitely is a poor radiation hardness. Beside that, that detector showed good imaging capabilities sharply reproducing  $100 \mu\text{m}$  large details even after irradiation. To study the INTPIX6 detector performance author of presented thesis had to prepare the measurement stand, perform numerous measurements using different signal sources and different detector assemblies, as well as prepare a dedicated data analysis software allowing to extract the detector parameters.

After obtaining promising results with the INTPIX6 detector, author of the thesis was highly involved in the design of several SOI monolithic pixel detectors prototypes, of which the two most important are presented in this work. First of them was a general purpose detector comprising different readout approaches. For this prototype the obtained ENC values were around  $100 e^-$  and  $110 e^-$  for the best configurations on the FZ(n) and the DSOI(p) wafers respectively. Thanks to the implementation of different readout architectures and different sensor geometries, a high coupling between the electronics and sensor was found and its origin was well understood. This was a very important outcome in terms of the next devices design. In addition to the lab-measurements, this prototype pixel detector was also studied during several test-beams. The best performing configuration showed an excellent spatial resolution of  $2.1 \mu\text{m}$  for  $30 \mu\text{m} \times 30 \mu\text{m}$  pixels.

During the design of this prototype, author of this thesis was mainly responsible for the charge pre-amplifier pixels matrix and the periphery analog parts. Beside the design, author has also prepared the dedicated data acquisition software allowing for the communication with the readout board, performed the measurements and developed the data analysis software. Author also took part in many test-beam campaigns, during which he was responsible for the integration of the DAQ system with the external infrastructure and the data acquisition.

The last part of the PhD studies was devoted to the design of much more complex detector, named CLIPS, aiming for the demanding requirements of the CLIC vertex detector. It requires  $\sim 150\ \mu\text{m}$  thick device with very high granularity, to provide position measurement with the accuracy below  $3\ \mu\text{m}$  and 10 ns time-stamping. To meet these demands, several non-standard solutions were introduced in the CLIPS detector design (such as analog ToA measurement). Finally, an appropriate performance was achieved on the simulation level and the chip was sent for fabrication. The next step will be the verification of its performance by the measurements of already fabricated prototypes, which is foreseen after the PhD. During the design of CLIPS detector author of this thesis has prepared pixel matrices of three different types, analog parts of the readout chain (such as buffers, analog multiplexers/serializers), as well as composed all the individual functional blocks into the final detector structure.

To sum up, during the PhD studies:

- INTPIX6 detector was characterized, its radiation hardness and imaging capabilities were checked,
- general purpose, monolithic SOI pixel detector was designed and its noise performance was estimated during the lab-measurements, whereas its spatial resolution was verified during the test-beams,
- CLIPS detector was designed and its behaviour was checked on the simulation level.

Thus, the main goal of this thesis, namely the research and development on the capabilities of the Lapis SOI technology in terms of its usage for the design of monolithic pixel detectors, was fully achieved.

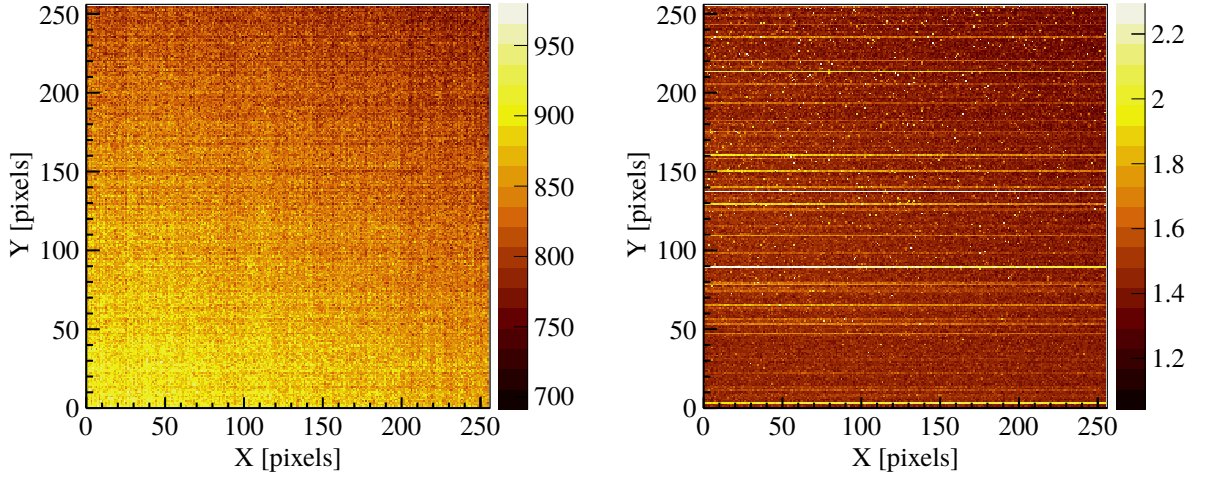
All the performed measurements allowed to broaden the knowledge about the Lapis 200 nm SOI CMOS technology, especially in terms of monolithic pixel detectors design. It has been proven that this process allows for fabrication of fully functional devices overcoming the limitations of hybrid detectors (for instance allowing the fine segmentation or detector capacitance reduction). The in-depth analysis of obtained results provide important guidelines for the future designs and reveals the areas of research that should be further studied (e.g. radiation hardness).

Besides all the content presented in this thesis, its author was also involved in different projects. For example, he took part in the development of the SALT (Silicon ASIC for LHCb tracking) readout chip for LHCb upgrade, for which he designed the biasing DACs. He also took part in several internships at CERN and KEK, which allowed for strengthen the cooperation with the leading research centers. The significance of the performed studies can be confirmed by the numerous presentations on international conferences and several publications in peer-reviewed journals.

## Appendix A

# Additional plots for INTPIX6 FZ(n) detector

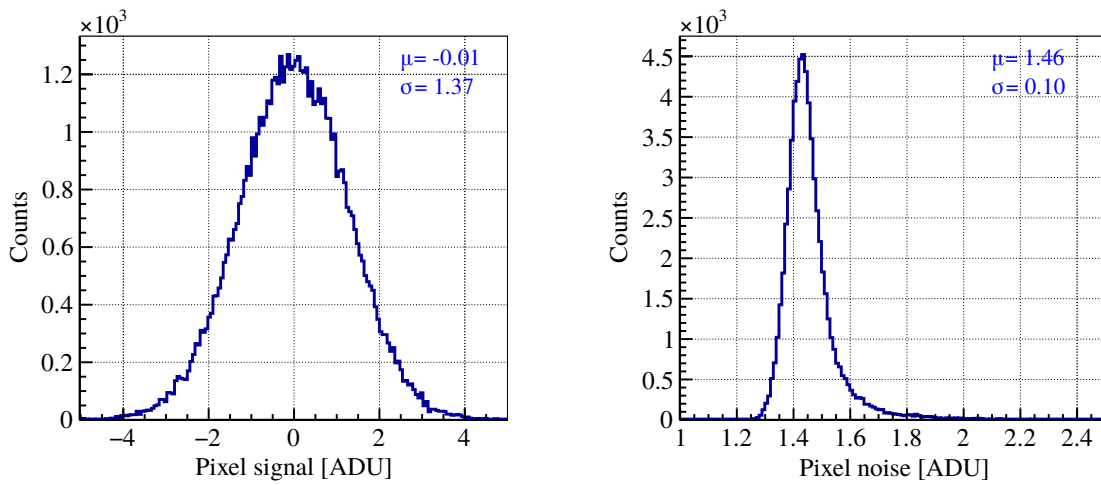
Additional plots showing the basic behaviour of the INTPIX6 detector fabricated on the FZ(n).



(A) Pedestal map  $P[i][j]$ .

(B) Noise map  $\sigma[i][j]$ .

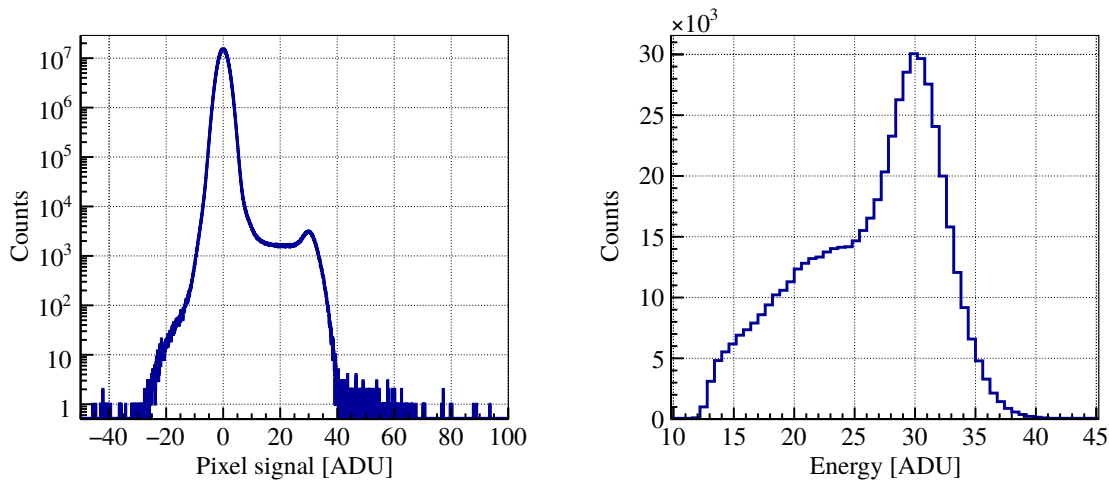
FIGURE A.1: Exemplary plots showing the pedestal and noise distribution over the matrix given in ADC counts [ADU]. Obtained with the INTPIX6 detector fabricated on FZ(n) wafer.



(A) Spectrum of the pixel signal  $S[i][j]$ , combined for all pixels in the matrix.

(B) Spectrum of the pixel noise  $\sigma[i][j]$ .

FIGURE A.2: Exemplary plots showing spectra of the pixel signal and the pixel noise for the “calibration” data sample. Obtained with the INTPIX6 detector fabricated on FZ(n) wafer.



(A) Spectrum of the pixel signal (before clusterization).

(B) Spectrum of the cluster energy.

FIGURE A.3: Exemplary plots showing the spectra of pixel signal and cluster energy. Obtained with the INTPIX6 detector fabricated on FZ(n) wafer using  $^{55}\text{Fe}$  radiation source.

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