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CMOS Technologies in Detector Readout Systems of Modern Particle Physics Experiments

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Aware of legal responsibility for making untrue statements I hereby declare that I have written this dissertation myself and all the contents of the dissertation have been obtained by legal means.

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Abstract

In the times of constantly expanding knowledge of particle physics and the improvement of the large accelerators, increases the luminosity of experiments. Consequently, it requires better detectors and more precise and faster readout systems. Mostly every system contains the Application Specific Integrated Circuits (ASIC) that allow to preprocess particles' signals from specific detector.

The main focus in this research is on the readout system for straw tube tracker detectors, done with collaboration between groups of the Jagiellonian University and AGH University. The detectors are used in two experiments, in future $\overline{\mathrm{P}}\mathrm{ANDA}$ (Straw Tube Tracker (STT) and Forward Tracker (FT)) and in upgraded HADES (Straw Tracking Stations (STS)), both at the FAIR facility in Darmstadt. The readout is based on the PASTTREC ASIC developed by the AGH University group. Since more than 5000 chips are used in both experiments, the main goal was to prepare the measurement setup for mass tests and qualification procedures. Everything was verified by measurements with the straw tube module and ^{55}Fe source. As a part of this work, also the optimisation of the Front-End Boards (FEBs) containing PASTTRECs was done and one week internship in HADES during beamtime.

The second part of the research concentrates on the development of ASICs for future experiments. In modern systems, not only the information about the signal's amplitude is needed, but also the measurement of time starts to be required. Therefore, the main focus was on developing a Time-to-Digital Converter (TDC) using 130 nm CMOS technology based on 10-bit SAR ADC (Successive Approximation Register Analog-to-Digital Converter) [1, 2]. The 8-channel prototype TDC was designed that allows time measurements with configurable resolution from 10 to 100 ps. The aforementioned 10-bit SAR ADC was also part of HGCROC ASIC for HGCAL in CMS experiment designed by OMEGA group from Ecole Polytechnique in collaboration with the CEA-IRFU Institute in Saclay, CNRS from Paris, CERN and AGH UST. The AGH University group was responsible for ADC design, whose measurements and settings optimisation were part of this thesis.

Streszczenie

W czasach stale rozwijającej się wiedzy z zakresu fizyki cząstek elementarnych oraz udoskonalania wielkich akceleratorów, wzrasta świetlność eksperymentów. W związku z tym zwiększa się zapotrzebowanie na coraz lepsze detektory oraz bardziej precyzyjne i szybkie systemy odczytu. Przeważnie każdy system zawiera dedykowane układy scalone (ang. Application Specific Integrated Circuits (ASIC)), które umożliwiają wstępne przetwarzanie sygnałów cząstek z określonego detektora.

Główną częścią tej pracy jest system odczytowy dla śladowych detektorów słomkowych, realizowany we współpracy z zespołem z Uniwersytetu Jagiellońskiego. Detektory te są używane w dwóch eksperymentach, w przyszłym eksperymencie $\overline{\mathrm{P}}\mathrm{ANDA}$ (w Straw Tube Tracker (STT) i Forward Tracker (FT)) oraz w zmodernizowanym eksperymencie HADES (Straw Tracking Stations (STS)), oba w ośrodku FAIR w Darmstadt. Ich odczyt bazuje na układzie PASTTREC zaprojektowanym przez grupę z AGH. W związku z wykorzystaniem ponad 5000 chipów w obu eksperymentach, głównym celem było przygotowanie układu pomiarowego do testów masowych i procedur kwalifikacyjnych chipów. Wszystko zweryfikowano pomiarami z modułem detektora słomkowego i źródłem żelaza ^{55}Fe. W ramach tej pracy wykonano również optymalizację płytki drukowanej (Front-End Board (FEB)) zawierającej chipy PASTTREC oraz odbyto tygodniowy staż w eksperymencie HADES podczas pomiarów na wiązce.

Druga część badań koncentruje się na rozwoju układów ASIC do przyszłych eksperymentów. W współczesnych eksperymentach istotna staje się nie tylko informacja o amplitudzie sygnału, ale również pomiar czasu. W związku z tym główny nacisk położono na opracowanie układu do pomiaru czasu (konwerter czasowo-cyfrowy TDC, ang. Time-to-Digital Converter) z wykorzystaniem technologii CMOS 130 nm w oparciu o 10-bitowy przetwornik anologowo-cyfrowy SAR ADC (ang. Successive Approximation Register Analog-to-Digital Converter). Zaprojektowano 8-kanałowy prototyp TDC, który umożliwia pomiar czasu z konfigurowalną rozdzielczością od 10 do 100 ps. Wspomniany 10-bitowy przetwornik SAR ADC jest również częścią układu HGCROC dla HGCAL w eksperymencie CMS, CERN zaprojektowanym przez grupę OMEGA z Ecole Polytechnique we współpracy z Instytutem CEA-IRFU w Saclay, CNRS z Paryża, CERN i AGH. Grupa z AGH była odpowiedzialna za układ ADC, którego pomiary i optymalizacja ustawień była częścią tej pracy.

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Acronyms

$\overline{\text{P}}$ANDA antiProton ANihilation at DArmstadt. xiii, 1, 2, 4–6, 8–14, 17, 18, 30, 43, 44, 89, 91

ADC Analog-to-Digital Converter. xvii, 1, 2, 14, 61–63, 65–74, 77, 79, 82–85, 90, 91

AGH University Akademia Górniczo-Hutnicza University of Krakow. 2, 8, 11, 19, 61, 62, 82, 90, 91

ASIC Application-Specific Integrated Circuit. xiii–xv, xvii, xix, 1, 2, 8, 11, 12, 14, 15, 17–19, 21, 25, 28–33, 36–39, 41, 42, 61, 63, 75, 77, 79, 80, 82, 89–91

BGA Ball Grid Array. 83

CBM Compressed Baryonic Matter. 5

CERN European Organization for Nuclear Research. 2, 5, 61, 82, 91

CIB Charge Injection Board. xiv, 23, 24

CMOS Complementary Metal–Oxide–Semiconductor. 1, 14, 15, 61, 62, 71, 89

CMS Compact Muon Solenoid. xiii, 1, 2, 5, 6, 61, 89, 91

CP Charge Pump. xvii, 63–68, 70, 73, 77

CVD Chemical Vapour Deposition. 7, 10

DAC Digital-to-Analog Converter. xiv, xvii, xviii, 18, 19, 25–27, 30, 32, 33, 35, 38, 45, 62, 64, 67, 69, 79, 83–86

DAQ Data Acquisition. 2, 54, 60

DIRC Detection of Internally Reflected Cherenkov light. 10

DNL Differential Non-Linearity. xiv, xvii, xviii, 25, 26, 62, 69, 72, 73, 75, 83–87, 90, 91

DSP Digital Signal Processing. 14

ECAL Electromagnetic Calorimeter. 8

EMC Electromagnetic Calorimeter. 5, 6, 10

ENC Equivalent Noise Charge. xiv, 28, 30

ENOB Effective Number of Bits. 62, 69

FAIR Facility for Antiproton and Ion Research. xiii, 2, 5, 6, 8, 9

FEB Front-End Board. xiii–xv, 1, 2, 12, 17–27, 29–31, 33, 35, 40, 43, 57, 89, 91

FPGA Field-Programmable Gate Array. 12, 14, 19, 80, 81, 83

FRPC Forward Resistive Plate Chamber. 8

FS Forward Spectrometer. 9, 10

FT Forward Tracker. xiii, 6, 10–13, 18, 20, 23, 43

GEM Gas Electron Multiplier. 10

GSI Gesellschaft für Schwerionenforschung. 5, 6, 17, 54

HADES High Acceptance DiElectron Spectrometer. xiii, xvi, 1, 2, 5–8, 11, 13, 14, 17, 18, 21, 43, 44, 54, 55, 58, 59, 89–91

HC Hadron Calorimeter. 5, 6

HESR High Energy Storage Ring. 8–10

HGCAL High Granularity Calorimeter. 1, 2, 61, 91

HGCROC High Granularity Calorimeter Read-Out Circuit. xvii, xviii, 1, 2, 61, 77, 82–87, 89, 91

HL High Luminosity. 61

HV High Voltage. xvi, 11, 25, 46, 50–52, 54, 55, 90

HV-MAPS High Voltage Monolithic Active Pixel Sensors. 10

INL Integral Non-Linearity. xvii, xviii, 62, 69, 72, 74–76, 78–80, 83–87, 90, 91

LDO Low Dropout. 18, 20, 21

LED Leading Edge Discriminator. 18

LHC Large Hadron Collider. 4–6, 61

LSB Least Significant Bit. 69

LVDS Low-Voltage Differential Signalling. 18, 19

MDC Mini (cell) Drift Chambers. 7, 19

MIM Metal-Insulator-Metal. 69

MIP Minimum-Ionising Particle. 43, 82

MSB Most Significant Bit. 63, 69, 77, 90

MVD Micro Vertex Detector. 10

OTA Operational Transconductance Amplifier. xvii, 67, 68, 73

PASTTREC **PA**NDA **STT** **RE**adout **C**hip. xiii, xiv, xix, 2, 8, 11, 12, 14, 17–20, 23, 25, 27, 28, 30–33, 36, 38, 55, 58, 89

PFD Phase Frequency Detector. xvii, 63–69, 73

PZC Pole Zero Cancellation. 18

QA Quality Assurance. 58

QCD Quantum Chromodynamics. 4, 6, 8

R&D Research and Development. 63

RHIC Relativistic Heavy Ion Collider. 5, 6

RICH Ring-Imaging Cherenkov. 7, 8, 10

RPC Resistive Plate Chamber. 7

SAR Successive Approximation Register. xvii, xix, 2, 61–63, 66, 68–70, 77, 82, 83, 90, 91

SINAD Signal-to-Noise and Distortion Ratio. 62, 69

STS Straw Tracking Stations. xvi, 6, 8, 11, 13, 17, 18, 20, 21, 23, 43, 54–60, 90

STT Straw Tube Tracker. xiii, 6, 10, 11, 18, 20

TAC Time-to-Analog Converter. xvii, 61–64, 66, 68–71, 73, 79, 90, 91

TC Tail Cancellation. 14, 18

TDC Time-to-Digital Converter. xvii, 1, 2, 12, 14, 19, 38, 61–64, 69–75, 77–82, 89–91

TOA Time-Of-Arrival. 11, 14, 17, 19, 52, 82

TOF Time of Flight. 7, 8, 10

TOT Time-Over-Threshold. xiv, xvi, xix, 11, 17, 19, 25, 26, 29, 44, 45, 47, 50, 51, 53, 58–60, 82, 90

TRB Trigger Readout Board. 12, 14, 19

TS Target Spectrometer. 9, 10

TWEPP Topical Workshop on Electronics for Particle Physics. 17, 89

VCM Voltage Common Mode. xvii, 63, 67, 68, 73

Introduction

The question of how the matter around us is built has always been asked by people since ancient times. Along with the development of technology, knowledge of matter was also expanded, creating the field of particle physics. Through the years, people have discovered smaller and smaller particles that build surrounding matter. To observe the new particles that were expected by theory, high-energy physics experiments with large accelerators had to be constructed. The particle beams are speeded up in the accelerator and then hit with each other or the target at very high energies. The particles created in this collision have to be detected in large detector systems, which allow one to measure particle's momentum and energy. One of the most important parts of detector is the readout electronics system that reads signal from detector and converts it to data that can be then analysed. Modern experiments have a large number of channels, placed very densely, but modern technologies allow reducing the size of circuits and reducing power consumption. Furthermore, the detector and readout electronics have to work under high radiation conditions. These factors cause almost every detector to need its own dedicated Application-Specific Integrated Circuit (ASIC).

The aim of this thesis was the development of detector readout systems for particle physics experiments such as anti**P**roton **AN**ihilation at **DA**rmstadt ($\overline{\mathrm{P}}$ANDA), High Acceptance DiElectron Spectrometer (HADES) and Compact Muon Solenoid (CMS). The main purpose was to optimise the front-end electronics of the straw tube detectors for experiments HADES and $\overline{\mathrm{P}}$ANDA, to prepare the setup for mass tests of their Front-End Boards (FEBs) and to analyse the data from the first bench of boards. The next objective of the thesis was the development of dedicated ASICs for future experiments. Modern experiments require more often time measurement (for example, for the measurement of arrival time of particle). Therefore, the aim was to design the Time-to-Digital Converter (TDC) circuit with 10 to 100 ps time resolution which could be the part of ASIC for future experiments. The last goal was the Analog-to-Digital Converter (ADC) optimisation for High Granularity Calorimeter Read-Out Circuit (HGCROC) ASIC for High Granularity Calorimeter (HGCAL) detector in CMS experiment.

This work allowed the author to be involved in every part of the process of creating the readout system, starting from designing the electronics circuit in submicron Complementary Metal–Oxide–Semiconductor (CMOS) technology, through prototype tests, preparation of the test setup, final tests with detector and qualification measurements of ASICs, and finally participation in experiment monitoring during beamtime.

This thesis consists of an introduction, three chapters describing the 4-year work, and a summary. The first chapter describes the basics of particle physics and introduces the subject of particle

physics experiments. The overview of typical experiment is presented based on CMS experiment. In the second part of the chapter, two experiments important for this work, HADES and future $\overline{\mathrm{P}}\mathrm{ANDA}$, are presented. Both are located at the Facility for Antiproton and Ion Research (FAIR) facility in Darmstadt, Germany. Particular attention is given to the straw tube tracking detectors used in the aforementioned experiments, $\overline{\mathrm{P}}\mathrm{ANDA}$ and HADES. The chapter ends with a description of the development of ASICs for modern particle physics experiments.

The second chapter focusses on the readout electronics for the $\overline{\mathrm{P}}\mathrm{ANDA}$ and HADES experiments. This project was carried out in close collaboration between groups from Jagiellonian University and Akademia Górniczo-Hutnicza University of Krakow (AGH University). The Jagiellonian University group is responsible mainly for the straw detector part and the Data Acquisition (DAQ) system, while the AGH University group is in charge of the front-end electronics. At the beginning of the chapter, the readout system is presented, which is based on **PA**NDA **STT RE**adout **C**hip (PASTTREC) ASIC mounted on a dedicated FEBs. First, the optimisation of FEBs was performed. Since more than 5000 chips had to be produced for both experiments, the mass test setup was required. Hence, the next part of the chapter discusses this setup together with measurement procedures and qualification requirements. The main part of the chapter are the results from the above mentioned mass tests and then the results obtained with straw tubes and ^{55}Fe source in the Jagiellonian University laboratory. Finally, the monitoring of the HADES beamtime detector is described due to the completed one-week internship at HADES during beamtime.

The third chapter concentrates on development of dedicated ASICs for future experiments. The main part of this work was the design of Time-to-Digital Converter (TDC). Hence the first part of the third chapter presents the design of TDC, results from simulations and the design of an 8-channel prototype ASIC together with the preparation of the prototype measurement setup. In the second part of this chapter, the ADC measurements of HGCROC ASIC are presented. The HGCROC is a readout ASIC for the HGCAL detector in the CMS experiment, European Organization for Nuclear Research (CERN). The AGH University group contributed to the design of the fast 10-bit Successive Approximation Register (SAR) ADC for the HGCROC readout ASIC.

Chapter 1

Particle physics experiments

1.1 Introduction

People have always wondered how the world around us is built. Philosophers in ancient Greece have already used the term *atom* as something very small from which the matter is built and cannot be divided. Then through the last centuries more discoveries have proven the particle structure of matter: first atom concept of John Dalton (1808), periodic table of Mendeleev (1896), but finally it was proven that atoms are built of smaller parts, like proton, neutron and electron. In 1897, J. J. Thomson, after almost 50 years of research, claimed the presence of negatively charged electrons, and at the turn of the 19th and 20th century the presence of proton in the atomic nucleus was confirmed (Rutherford). In the next years further particles were discovered: positrons, muons, neutrinos, etc. The second part of the 20th century has brought a fast development in technology that also caused a development in particle detection, and hence, widening knowledge in the field of particle physics.

In the 1970s of the 20th century, the term *Standard Model*, similar to what we know now, was introduced to the world of science by Abraham Pais and Sam Treiman. The Standard Model of Particle Physics (Figure 1.1) so far contains 12 particles, fermions, from which matter is made and 13 particles, bosons, that are responsible for transferring interactions between other particles.

The fermions are grouped into 3 generations. Six of them are known as quarks (up u, down d, charm c, strange s, top t and bottom b) and the other six are leptons (electron e, muon μ, tau τ, electron neutrino ν_e, muon neutrino ν_μ and tau neutrino ν_τ). All fermions have spin equal to $\frac{1}{2}$, they differ in mass and charge. Three leptons have negative charge -1, e, μ, τ, and the other three are electrically neutral and very light corresponding neutrinos: ν_e, ν_μ and ν_τ. Additionally, there are 12 antiparticles, respectively, to the mentioned fermions with opposite charge.

Quarks can be seen so far only in hadrons, together with other quarks or gluons. They have the additional property of colour, red, green, or blue, and antiquarks that have respective anticolor, antired, antigreen, or antiblue, which gives the possibility of strong interactions. To form the hadron, they have to have neutral colour, white: colour-anticolour or three different colours/anticolours. The most common hadrons are mesons (pairs of quarks) and barions (triples of quarks). Mesons have spins 0 or 1, so in this understanding they are also bosons, while barions have spins

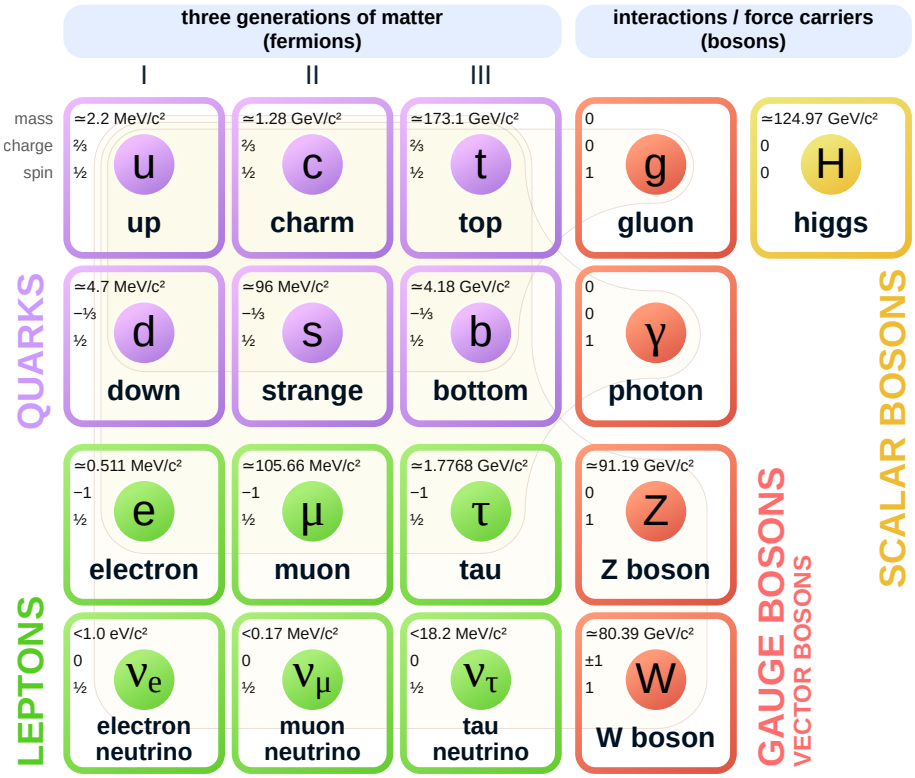


Figure 1.1: Standard Model of Particle Physics [3].

$\pm\frac{1}{2}, \frac{3}{2}, \ldots$, which makes them complex fermions. It is predicted that only 5 of the quarks take part in creating barions, since the t has too fast decay time to last and create any hadron. One of the most common barions are p and n. Now all barions that are formed of only u and d quarks are called nucleons, among others p (uud) and n (udd). All hadrons have their antiparticles, created from respective antiquarks. Hadrons can also be formed in tetraquarks (in 2014, the LHCb experiment observed a Z (4430) 4-quark hadron), glueballs or other exotic hybrids, which will be observed, among others, in future anti**P**roton **AN**ihilation at **DA**rmstadt ($\overline{\mathrm{P}}$ANDA) experiment.

The matter that we see on Earth is built only of the particles from the I fermion generation of the Standard Model. Particles from the II generation, s, μ and ν_μ (except c) come with cosmic radiation with particles such as pions π and kaons K. The rest of the fermions require very high energy to be produced.

The other part of the Standard Model contains bosons. They have an integer value of spin, and they are responsible for the transfer of interactions between other particles. There are: two, W^+, W^-, and one Z^0 boson, which mediate weak interactions, eight gluons that mediate strong interaction between quarks or other gluons, photons γ responsible for electromagnetic interactions and the Higgs boson observed in 2012 that gives masses to particles interacting with the Higgs field.

At the beginning of the universe in the first few millionth parts of the second there was a hot and dense mix of quarks and gluons, which then, after cooling, created protons, neutrons, and other particles. Quantum Chromodynamics (QCD) is a theory that describes the strong interactions of quarks, antiquarks, and gluons that bond them into hadrons. Modern experiments such as Large

Hadron Collider (LHC) or Relativistic Heavy Ion Collider (RHIC) simulate hot and low baryonic density conditions, probably observed in the early universe. On the other hand, in compact stars, a cold and very high internal baryonic density is present. This part will be reconstructed in Compressed Baryonic Matter (CBM), Facility for Antiproton and Ion Research (FAIR) experiment, but also High Acceptance DiElectron Spectrometer (HADES) experiment will produce reference data.

New particles, their complex interactions and internal structures can be studied only with high energies, since not all particles are observed on Earth; some of them were present only in the early universe or now in stars. To broaden our knowledge of particles, particle accelerators are needed, where the particles' beams are speeded up and then hit with each other at very high energies (proton beam collisions of two counterrotating beams with energies 0.9-13 TeV in Compact Muon Solenoid (CMS) at LHC at European Organization for Nuclear Research (CERN)) or with target (proton beam collision with metal (gold) foil with energies up to 4.5 Gev (29 GeV after upgrade) in HADES at Gesellschaft für Schwerionenforschung (GSI) or antiproton beams with metal foil with energies about 3 GeV in $\overline{\mathrm{P}}$ANDA at FAIR).

After collision, very precise detection of created particles is needed to understand their structure and features. A typical detection system contains four main parts: a tracking system, caloriemeters: Electromagnetic Calorimeter (EMC) and Hadron Calorimeter (HC), and muon chambers. Additionally, to obtain the momentum results from trackers, there is also a large magnet (4 T magnetic field by solenoid magnet in CMS) that bends the particles' paths, the more momentum the particle has, the less curved its path is. The example of the detector system (CMS [14]) is presented in Figure 1.2. Since in the CMS two particle beams collide, the detector has the shape of a barrel (the slice is seen in Figure 1.2) with appropriate endcaps to close all the space around the collision point.

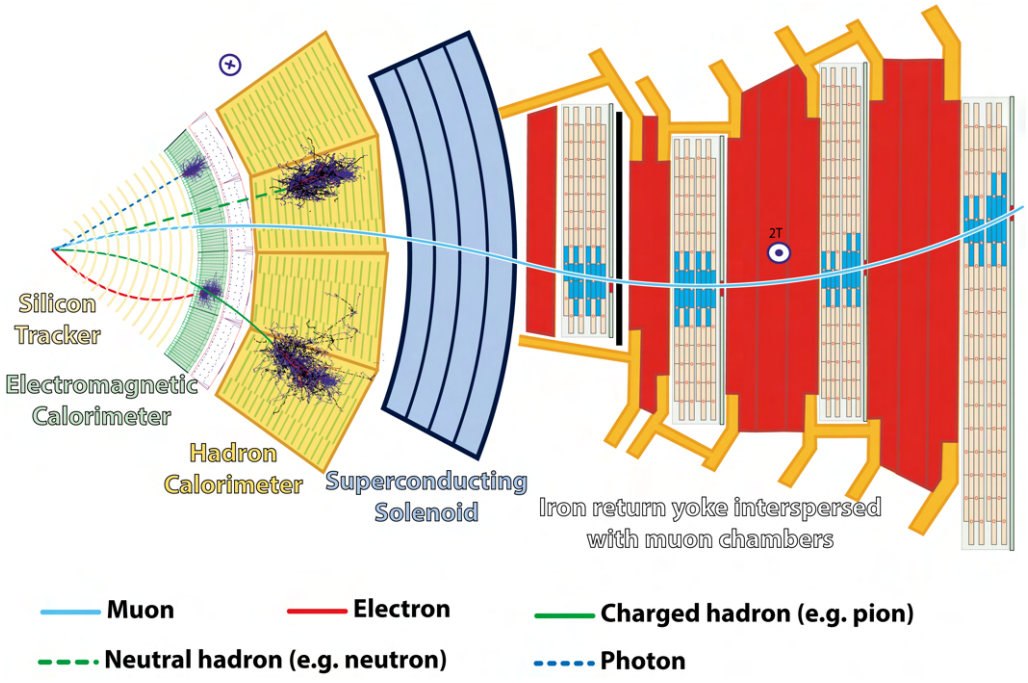


Figure 1.2: CMS detector slice with example particles [4].

Closest to the interaction point, there is a tracking system. To obtain particle's momentum information, a very accurate particle's track in a magnetic field (only charged particles are bent) is provided. Moreover, the trackers must be lightweight, to disturb particle flight as little as possible; therefore, they are usually made of silicon (CMS) or gaseous straw tubes (Straw Tracking Stations (STS) in HADES or Straw Tube Tracker (STT) and Forward Tracker (FT) in $\overline{\mathrm{P}}\mathrm{ANDA}$). Calorimeters are systems that measure the energies of particles; hence, the particles are fully absorbed there. EMC measures the energies of e and γ. In the CMS experiment, lead tungstate ($\mathrm{PbWO_4}$) crystals are used, which are ideal for stopping high-energy particles because they are heavier than steel. The crystals are transparent and scintillate, producing light proportional to the energies passing through e and γ. After EMC, there is HC that measures the energies of hadrons. In CMS alternately layers of brass/steel and plastic scintillators are placed. Brass and steel layers are very dense materials that cause stopping of the particles that then produce signals in plastic scintillators that are read by photodiodes. Muons interact very weakly with matter; therefore, the muon chambers are at the end of the whole detector system interleaved with iron planes. In the CMS experiment, it is one of the most important parts, because it is predicted that muons are a relevant part of new particles' decays, hence in the system there are four stations. There are four types of detector used, all based on different types of gaseous detectors. The multilayer system provides the possibility to measure the trajectory of the particles, and as a result the momentum information is obtained.

1.2 HADES experiment

The High Acceptance DiElectron Spectrometer (HADES) [15] is a magnetic spectrometer at the SIS18 accelerator at the GSI Helmholtz Center for Heavy Ion Reasearch in Darmstadt, Germany, which has been operating since 2002. The SIS accelerator delivers proton beams with energies up to 4.5 GeV that are collided with proton or nuclear fixed targets reaching energies up to few GeV. This results in induced reactions of proton, secondary pions and heavy ions that can be measured on HADES as charged hadrons (proton, pions, and kaons), leptons (electrons and positrons), or photons.

Experiments such as LHC or RHIC provide information only on regions with high temperatures and very small baryon densities; therefore, HADES will provide a complement to these data at lower energies. The main goal of the HADES is to investigate the electromagnetic structure of baryonic resonances and their production mechanisms for energies of several GeV. To explore it, the nucleus-nucleus and $\pi - \mathrm{nucleus}$ reactions are used. The HADES measurements will provide reference data that can be important for upcoming heavy-ion experiments, among others from FAIR, studying the QCD phase diagram in the high baryon density region. Particular attention will be given to the proton-proton reaction from which the hyperons (hadrons with at least one s quark but without c, b, t, existing in stable form within the core of some neutron stars) will be produced. In particular, there is almost no information on the production of multi-strange hyperons with larger masses in the beam energy range provided at the HADES. Higher hyperon resonances can also affect the thermodynamics of QCD or the evolution of the early universe [16]. To achieve these goals, the proton beam energy must be increased to 29 GeV, and the HADES spectrometer

must undergo several hardware changes. The feasibility studies from 2021 [5] show that the upgraded HADES can deliver information about the structure of hyperons and the function of strange quarks in their structure.

The schematic cross-sectional view of the upgraded HADES spectrometer is presented in Figure 1.3. So far the HADES has included the system covering angles $18° - 85°$ around the beam axis in the forward direction. This part of the detection system contains six identical sectors in circular shape together with superconducting coils providing a magnetic field up to 3.6 T placed in the middle of the detection system. The closest to the interaction point is the START-VETO detector to determine the reaction time (part of the Time of Flight (TOF) measurement) and monitor the properties and quality of the beam. The START subdetector is placed 2 cm in front of the target and built of 50 μm thickness Chemical Vapour Deposition (CVD) diamond detectors that provide low noise at high rate with radiation hardness better than silicon. The VETO subdetector is 100 μm thick polycrystalline diamond detector placed about 70 cm behind the target. Next, there is the Ring-Imaging Cherenkov (RICH) detector, position sensitive for e^+/e^- pair identification, and hadrons are not visible by it. It is filled with C_4F_{10} gas which emits Cherenkov light, then it is reflected by carbon fibre mirrors and detected by photocathodes. After RICH, the low mass Mini (cell) Drift Chambers (MDC), multilayer drift chambers are placed. They provide a precise measurement of the spatial position of the hit points and the energy loss. They are built from four tracking planes. Two of them (I, II) are placed before a superconducting toroid, and two after it. Each of the tracking planes contains 6 trapezoidal layers, which gives 24 layers in total. Layers contain cells that are of size 5×5 mm (I layer) to 10×14 mm (IV layer); in total, there are about 27000 cells [17]. To measure the TOF of particles, the TOF detector for outer time measurement and the Resistive Plate Chamber (RPC) detector for inner time measurement are placed behind the MDC. Each sector of the TOF detector contains 8 cases with 8 scintillating bars whose signal is read by photomultipliers to reconstruct TOF with a resolution of 100-150 ps.

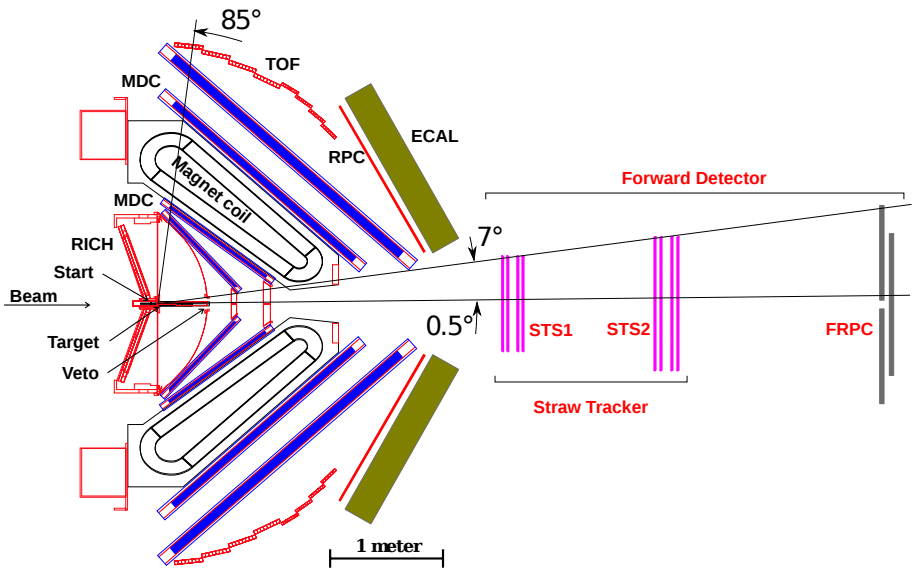


Figure 1.3: Schematic cross-sectional view of the upgraded HADES spectrometer [5].

Recently, in the upgraded version, two changes were implemented in 2019. The first of them was the upgrade of RICH in order to enhance the dilepton identification. Second, the Electromagnetic Calorimeter (ECAL) has been added for the gamma reconstruction that covers $16^\circ - 45^\circ$ around the beam axis. This provides electron-pion separation and studies of neutral meson production. Finally, in 2021, the Forward Detector was added to HADES, which provides the measurements in the forward direction, and adds information about particle tracks and their velocities. It contains two Straw Tracking Stations (STS) - STS1, STS2 and a Forward Resistive Plate Chamber (FRPC) for measurements of TOF. They are located 3.1 m, 4.6 m and 7.5 m from the target, respectively. They provide full azimuthal coverage from the 0.5° to 7° polar angles. The STS is made up of gas straw tube tracking detectors (developed by the Jagiellonian University group) with front-end electronics based on a dedicated **PA**NDA **STT RE**adout **C**hip (PASTTREC) Application-Specific Integrated Circuit (ASIC), which was developed by the Akademia Górniczo-Hutnicza University of Krakow (AGH University) group. The detector system, together with the readout part, was developed preliminary for the $\overline{\mathrm{P}}\mathrm{ANDA}$ experiment and will be described in Section 1.4. The STS was installed in HADES at the end of 2020, it passed first tests in February 2021 with a proton beam up to 4.2 GeV [18] and the first beam measurements with proton beam energies up to 4.5 GeV were made in the first part of 2022.

1.3 PANDA experiment

anti**P**roton **AN**ihilation at **DA**rmstadt ($\overline{\mathrm{P}}\mathrm{ANDA}$) is a future experiment in the FAIR facility in Darmstadt, Germany, which is under construction - Figure 1.4. In $\overline{\mathrm{P}}\mathrm{ANDA}$ experiment, a very high intensity antiproton beam with energies of about 3 GeV will be used. The antiproton beam will be produced by the SIS100 synchrotron, hitting the high-energy proton beam with a metal target. Then the antiproton beam will be accumulated in High Energy Storage Ring (HESR) in two modes: high intensity and high resolution [6]. It leads to even $2 \cdot 10^{32}\mathrm{cm}^{-2}\mathrm{s}^{-1}$ luminosity in high-intensity mode. The high energy range provided in the experiment will allow wide physics studies [19, 20].

One of the main goals of the $\overline{\mathrm{P}}\mathrm{ANDA}$ experiment will be the spectroscopy studies of charmonium and open charm mesons, as well as charmed baryons. Furthermore, there will be the possibility to study gluonic excitations or, generally, more precise experiments within QCD [21]. Anihilation of antiproton-proton instead of collision of proton beams gives a unique opportunity to produce hyperons above 4 GeV energy and will allow their more detailed studies.

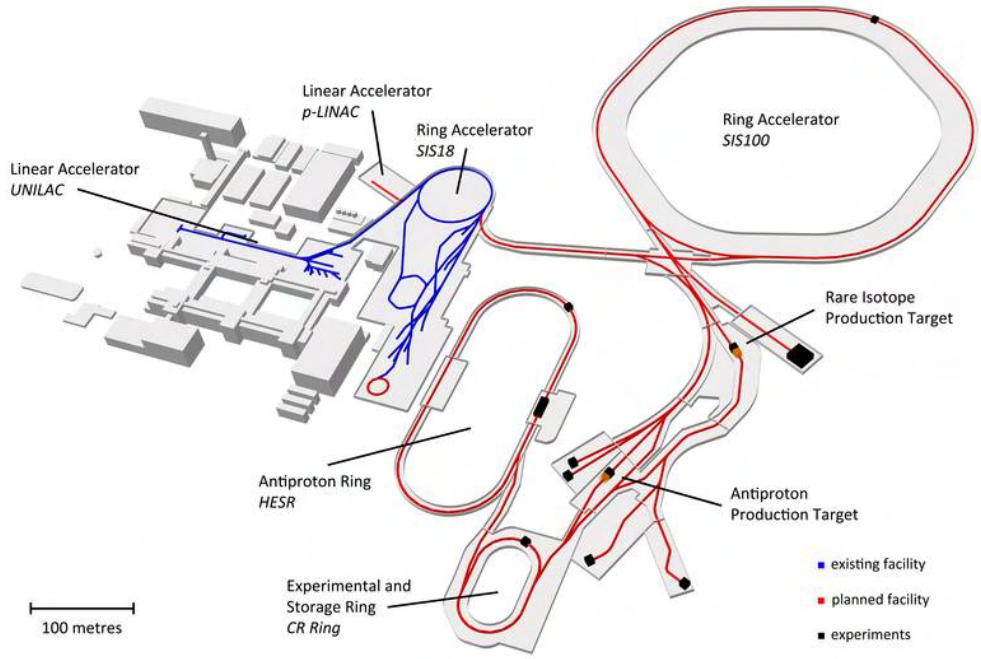


Figure 1.4: Overview of FAIR facility [6].

$\overline{\text{P}}$ANDA experiment will be placed on the straight part of the HESR racetrack shape ring. It will have two main detector systems Target Spectrometer (TS) and Forward Spectrometer (FS) [6] - see Figure 1.5. The first one is a typical collision spectrometer barrel shape with endcaps that will provide 4π coverage around the interaction point. The second part will give information about particles in forward direction behind the collision along the beam line. It will cover angles of $\pm 10^{\circ}$ horizontally and $\pm 5^{\circ}$ vertically. Both parts will provide complete data: tracking, particle identification, calorimetry and muon detection in full momentum range.

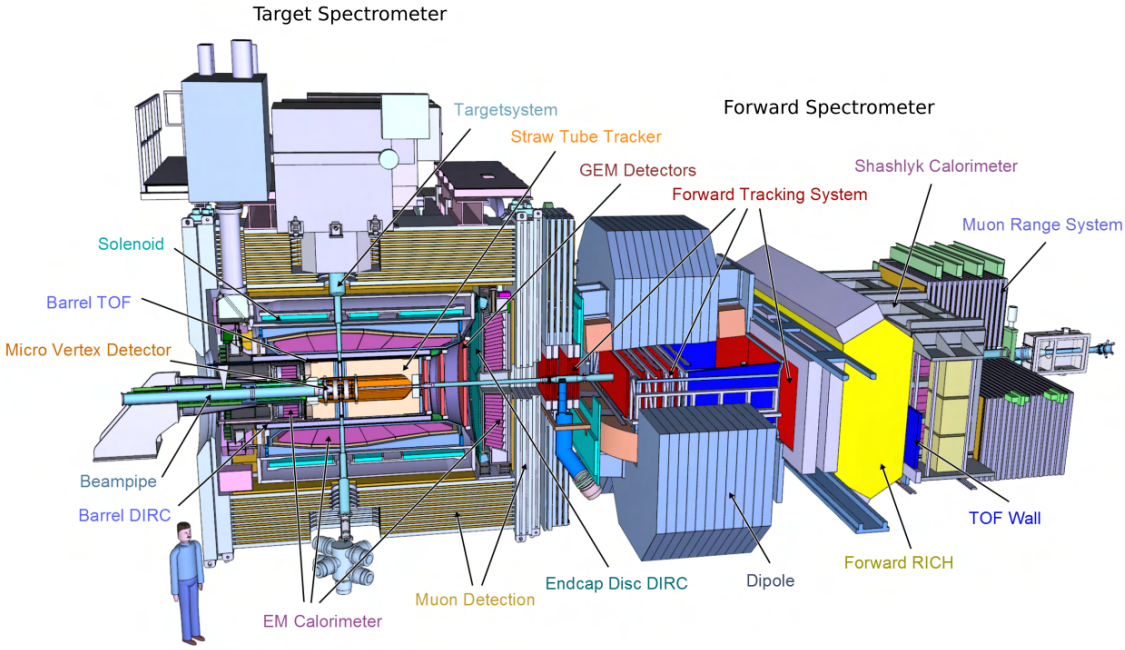


Figure 1.5: Schematic view of $\overline{\text{P}}$ANDA experiment setup at FAIR [7].

The TS will contain three-step charged particle tracking Micro Vertex Detector (MVD), Straw Tube Tracker (STT), and Gas Electron Multiplier (GEM). The first and second will cover the space around the interaction point, and GEM will track the charged particles in the forward direction. The MVD detects short-lived charged particles and provides a high vertex resolution of about 50 μm. It contains four barrel layers and six discs in the forward direction. The first two barrels and all disc (except the last one) layers are pixel detectors, and the rest (2 last barrels and last disc layer) are double-sided silicon strip detectors. The STT is a straw tube gasous detector placed around MVD barrel part. It is described in more detail in the next subsection. The GEM contains 3-circular stations with a diameter of 0.9 m (first) to 1.5 m (last), placed after MVD in the forward direction. The almost 2 T magnetic field in the beam direction surrounding the TS part will be provided by the superconducting solenoid. To identify particles, the Barrel Detection of Internally Reflected Cherenkov light (DIRC) will be located after STT, 450 mm from the interaction point, with angles $22^\circ - 140^\circ$. It will allow to separate charged pions from kaons in momenta in the range from 0.5 to 3.5 Gev/c. The same role in the forward direction will be performed by a 5 cm thick Disc DIRC, located after GEM. Behind Barrel DIRC the time measuring Barrel TOF will be situated. It contains fibre structure photosensors that form a 2.5 m long hodoscope and ensure that the time resolution is less than 60 ps. The calorimetry in TS will be performed using a 3-part EMC spectrometer containing: Barrel, Forward Endcap and Backward Endcap to ensure full coverage. All of them consist of lead tungstate ($\mathrm{PbWO_4}$) crystals providing good resolution for photons up to 15 Gev.

In FS the tracking will be provided by Forward Tracker (FT) which is based on the same straw tubes as in STT and is described in the next subsection. Part of the tracking system will be placed in the dipole magnet which will also be part of the HESR beam line. The identification of particles in the forward direction will be delivered by Forward RICH located behind the FT. It consists of focussing aerogel tiles placed perpendicularly to the beam with segmented mirrors and reflecting Cherenkov light to photosensors located below and above the beam line. The pion-kaon separation will be done in the range of 2-10 Gev/c. Time measurement, with less than 100 ps resolution, will be carried out by Forward TOF constructed of plastic scintillator plates with photomultiplier tubes above and below. The calorimetry in the forward direction will be done with the Forward Shashlyk Calorimeter (behind Forward TOF) containing plastic scintillator tiles placed alternately with 1.5 mm lead absorber plates over the 68 cm length.

Additionally in both parts will be Muon Detectors, that will provide mostly muon detection. Together, they contain 4200 Mini Drift Tubes placed alternately with iron absorbers of 3 cm long in TS (except forward part) and 6 cm long in FS and forward part of TS.

At the end of the FS (behind Muon Chambers), 11 m from the interaction point, the Luminosity Detector will be located, which will deliver information about the relative and absolute luminosity of $\overline{\mathrm{P}}\mathrm{ANDA}$ experiment by measuring antiprotons deflection at low angles. The measurement is performed by High Voltage Monolithic Active Pixel Sensors (HV-MAPS) that are silicon-pixel sensors placed on the CVD diamond support perpendicularly to the beam.

1.4 Straw tube tracking detectors for PANDA and HADES experiments

The Straw Tracking Stations (STS) detectors from the HADES are built on the basis of the central Straw Tube Tracker (STT) and the Forward Tracker (FT) of the future $\overline{\mathrm{P}}$ANDA experiment. The work is done in close collaboration between the groups from Jagiellonian University that developed the straw detector system and AGH University that developed the electronic readout system based on PASTTREC ASIC that is used for all mentioned detectors.

The above detectors provide the determination of drift time by measuring Time-Of-Arrival (TOA) and the identification of low-momentum particles by the Time-Over-Threshold (TOT) method measuring energy loss in straw trackers [15, 22]. For the first time, the TOT method was used by the ATLAS experiment [23] and the HADES in multi-wire drift chambers [24].

The STT and FT are built of the 10 mm diameter straw tube detectors [8, 9]. The grounded cathodes are made of aluminised Mylar foil of 27 μm thickness. The anodes are 20 μm gold plated tungsten wires connected to High Voltage (HV). The internal pressure of the gas is equal to 2 bars, which mechanically stabilises the straws and provides their self-support. Additional detector frames are used only for straw positioning. The straws are filled with the 90% Ar + 10% CO_2 gas mixture that minimises the ageing effects. The straw tubes provide a gas gain of about 5×10^4, about 130 ns maximum drift time, and a spatial resolution for minimum ionising protons of about 0.13 mm. The detection efficiency on a single straw was measured to be about 95% for 2 Gev/c momentum protons [9].

The $\overline{\mathrm{P}}$ANDA STT straw tubes are of 150 cm length and are arranged in 12 double layers around the beam axis in a hexagonal pattern and placed in an aluminium cylindrical frame as shown in Figure 1.6. The internal radius is 15 cm and the external radius is 41.8 cm. Layer 5 is inclined to +3° and layer 6 to -3° [8].

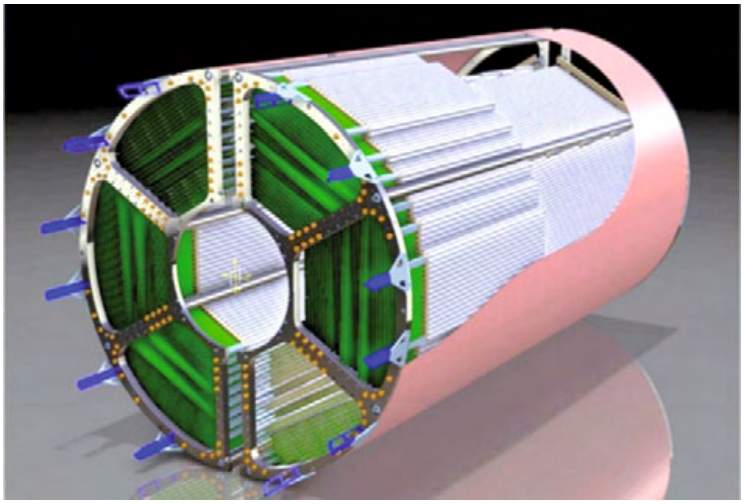


Figure 1.6: 3D visualisation of the STT for $\overline{\mathrm{P}}$ANDA experiment [8].

In the FT, straws are arranged in detector planes built of separate modules that contain 32 straws organised in two layers each. The length of the straws is adjusted to the tracking area of each detection plane (described in the next paragraph). The modules are mounted side-by-side on a support frame and, in this way, form a double-layer detection plane. The possibility of removing a single module without dismounting others simplifies the replacement of modules if necessary. Each module has its own two front-end electronic cards (Front-End Boards (FEBs)) and each of them comprises two PASTTREC ASICs [25]. Furthermore, multichannel Time-to-Digital Converter (TDC) are implemented in Trigger Readout Board (TRB) [26]. So far the experiment used version 3 of TRB, but there is work to replace it with updated version 5 that contains newer Field-Programmable Gate Arrays (FPGAs) and newer construction.

The FT contains six tracking station planes set in pairs. The first pair is installed in front of the dipole magnet (FT1, FT2), the second inside the magnet spacing (FT3, FT4), and the last behind the magnet (FT5, FT6). The schematic view of FT in the $\overline{\mathrm{P}}$ANDA experiment is presented in Figure 1.7 and the double layer mounted on a prototype frame in Figure 1.8. Each station contains four double layers of straw tubes, from which the first and last are vertically arranged and the middle ones are aligned by an inclination of, respectively, +5° and -5°. The tracking area at the FT stations ranges from 134×64 cm (FT1, FT2) to 392×120 cm (FT5, FT6) - a more detailed description can be found in [27].

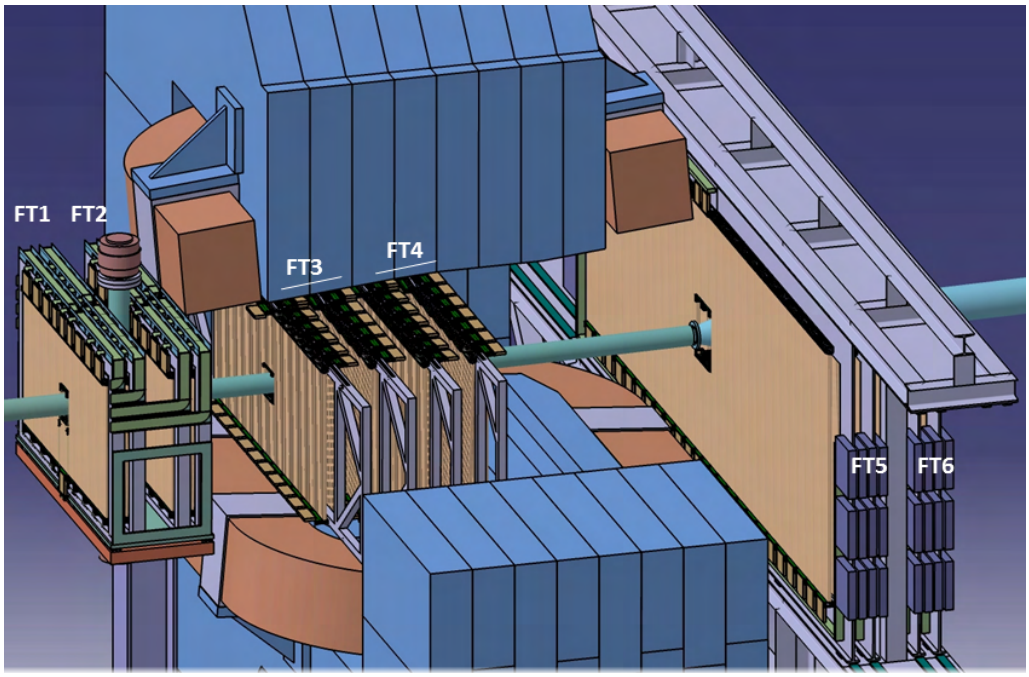


Figure 1.7: Schematic view of the FT stations position in $\overline{\mathrm{P}}$ANDA experiment with dipole magnet [9].

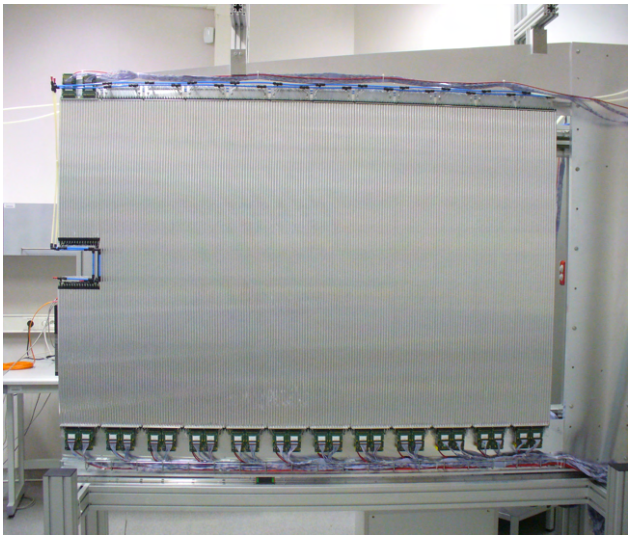
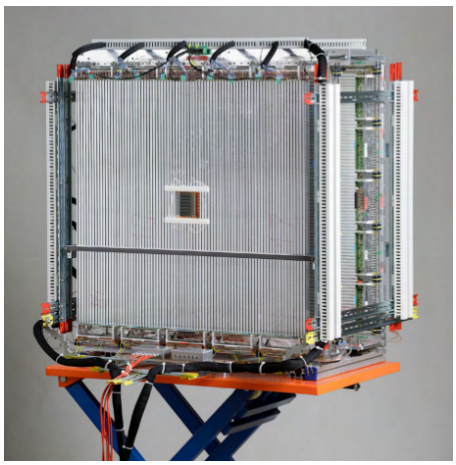
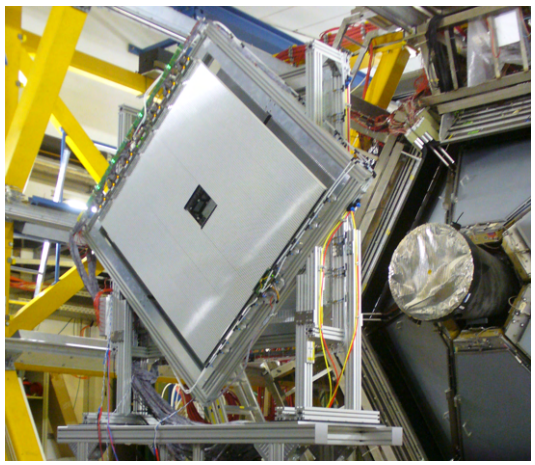


Figure 1.8: Double layer of straw tube detectors mounted on a prototype half-frame for the $\overline{\mathrm{P}}$ANDA FT [10].

Similarly to the FT, the STS detector for the HADES experiment will be built of the same straw modules differing in their alignment. Both STS1 and STS2 are constructed from four double layers, which are grouped into two double layers on a support structure. The double layers in STS1 are arranged at an angle of $0°$, $90°$, $90°$ and $0°$, respectively, in the vertical direction (see Figure 1.9a). The first two double layers of STS2 are placed at an angle of $0°$ and $90°$, while the second two double layers are aligned by an inclination of $+45°$ and $-45°$ (see Figure 1.9b). This solution will provide a clear multi-track event reconstruction. The straws have 76 cm (STS1) and 125 cm (STS2) length, and the modules have a width of 80 cm (STS1) and 112 cm (STS2). The most central straws at both stations are replaced by two shorter ones to create a central opening for the beam that has 8×8 cm (STS1) and 16×16 cm (STS2). In total, there are 704 (STS1) and 1024 straw (STS2) tubes.



(a) The STS1 for HADES [5].



(b) The STS2 installed in HADES [10].

Figure 1.9: Straw Tracking Stations for the HADES spectrometer.

1.5 Development of ASICs for modern experiments

As was shown in previous sections, high-energy physics experiments consist of many detector systems with different goals. Detectors contain a large number of channels placed, sometimes very dense, which causes the need of electronics miniaturisation and very low power consumption per channel. To detect particles with good resolution, low noise and good signal-to-noise ratio need to be provided. Moreover, contrary to most industrial applications, detectors work under very high radiation conditions, so front-end electronics should also be radiation resistant.

Therefore, there is a need for dedicated readout circuit Application-Specific Integrated Circuit (ASIC), that meet these requirements. Furthermore, depending on the detector type and its purpose, different demands might be imposed on the front-end electronics, requiring different gain (typically expressed as output voltage to input charge ratio), peaking time (how fast the signal must be processed to avoid the pill-up effect), or tail cancellation (which is particularly visible in gaseous detectors that generate an ion tail that needs to be compensated). ASICs evolved through the years together with technological development that allowed improvements in the field of particle detection.

The first stage of a typical readout system is a charge-sensitive low-noise preamplifier. The signal from the detector can be approximated as a Dirac delta, and the preamplifier can be approximated as an ideal integrator, which gives the voltage step in its output; see Figure 1.10. After this the shaper circuit is necessary to form the pulse shape and prevent pill-up effect. In tracking systems, where usually only information about the occurrence of a particle in the straw or pixel is needed, the binary front-end is sufficient. It is one of the oldest types because of its low-power features. After the preamplifier-shaper, the comparator detects only if the input signal is above the given threshold. The example of a circuit containing binary output is the PASTTREC readout ASIC that except preamplifier-shaper stage has an additional Tail Cancellation (TC) circuit. The ASIC is described in more detail in the next chapter.

With decreasing size in Complementary Metal–Oxide–Semiconductor (CMOS) technology and improvement in Analog-to-Digital Converter (ADC) architectures, they began to consume less power and be more power efficient (now less than 1 mW per channel) and provide more bits (typically 8-12 bits). Today, in spectroscopy, the energy is obtained by ADC, which converts the amplitude, providing a large dynamic range. The advantage is real-time digitisation, but on the other hand, it produces a large amount of data, which makes Digital Signal Processing (DSP) necessary. Further technological development allowed sending out more amounts of serialised data through high-speed links up to Gb/s to outer FPGA boards.

The increasing luminosity of experiments caused that nowadays not only the tracking and amplitude measurements are required but also high precision time measurements (for example, arrival time of a particle - TOA). This introduced the demand of TDC, which is part of this research and will be discussed in detail in further chapters. Originally, they were used as separate components (such as the TRB board in the readout of straw tubes in $\overline{\mathrm{P}}$ANDA and HADES), but together with

the progress in CMOS technology, it allowed them to be integrated with front-end electronics in every channel.

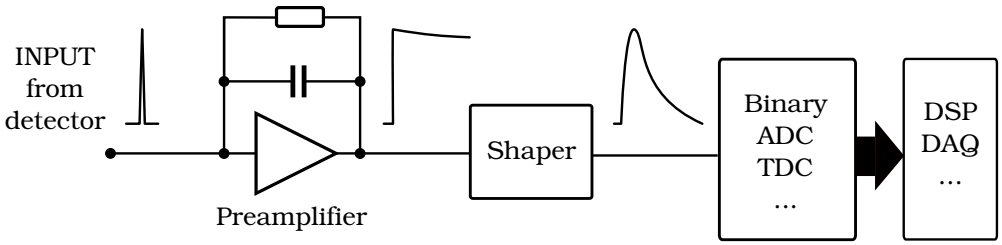


Figure 1.10: The example of signal path in typical ASIC channel for high-energy physics experiments.

Chapter 2

Front-end electronics measurements for HADES and PANDA experiments

The main focus of the thesis is on the readout electronics for the straw tracking systems in HADES and $\overline{\mathrm{P}}$ANDA experiments. The system provides the measurement of TOA that requires fast signal shaping. As mentioned in the previous chapter, both experiments use the TOT method to measure energy loss in straw tube trackers. This method implied stabilisation of the baseline on the front-end. All these requirements are met by dedicated readout electronics based on the PASTTREC ASIC described in Section 2.1.

Firstly, the optimisation of FEBs was done, which is described in Section 2.2. Since more than 5000 PASTTRECs are produced for both experiments, the mass tests of the chips are necessary. The measurement setup had to be prepared together with the measurement procedures to verify the operation of ASICs - Section 2.3. The first 280 PASTTRECs (140 FEBs) were measured, giving a production yield of 97.1% – results in Section 2.4. In the later stage, the boards with PASTTRECs were also tested with the entire detector chain, a straw tube module irradiated with the ^{55}Fe source. The results with the description of the measurement setup are presented in Section 2.5. The results of the mass tests together with the description of measurement setup and procedures have already been published in [10] and previously presented in the poster session during Topical Workshop on Electronics for Particle Physics (TWEPP) 2022 [28].

The STS was installed in HADES in 2020 and the first beam tests were performed in February 2021 with a proton beam up to 4.2 GeV energy [18]. At the beginning of 2022, at the GSI facility, the HADES experiment, together with the entire Forward Detector, was in phase-0 HADES beamtime for the first time with proton beam 4.5 GeV energy. As part of this work, a one-week internship was completed at the GSI facility during beamtime (Section 2.6).

2.1 PASTTREC readout ASIC and Front-End Board

As mentioned in the previous section 1.4 the straw tube trackers, used in $\overline{\mathrm{P}}$ANDA and HADES experiments, are arranged in modules. Each module of FT and STS detectors has two dedicated Front-End Board (FEB). Each of them comprises two **PA**NDA **STT RE**adout **C**hip (PASTTREC) chips, packed in a QFN68 (8x8 mm) package (ASIC0 and ASIC1 in Figure 2.1). Each ASIC has 8 front-end channels what gives 16 channel per board (ASIC0: channels 0–7, ASIC1: channels 8–15). Except for PASTTRECs, the FEB also includes decoupling capacitors, input protection diodes, and the Low Dropout (LDO) regulator. Previously, the board contained 4 LDOs but their number together with the size of the board, was reduced (see Section 2.2).

Figure 2.1: Photograph of FEB [10].

The PASTTREC [25] is a dedicated front-end ASIC for drift chambers and is used in the STT and FT in $\overline{\mathrm{P}}$ANDA experiment and STS in HADES experiment. ASIC is developed in 350-nm CMOS technology and provides analog and binary output, fast signal shaping with ion tail cancellation and stabilisation of the baseline.

The PASTTREC comprises 8 front-end channels, and each of them consists of a charge-sensitive preamplifier, two-stage shaper, and two outputs. The block diagram is shown in Figure 2.2. The preamplifier provides configurable gain K with four settings: 0.67 mV/fC, 1 mV/fC, 2 mV/fC and 4 mV/fC. The output of the preamplifier goes to the first stage of the shaper, with Pole Zero Cancellation (PZC) and an integrator, which provides a configurable peaking time: 10 ns, 15 ns, 20 ns and 35 ns, resulting in actual peaking times from 25 to 67 ns. The second stage of the shaper consists of the integrator and the TC circuit. The TC provides ion tail cancellation by setting two time constants, comprising two resistors and two capacitors. Each of them can be adjusted by a 3-bit Digital-to-Analog Converter (DAC), which gives 4096 possible configurations. To provide baseline stabilisation, which is a crucial part of this front-end, each channel comprises a Baseline Holder with a 5-bit baseline DAC to align all baselines (from -32 to 32 mV with 2 mV step). Each channel offers two outputs: analogue buffered output and digital Low-Voltage Differential Signalling (LVDS) output from Leading Edge Discriminator (LED).

Furthermore, PASTTREC also comprises a 7-bit global threshold DAC and biasing circuitry. To provide a precise voltage reference, a 1 V bandgap block is also included. Communication with ASIC is done using the slow control block with LVDS I/O .

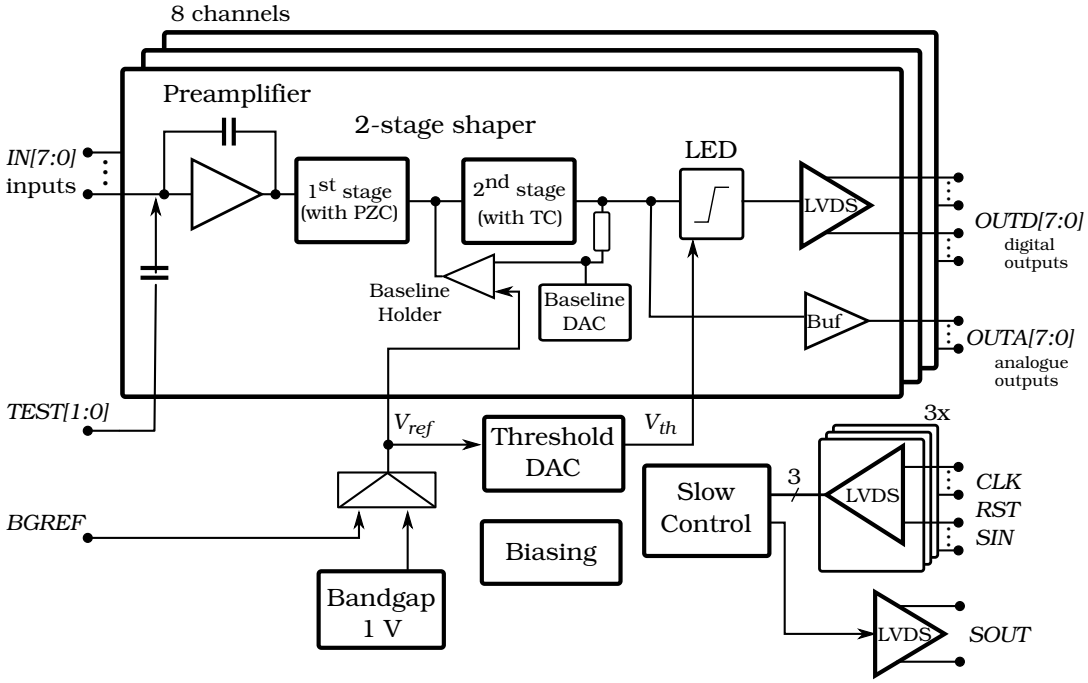


Figure 2.2: Block diagram of PASTTREC ASIC [10].

In the experiment, only the digital outputs of PASTTRECs are used. They are transmitted through ∼8 m long cable to the custom TRBv3 board of the Trigger Readout Board (TRB) family [26, 29] where the data are processed [30]. The TRBv3 board provides measurement of the leading and trailing edge time with 40 ps binning and 20 ps RMS time resolution by 192 multi-hit TDC channels. The TRB has four Lattice EXP3 LFE3-70 FPGAs controlled by the fifth Lattice EXP3 LFE3-150 central FPGA. Each of these four FPGAs has up to 64 channels – up to 4 FEBs can be connected to one FPGA. Every channel provides TOA and TOT measurement, and communication with PASTTREC through slow control (write and read its registers).

PASTTREC for MDC

The PASTTREC ASIC will be also used as a new front-end in MDC, developed by a group from Goethe University in Frankfurt, Germany. AGH University group is helping with the optimisation of the readout.

Until now, the MDC tracking system has used dedicated front-end electronics ASIC ASD-8 [31]. The ASICs were mounted on motherboards that also included TDC. Due to the different limitations of the existing readout system, an upgrade was needed. Based on the tests performed [32], PASTTREC ASIC was chosen as a good alternative to the previous read-out. Although ASD-8 has better time precision, PASTTREC will improve the energy loss measurements. Moreover, PASTTREC is more immune to noise and self-oscillations.

The default peaking time PASTTREC configuration used for the straw detectors in STT, FT and STS is equal to 20 ns, while ASD-8 provides 7 ns. However, there is the possibility of improving the time precision, since PASTTREC also contains shorter peaking time settings - 15 ns and 10 ns. Therefore, in the following sections, the results for peaking time 15 ns are also presented.

2.2 Front-End Board optimisation

Originally, FEB had 4 LDO regulators - two for each PASTTREC, for their analogue and digital parts. The space in experiments is limited, and the size of the front-end boards should be as small as possible. Due to this and to also reduce the number of components and what it brings, the price of the boards, the optimisation of FEBs was done.

Noise measurements were performed with a preliminary injection board setup. The tests were carried out with the $4mV20ns$ configuration and for:

1. The original FEB version - with four LDOs,
2. Board with 2 LDO regulators, one for the analogue part and one for the digital part,
3. Version with only one LDO regulator.

The obtained noise results are presented in Figure 2.3. It is shown that, regardless of the number of LDO regulators in FEB, the noise distribution between channels is practically the same.

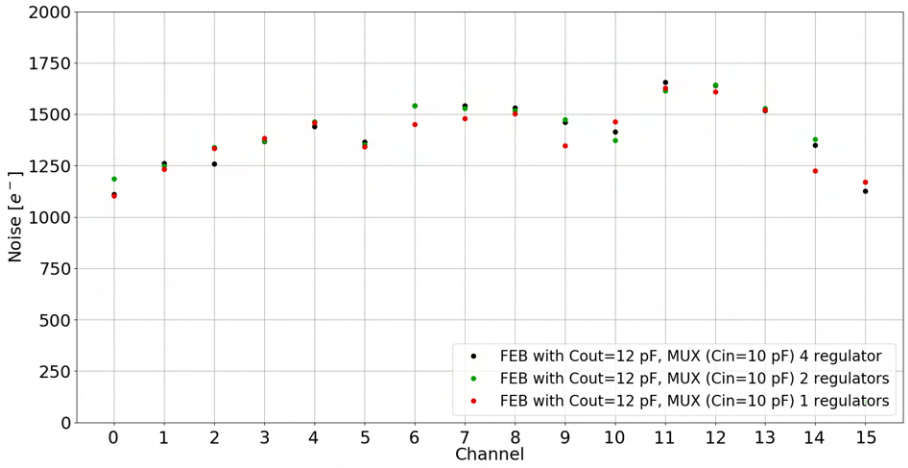
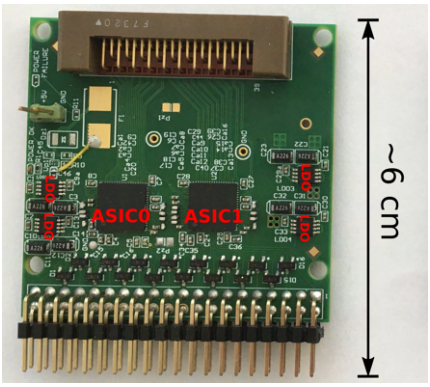


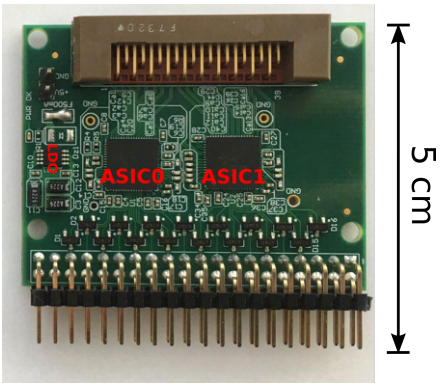
Figure 2.3: Noise of the FEB with different number of LDOs.

Based on the above measurements, the design of FEB was updated and the comparison of old and new versions of FEB can be seen in Figures 2.4a and 2.4b. The updated version has only one LDO regulator and its size was reduced to approximately 5 x 5.3 cm.

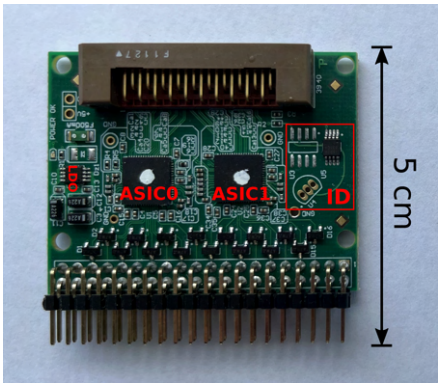
In further updates of the board, the chip ID function (to recognise chips easily in experiment) and the temperature measurement (to monitor the temperature and to cool down the system if needed) were added and realised by one circuit as marked in Figure 2.4c (red ID frame). Due to components accessibility difficulties, there are three footprints, and every time only one of them is assembled, but they have the same function.



(a) Old version of FEB (with four LDO regulators and larger size).



(b) New version of FEB (reduced size with one LDO).



(c) New version of FEB (reduced size with one LDO, chip ID and temperature measurement).

Figure 2.4: Comparison of old and new versions of FEBs.

One of the critical aspects of experiments, especially for STS in HADES, is the cooling system, so it was important to reduce the power consumption. For this reason, the performance of FEBs was verified for a lower power supply. In the earlier tests, FEBs were supplied with 5 V, but the ASICs require only 3.3 V power supply. The power consumption at 5 V is about 900 mW (∼56 mW per channel). It was verified that the FEBs work correctly until 3.5 V. Adding the safe dropout voltage for the LDO, the 3.8 V power supply was chosen which reduced power consumption to about 680 mW (∼43 mW per channel). The power consumption of the new version of FEB is presented in Figure 2.5.

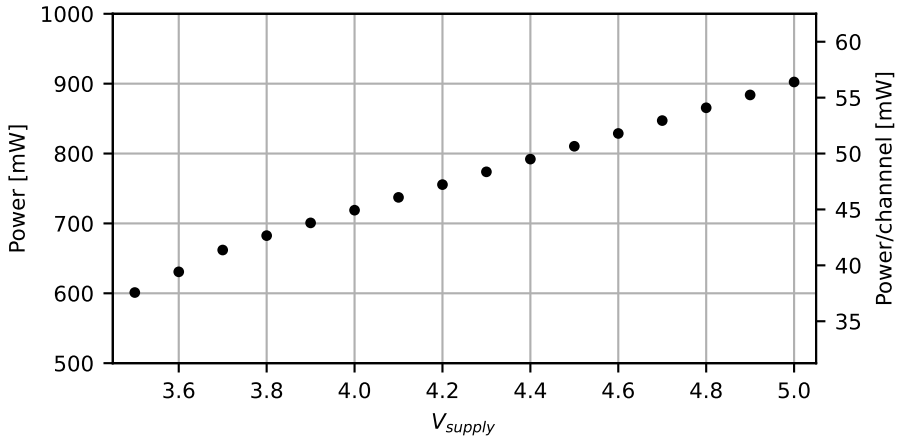


Figure 2.5: FEB power consumption in function of supply voltage.

All further measurements were performed with a new version of the FEB board (but without the chip ID and temperature measurement function) and a power supply voltage of 3.8 V.

2.3 Measurement setup and test procedures

Taking into account the production of more than 5000 PASTTRECs for both experiments and the need to verify them, the dedicated measurement setup was developed. The prepared setup provides multi-FEB measurements (up to 8 FEBs, 16 PASTTRECs in parallel). It delivers information about front-end parameters, like: baseline corrections, gain, and noise. Furthermore, the tests of the whole readout chain with the straw tube module, used in FT and STS, were performed.

2.3.1 Mass test measurement setup

To provide conditions similar to those with the straw tube detector, dedicated test boards, called Charge Injection Board (CIB), were prepared. The CIBs work as voltage-to-charge converters with the 15 fC/V conversion factor. Each of them requires the step-like signal to deliver the injection of charge to FEB. Therefore, the Agilent 81160A was used to generate four signals, which were then split into two, resulting in the 8 separate input signals for CIBs. The block diagram of the measurement setup is presented in Figure 2.6 and its photo in Figure 2.7.

First, the input signal in CIB passes through the -40 dB attenuator (block diagram of CIB in Figure 2.8) which ensures that the signals are small enough and correspond to the input range of the front-end. Subsequently, the signal is split into eight microcontroller-controlled relays and sent to one channel of each of the two PASTTRECs on FEB. After every relay, there is a voltage divider and then the signal is injected through the 10 pF capacitor. Each CIB was calibrated and its calibration factors are saved and related to the corresponding 4-bit hardware address of the board. It allows for automatic identification of the board in multi-board tests. The boards also provide the distribution of the power supply for FEB, prepared in the same way as in the experiment. The whole system is fully controlled by PC and Python scripts.

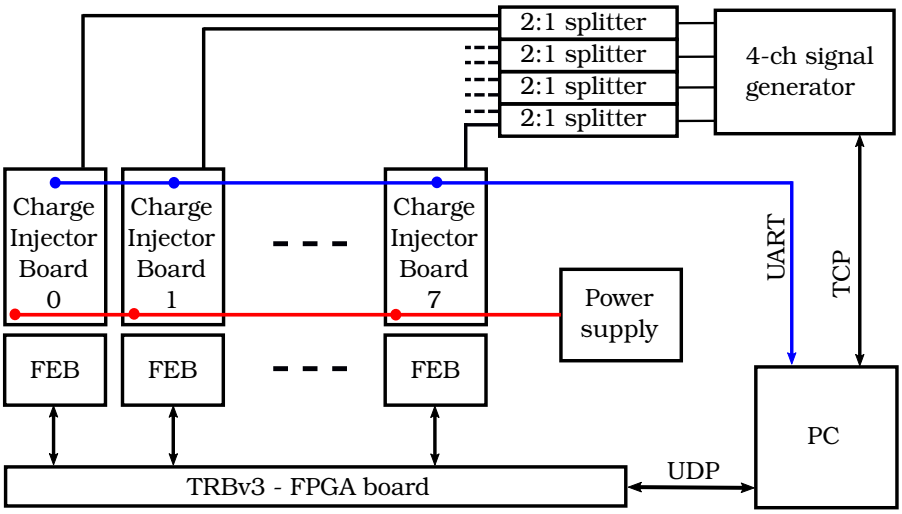


Figure 2.6: Block diagram of the measurement setup for 8 FEBs (16 PASTTRECs). The four step-like signals from the generator are split 2:1 and then injected through the dedicated CIB to FEBs. The communication with FEBs is done by TRBv3 FPGA board. The setup is controlled from a PC via Ethernet (UDP and TCP) and USB (UART) connections [10].

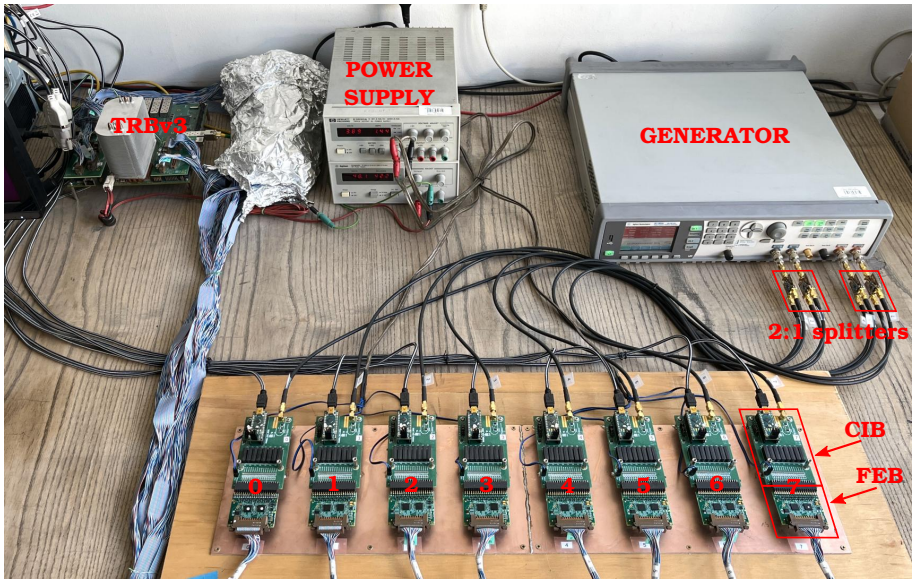


Figure 2.7: Photograph of measurement setup for 8 FEBs (16 PASTTRECs). The four signals from the generator are split 2:1 and then injected through the dedicated CIB to FEBs. The communication with FEBs is done by TRBv3 FPGA board. Everything is controlled from a PC (not shown in the photograph) [10].

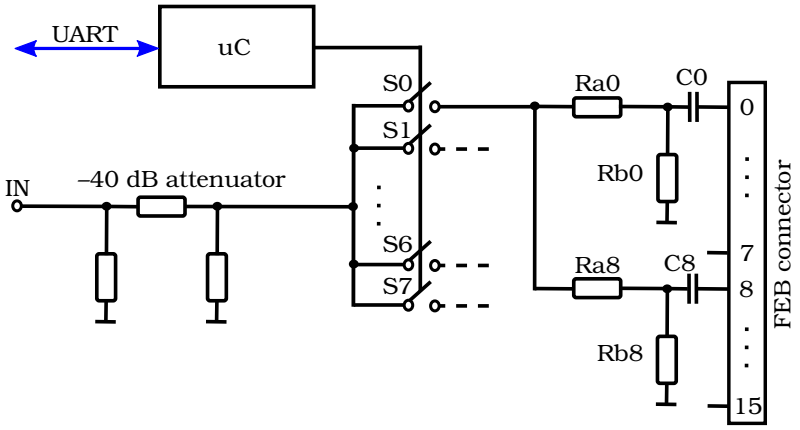


Figure 2.8: Block diagram of Charge Injection Board (CIB) used in PASTTREC test setup. The input signal goes through -40 dB attenuator, then through one of the 8 relays controlled by the microcontroller. The signal from one relay is distributed to a pair of FEB channels through voltage dividers (Ra0/Rb0–Ra15/Rb15). Finally, the signal is injected through 10 pF capacitors (C0-C15) [10].

2.3.2 Mass test procedures

The mass measurements for each FEB contained a series of test procedures that were performed to verify its performance. Tests were carried out for five selected configurations that vary with gain K, peaking time T_{peak} and tail cancellation settings as presented in Table 2.1. The configurations were selected from many settings studied in detail in [33] using the signal shape from analogue outputs of the PASTTREC. The selected configuration meets the requirements of the experiment [22]. The $4mV20ns$ was selected as the default configuration due to the highest signal-to-noise ratio and the possibility to use a lower gas gain, lower setting of HV of the straw tubes.

Table 2.1: Test configurations of PASTTREC used in following mass measurements.

Setting name	K [mV/fC]	T_{peak} [ns]	TC_{C1} [pF]	TC_{R1} [kΩ]	TC_{C2} [pF]	TC_{R2} [kΩ]
$1mV20ns$	1	20	10.5	27	0.9	20
$2mV15ns$	2	15	9	19	1.05	26
$2mV20ns$	2	20	10.5	31	1.2	20
$4mV15ns$	4	15	9	19	1.05	26
$4mV20ns$	4	20	10.5	27	0.9	20

Monotonicity of threshold and baseline DACs

As a first step, the monotonicity of the threshold and baseline DACs was verified. The DACs do not have test outputs; hence, their scans were performed using the TOT measurement. Each DAC and each ASIC channel was tested separately. The TOT measurement is not linear, but was sufficient to verify the monotonicity. To keep the TOT value as much as possible in the linear region, the generator amplitude was set to the maximum value (5 V). DACs do not depend on the ASIC configuration, hence measurements were made for only one configuration, *4mV20ns*, with the highest gain.

During the threshold DAC scan all baselines were set to 0 to keep the baseline as low as possible and provide the best linear region. The scan was carried out throughout the entire DAC range and in every step TOT was read. The TOT as a function of threshold DAC was obtained and then Differential Non-Linearity (DNL) was calculated and the monotonicity of DAC was verified. Since the results of TOT as a function of the threshold DAC are decreasing, only negative DNL values were accepted. The results of DNL for selected FEB (E019) are presented in Figure 2.9.

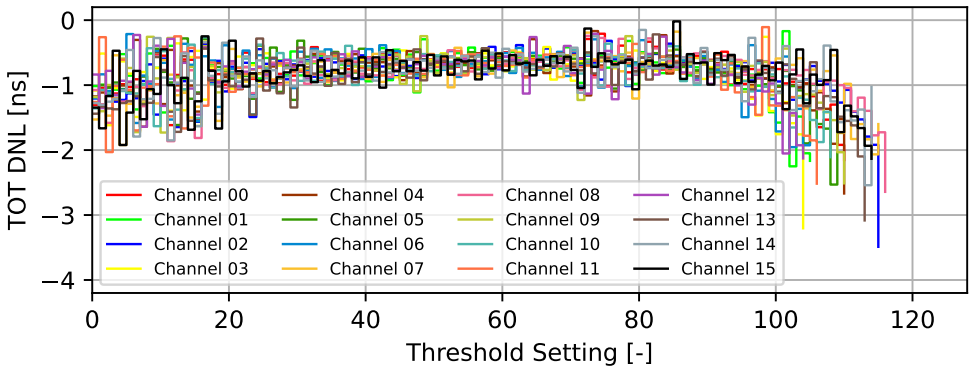


Figure 2.9: Results of the TOT DNL of threshold DACs for selected FEB (E019) for *4mV20ns* configuration.

During the baseline DACs scan, the threshold DAC was set to 24 to maintain the safe margin between the baseline and threshold level (about 10 LSB margin). Analogously to the threshold DAC scan, the baseline DAC was run throughout the entire DAC range and in every step the TOT value was read. Afterwards, the TOT in a function of threshold DAC was obtained and DNL was calculated. In the end, the monotonicity of DAC was verified. Since the results of TOT as a function of the baseline DACs are increasing, only positive DNL values were accepted. The results of DNL for selected FEB (E019) are presented in Figure 2.10.

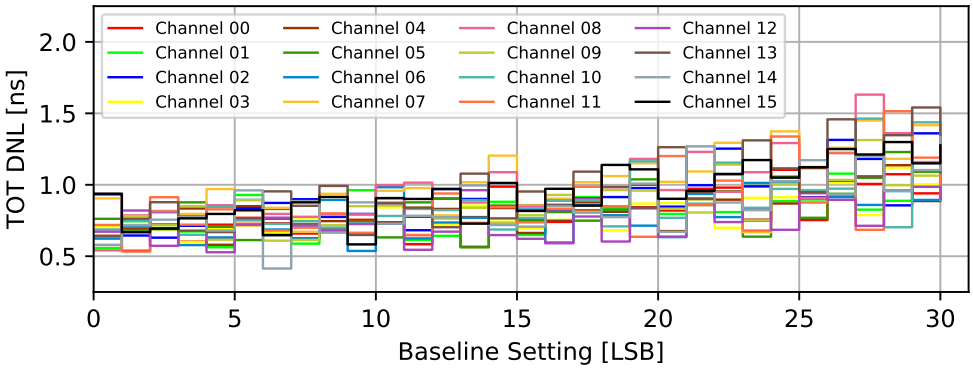
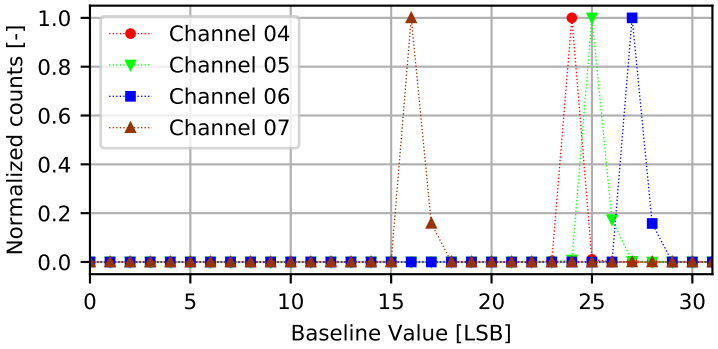


Figure 2.10: Results of the TOT DNL of baseline DACs for selected FEB (E019) for *4mV20ns* configuration.

Baseline scan

To equalise the baseline positions, a baseline scan is performed throughout the baseline DAC range. During the measurement, the threshold DAC is set to 0 mV (related to V_{ref}). In each step, from -32 mV to 32 mV with 2 mV step, the noise counts are read and its average is calculated. Based on the results, the baseline correction is obtained. Since the internal noise of PASTTREC is very low and sometimes no counts can be seen, the high-frequency (10 MHz) and low-amplitude signal is added to the inputs. The amplitude was experimentally adjusted to observe at least two baseline DAC values with a non-zero count number, as shown in Figure 2.11. The exemplary values of the baseline corrections for selected FEB are presented in Figure 2.12. It can be observed that the baseline values are almost the same for all configurations - baselines depend mostly on the input stage of the preamplifier, not on the other settings (gain, peaking time, or tail cancellation).



Channel	B_{corr} [LSB]	B_{DAC} [LSB]
ch04	24.01	24
ch05	25.14	25
ch06	27.14	27
ch07	16.14	16

Figure 2.11: Baseline scan measurement for selected channels of FEB E019 (left) and obtained parameters (right). B_{corr} corresponds to calculated baseline value and B_{DAC} is final value set by baseline DAC [10].

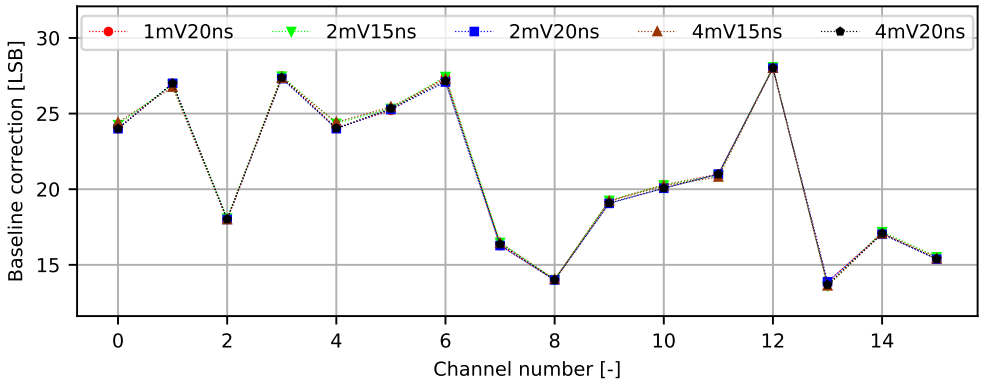
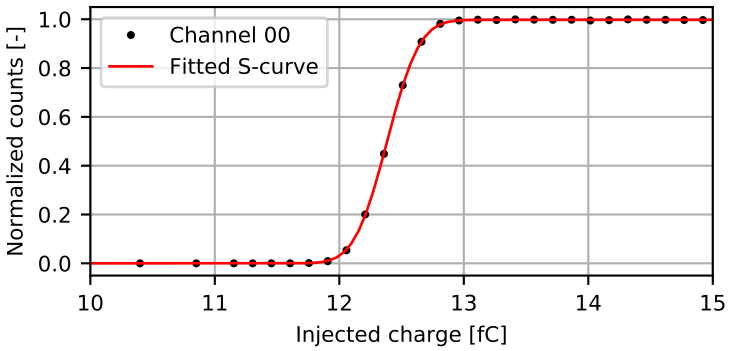


Figure 2.12: Results of the baseline correction for selected FEB (E019) for five different configurations.

S-curve scan

S-curve method is a standard method used to measure noise and gain in binary systems, and hence this method was used to parameterise PASTTREC. At each step, the amplitude of the signal was increased and the number of counts was read, forming the S-curve function. The counts were then normalised. To avoid artificially generated crosstalk, the signal was injected into each channel of ASIC separately. Assuming that the normalised number of counts in a function of the injected charge acts like a complementary error function, the appropriate fit was done. From the fit two parameters were obtained, μ_{sc}, the effective input charge for the given threshold and σ_{sc} which can be taken as Equivalent Noise Charge (ENC). An example of the measurement result is presented in Figure 2.13.



Parameter	Value
μ_{sc} [fC]	12.38
σ_{sc} [fC]	0.21

Figure 2.13: Example of the S-curve measurement for FEB E019 (left) and fit parameters (right). μ_{sc} corresponds to effective input charge of the given threshold and σ_{sc} is ENC value [10].

The S-curve scan was repeated for the threshold setting from 0 to 25. For each threshold setting, the effective input charge was obtained; the example result can be seen in Figure 2.14. From the linear fit to the obtained results, the gain and offset values were calculated.

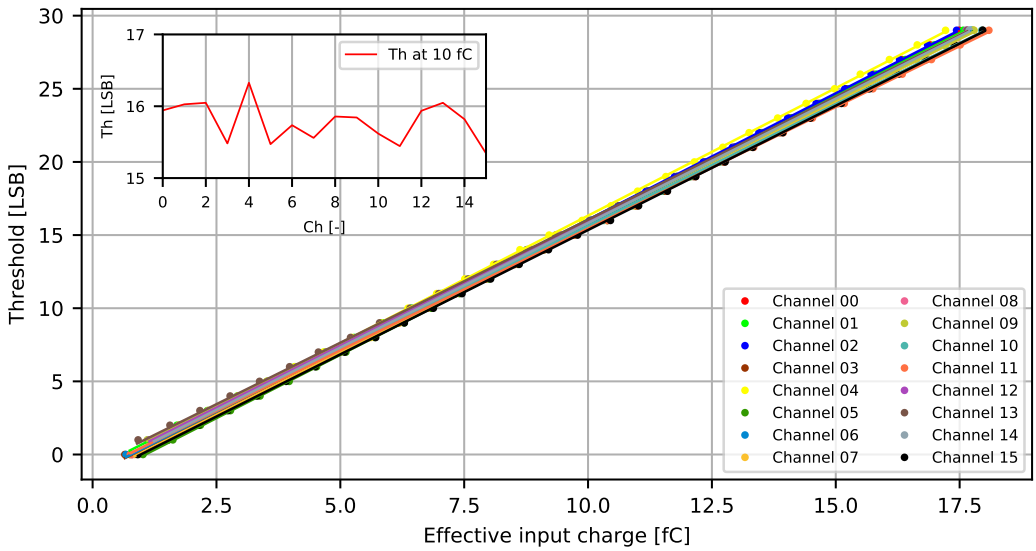


Figure 2.14: Response curve (effective input charge μ_{sc} parameter taken from S-curve fit – see Figure 2.13) for selected FEB (E019) and *4mV20ns* configuration. The threshold distribution of all channels at 10 fC charge is presented in upper left corner [10].

TOT scan

In the final system, the results of TOT allow one to obtain the deposited charge of the particle values. The goal of the TOT scan was to make corrections and obtain more accurate results of the injected charge. As a first attempt, the TOT scan was performed similarly to the s-curve scan. Charge was injected into each ASIC channel separately, but instead of counts, the value of TOT was read. The results obtained are shown in Figure 2.15. However, the obtained results did not correspond to the real particle charge values. The reason might be the shape of the injected signal that is not similar to the signal shape generated by the detector. Work on the TOT scan and shape of the input signal is still in progress.

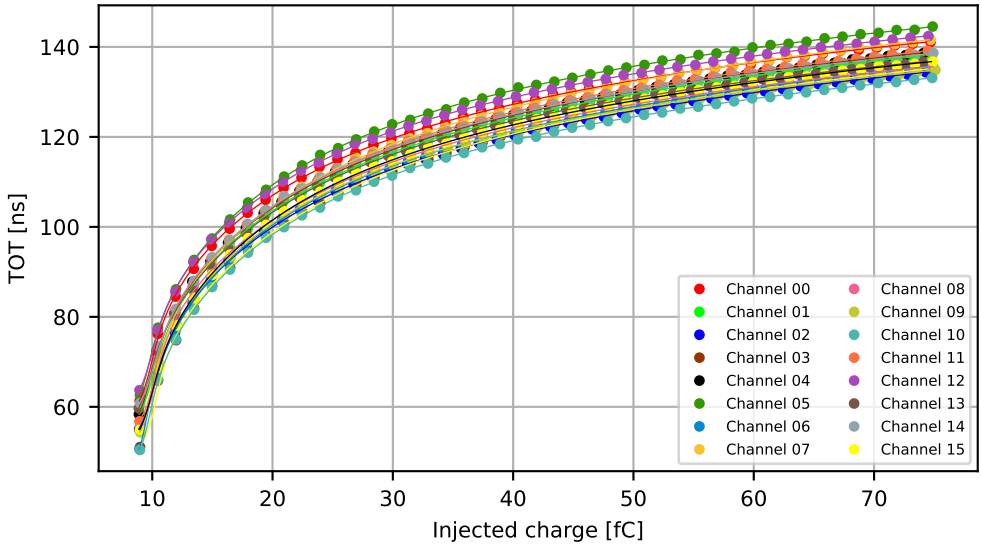


Figure 2.15: TOT as a function of the injected charge for Th=8 for selected FEB (E019) and $4mV20ns$ configuration.

2.3.3 Front-End Board qualification criteria

During test measurements, PASTTRECs were classified into one of three categories: I (good ASICs), II (backup ASICs), and III (rejected ASICs). To verify and add ASICs to one of these categories, the requirements have been established and are listed below. The 1. and 2. requirements are mandatory to be fulfilled; otherwise the chip is marked as rejected (III category). The last requirement classifies ASICs into one of the three categories. Summary information on qualification criteria and the number of PASTTRECs in each category is presented in Table 2.2.

1. Basic operation functionality of PASTTRECs. During this procedure, communication with ASICs is verified, the possibility to read and write all internal registers. Then the correct operation of the signal processing from the preamplifier to the discriminator output of each channel is checked. First, the response for a signal smaller than the threshold is tested (no counts on the output). Next, the response for signal with amplitude much larger than the threshold is checked (the number of counts should be proportional to the signal frequency). In both parts, the signal is injected into channels one by one.
   Duration of procedure: less than 1 minute.

2. Proper baseline correction factors from the *baseline scan* procedure. The baseline values obtained should be within the range of PASTTREC baseline DAC with a 1 LSB margin from the border values.
   Duration of procedure: less than 1 minute.

3. Noise and gain results (for the default configuration $4mV20ns$). The limit values are chosen arbitrarily and can still be changed in the future.

   - The noise (ENC) must be below 0.26 fC, if not PASTTREC is rejected (III category). The noise limit is more restrictive than 1 fC specified in $\overline{\mathrm{P}}$ANDA TDR [22].
   - The PASTTRECs with gain values (for each ASIC channel) within the $\pm 10\%$ range from mean gain value are classified in the I category. The PASTTRECs with at least one channel with gain value greater than $\pm 20\%$ from the mean value are rejected (III category). The rest of ASICs (with at least one channel with gain value between $\pm 10\%$ and $\pm 20\%$) are marked as backup (II category). Duration of the procedure: around 3.5 hours (S-curve scan for one threshold setting lasts 8 minutes).

FEBs containing at least one PASTTREC classified in category II or III are also marked as backup or rejected boards, respectively.

2.4 Mass test results of Front-End Board Measurements

2.4.1 Qualification test results

During the first part of the mass test measurements, in the pre-production stage in 2021, 140 FEBs were tested, which gave 280 PASTTRECs in total. The summary of qualification criteria with the number of PASTTRECs in each category is shown in Table 2.2.

Table 2.2: Summary of PASTTREC qualification tests according to procedure defined in section 2.3.3. Check marks indicate tests that the ASIC must pass to belong to the specific category. Numbers in parentheses after cross mark indicate how many chips failed the test [10].

Requirement	Category I	Category II	Category III
Basic functionality (1)	✓	✓	$\times(3)$
Baseline scan (2)	✓	✓	$\times(4)$
Noise below 0.26 fC (3)	✓	✓	$\times(0)$
Gain within $\pm 20\%$ from μ_g (3)	✓	✓	$\times(1)$
Gain within $\pm 10\%$ from μ_g (3)	✓	$\times(14)$	—
Total number	258	14	8

In the above tests, 8 out of all measured PASTTRECs have been rejected, classified as category III. Three did not respond during checking the slow control communication. In view of the small number of chips that did not respond, the issue was not investigated in detail, what the source of this misbehaviour was (if it was the PASTTREC, its packaging, or the front-end boards). The other four PASTTRECs had a too large spread of the baseline position. In this case, the baseline equalisation could be inefficient or even not possible to be made; hence, these ASICs were also rejected. The eighth PASTTREC was found with gain values lower than the mean gain by almost 30%. The results of the board containing this ASIC are presented in Figure 2.16 (channels of rejected ASIC are marked red). In summary, the total production yield of ASICs was 97.1%.

The other 14 PASTTRECs were classified into category II. All of them had at least one channel with a gain value that varied from the mean gain by more than $\pm 10\%$. The FEBs containing these PASTTRECs were also marked as backup boards.

All chips, with the exception of those that were not communicating, were taken to further analysis, even the rejected ones. In total, 277 PASTTRECs (2216 channels) are analysed in the following section 2.4.2.

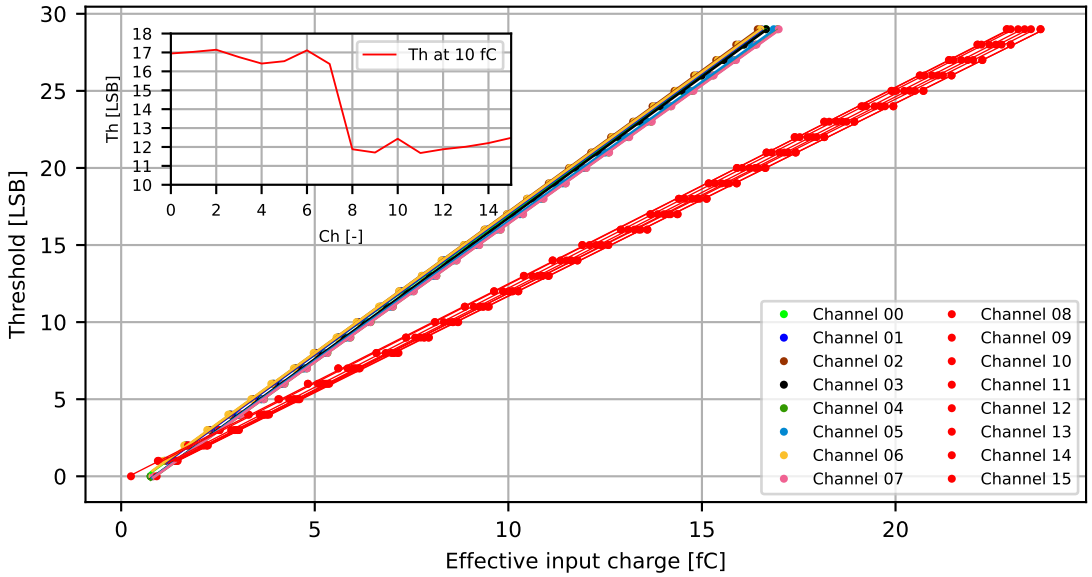
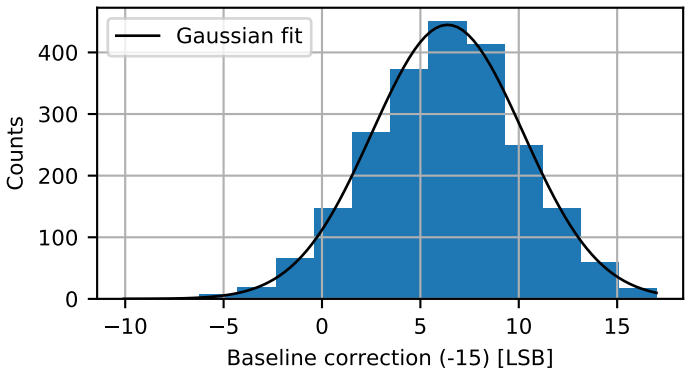


Figure 2.16: Response curve (effective input charge μ_{sc} parameter taken from S-curve fit – see Figure 2.13) for FEB (E018) containing rejected PASTTREC. The channels of rejected ASIC are marked red, and their gain values differ by almost 30%.

2.4.2 PASTTREC parameters results

Baseline correction

The baseline correction values for the default configuration *4mV20ns* are shown in the histogram in Figure 2.17. The statistical parameters of the results were calculated as unbiased estimators (also for all the following results) and are presented in the same figure (mean μ_b, standard deviation σ_b, standard deviation of the mean σ_{μ_b}). The Gaussian fit is also presented in the histogram for clarity. All baseline correction values are shown with -15 LSB shift due to the fact that the 15 LSB baseline DAC setting corresponds to a 0 mV offset.



Parameter	Value
μ_b [LSB]	6.364
σ_b [LSB]	3.9
σ_{μ_b} [LSB]	0.082

Figure 2.17: Distribution of baseline correction (values shifted by -15 LSB) for all 2216 channels (left) and its statistical parameters (right). Mean μ_b, standard deviation σ_b, and standard deviation of the mean σ_{μ_b} were calculated as unbiased estimator. Gaussian fit was added only for clarity [10].

Table 2.3: Statistical parameters (μ_{bch}, σ_{bch}, and $\sigma_{\mu_{bch}}$) of the baseline correction distributions for the groups of individual ASIC channels [10].

Parameter	ASIC channels							
	ch0	ch1	ch2	ch3	ch4	ch5	ch6	ch7
μ_{bch} [LSB]	6.29	6.33	6.45	6.24	6.48	6.29	6.53	6.30
σ_{bch} [LSB]	3.9	3.7	4.0	3.7	4.1	3.9	3.7	3.9
$\sigma_{\mu_{bch}}$ [LSB]	0.24	0.23	0.24	0.22	0.24	0.23	0.22	0.24

If we take into account the -15 LSB baseline DAC shift, we expect a mean value around 0 LSB. However, a systematic offset is observed in the baseline correction and the mean is 6.4 LSB, The standard deviation is less than 4 LSB and therefore 95% of the channels are within $\pm 2\sigma_b$, ± 8 LSB, which is half of the baseline DAC range (32 LSB). When comparing the results for individual channels of PASTTREC, which are shown in Figure 2.18 and their statistical parameters are shown in Table 2.3, we can see that the mean values for individual channels are in agreement with the mean for all channels within $\sigma_{\mu_{bch}}$. No significant differences are observed between different ASIC channels and the observed differences are purely statistical.

The same analysis was performed for other configurations (*1mV20ns*, *2mV15ns*, *2mV20ns*, *4mV15ns*). Their results are presented in Figures D.33 - D.36 for all channels and statistical parameters for individual channels in Tables D.3 - D.6, all in the Appendix. The same conclusions were made for them. Furthermore, regardless of the configuration, each channel has the same mean baseline correction within $\pm\sigma_{\mu_b}$ range alike the mean for all channels.

The purpose of the baseline measurement was to obtain corrections and align the baseline positions between all FEB channels. All further measurement results discussed in this Section are presented after the equalisation of the baselines.

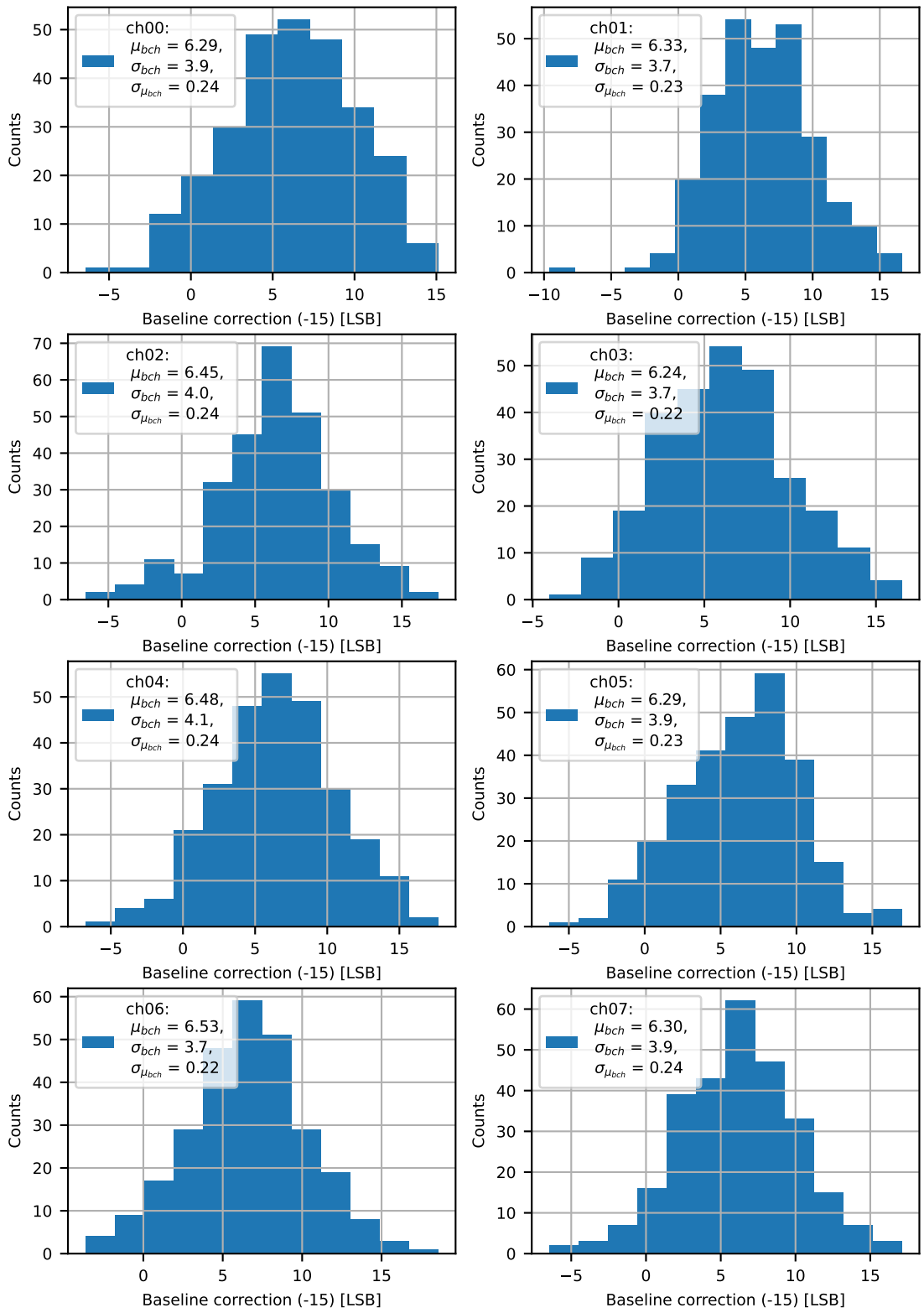


Figure 2.18: Distribution of the baseline correction for the groups of individual ASIC channels (values shifted by -15 LSB) and its statistical parameters (μ_{bch}, σ_{bch}, and $\sigma_{\mu_{bch}}$).

Gain and offset

Example gain and offset results for selected FEB (E019) and different configurations (*1mV20ns*, *2mV15ns*, *2mV20ns*, *4mV15ns*, *4mV20ns*) are presented in Figure 2.19. The threshold DAC has an LSB of approximately 2 mV, which was calculated in simulations, so the results obtained can easily be translated to mV/fC (gain) or mV (offset) by multiplying the results by 2. The gain values are similar to the set gain parameter K. The gain for peaking time 15 ns is larger than for the corresponding 20 ns configurations (around 12% larger for 4 mV/fC, and 25% for 2 mV/fC). The offset results are similar regardless of the configuration. The only exception is channel 13 in the *2mV15ns* and *4mV15ns* configurations that are 1 LSB smaller than for other settings.

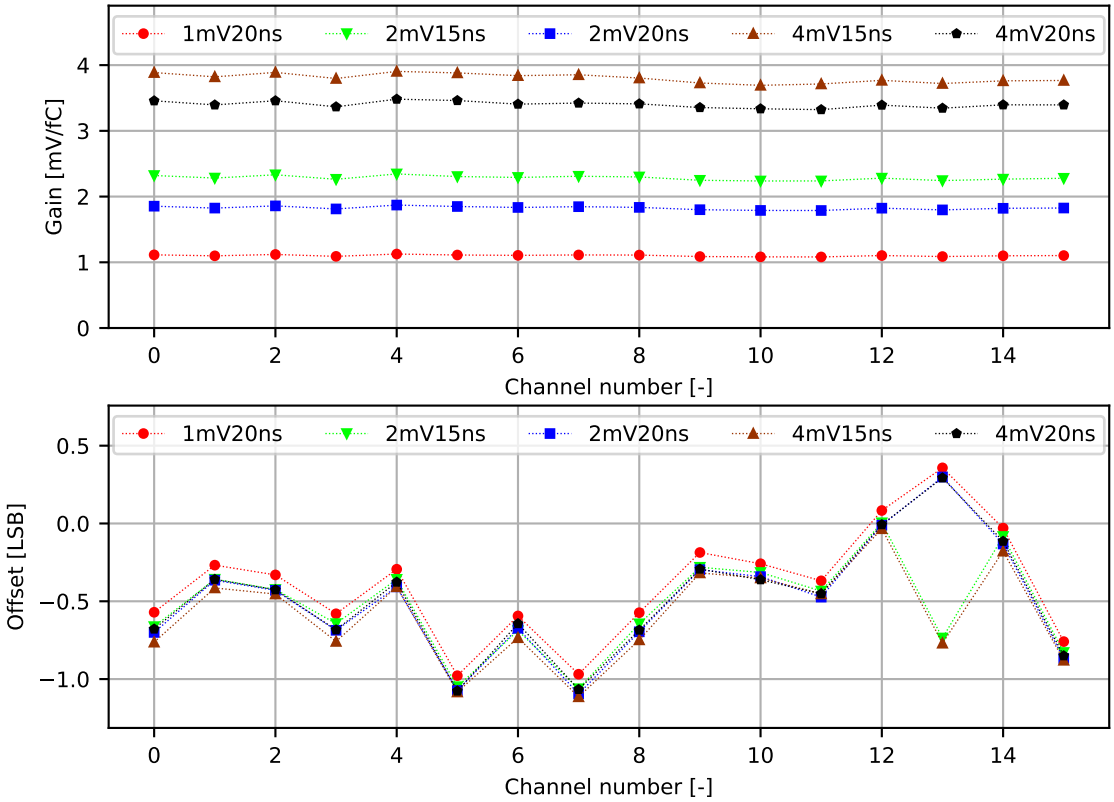
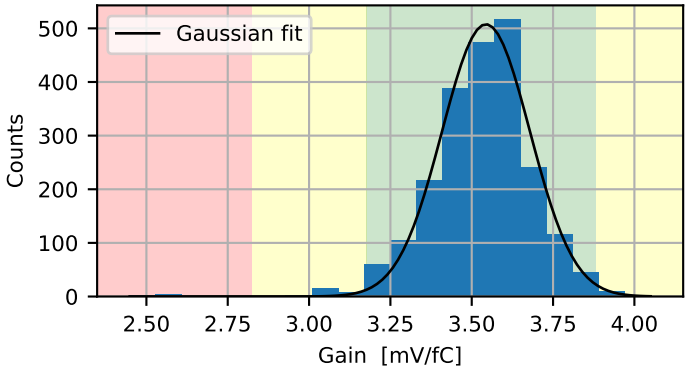


Figure 2.19: Gain (top) and offset (bottom) values for selected FEB (E019) for five different configurations.

The results of the gain values for all channels and the default configuration *4mV20ns* are presented in the histogram of Figure 2.20, together with its statistical parameters (μ_g, σ_g, σ_{μ_g}). The statistical parameters calculated for individual PASTTREC channels are shown in Figure 2.21 and Table 2.4. When comparing the mean values of the individual channels with the mean of all channels, we can see that they agree with each other within the $\pm 2\sigma_{\mu_{gch}}$ range. Therefore, no significant differences are observed between the ASIC channels and they are purely statistical.

The same analysis was performed for other configurations, which led to the same conclusions. The results for all channels and the statistical parameters for individual channels are shown in Figures D.37 - D.40 and Tables D.7 - D.10 in the Appendix, respectively.



Parameter	Value
μ_g [mV/fC]	3.5295
σ_g [mV/fC]	0.16
σ_{μ_g} [mV/fC]	0.0034

Figure 2.20: Distribution of gain values for all 2216 channels (left) and its statistical parameters (right). Mean μ_g, standard deviation σ_g, and standard deviation of the mean σ_{μ_g} were calculated as unbiased estimator. Gaussian fit was added only for clarity. ASIC qualification category ranges (see table 2.2) were marked in histogram with colours: green (cat. I), yellow (cat. II), and red (cat. III) [10].

Table 2.4: Statistical parameters (μ_{gch}, σ_{gch}, and $\sigma_{\mu_{gch}}$) of the gain value distributions for the groups of individual ASIC channels [10].

Parameter	ASIC channels							
	ch0	ch1	ch2	ch3	ch4	ch5	ch6	ch7
μ_{gch} [mV/fC]	3.5294	3.5319	3.5416	3.5155	3.5335	3.5251	3.5378	3.5211
σ_{gch} [mV/fC]	0.16	0.16	0.16	0.16	0.16	0.16	0.16	0.16
$\sigma_{\mu_{gch}}$ [mV/fC]	0.0094	0.0097	0.0098	0.0097	0.0098	0.0096	0.0097	0.0095

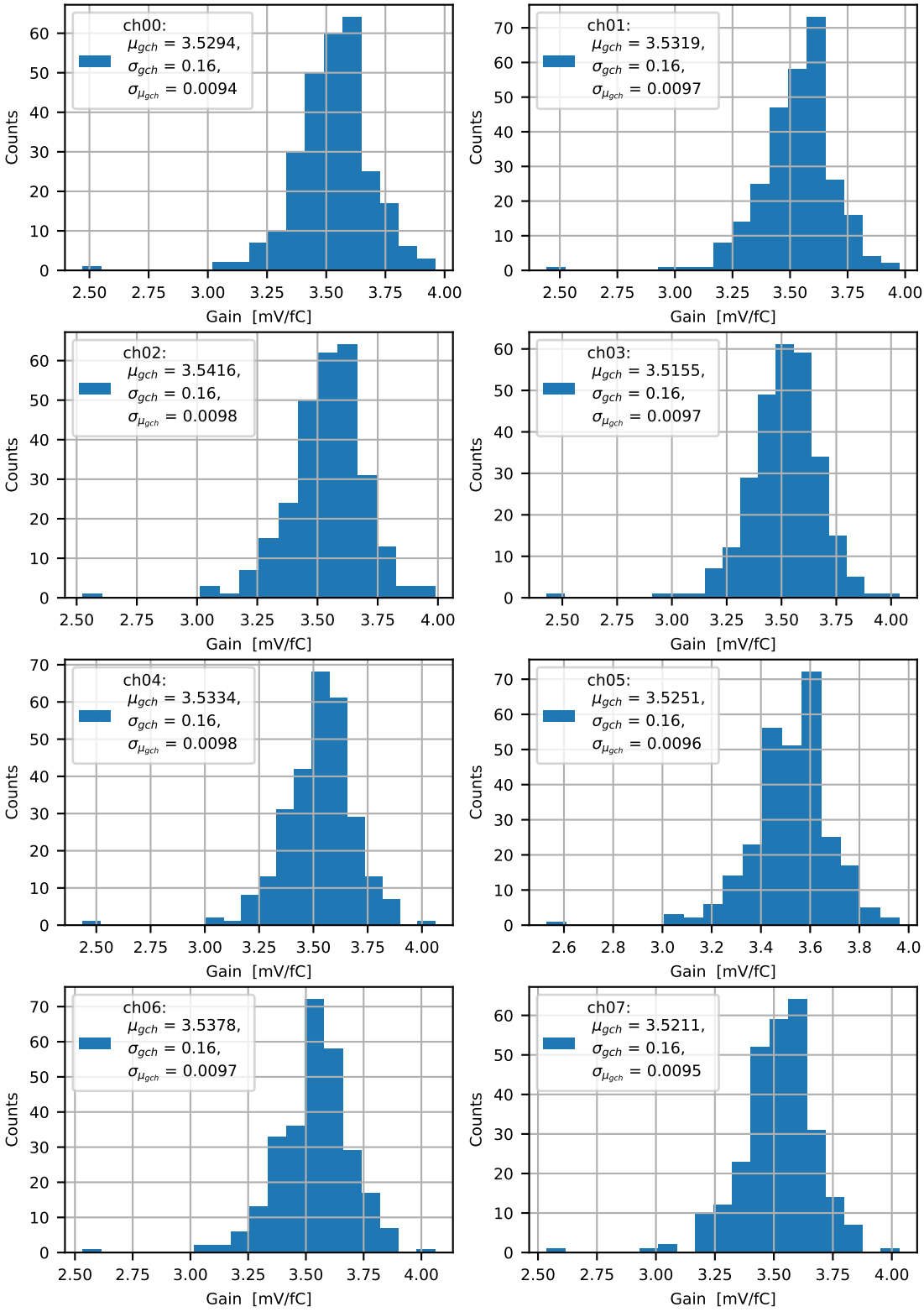
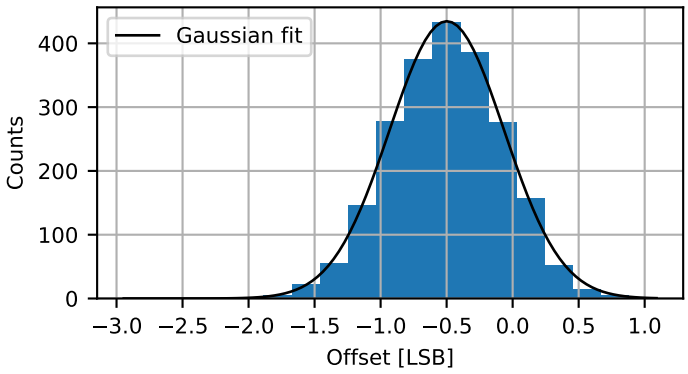


Figure 2.21: Distribution of the gain values for the groups of individual ASIC channels and its statistical parameters (μ_{gch}, σ_{gch}, and $\sigma_{\mu_{gch}}$).

The results of offset values for all channels and the default configuration *4mV20ns* are presented in the histogram in Figure 2.22, together with its statistical parameters (μ_f, σ_f, σ_{μ_f}). The values after baseline correction were expected to be 0 within 0.5 LSB of the baseline DAC. The results obtained are slightly different from this expectation. It may be the result of various causes (hysteresis of the discriminator, fitting procedure, TDC) that are difficult to precisely indicate. The statistical parameters calculated for individual PASTTREC channels are shown in Figure 2.23 and Table 2.5. It is seen that each mean of the individual channel agrees with the mean value for all channels within the $\pm 2\sigma_{\mu_{fch}}$ range and the observed differences are purely statistical.

The identical study was carried out for other configurations, leading to the same findings. The results for all channels and the statistical parameters for individual channels for other configurations are shown in Figures D.41 - D.44 and Tables D.11 - D.14 in the Appendix, respectively.



Parameter	Value
μ_f [LSB]	−0.5030
σ_f [LSB]	0.42
σ_{μ_f} [LSB]	0.0090

Figure 2.22: Distribution of offset values for all 2216 channels (left) and its statistical parameters (right). Mean μ_f, standard deviation σ_f, and standard deviation of the mean σ_{μ_f} were calculated as unbiased estimator. Gaussian fit was added only for clarity [10].

Table 2.5: Statistical parameters (μ_{fch}, σ_{fch}, and $\sigma_{\mu_{fch}}$) of the offset value distributions for the groups of individual ASIC channels [10].

Parameter	ASIC channels							
	ch0	ch1	ch2	ch3	ch4	ch5	ch6	ch7
μ_{fch} [LSB]	−0.513	−0.492	−0.532	−0.497	−0.484	−0.472	−0.515	−0.519
σ_{fch} [LSB]	0.43	0.42	0.44	0.41	0.451	0.42	0.43	0.39
$\sigma_{\mu_{fch}}$ [LSB]	0.026	0.025	0.026	0.025	0.027	0.025	0.026	0.024

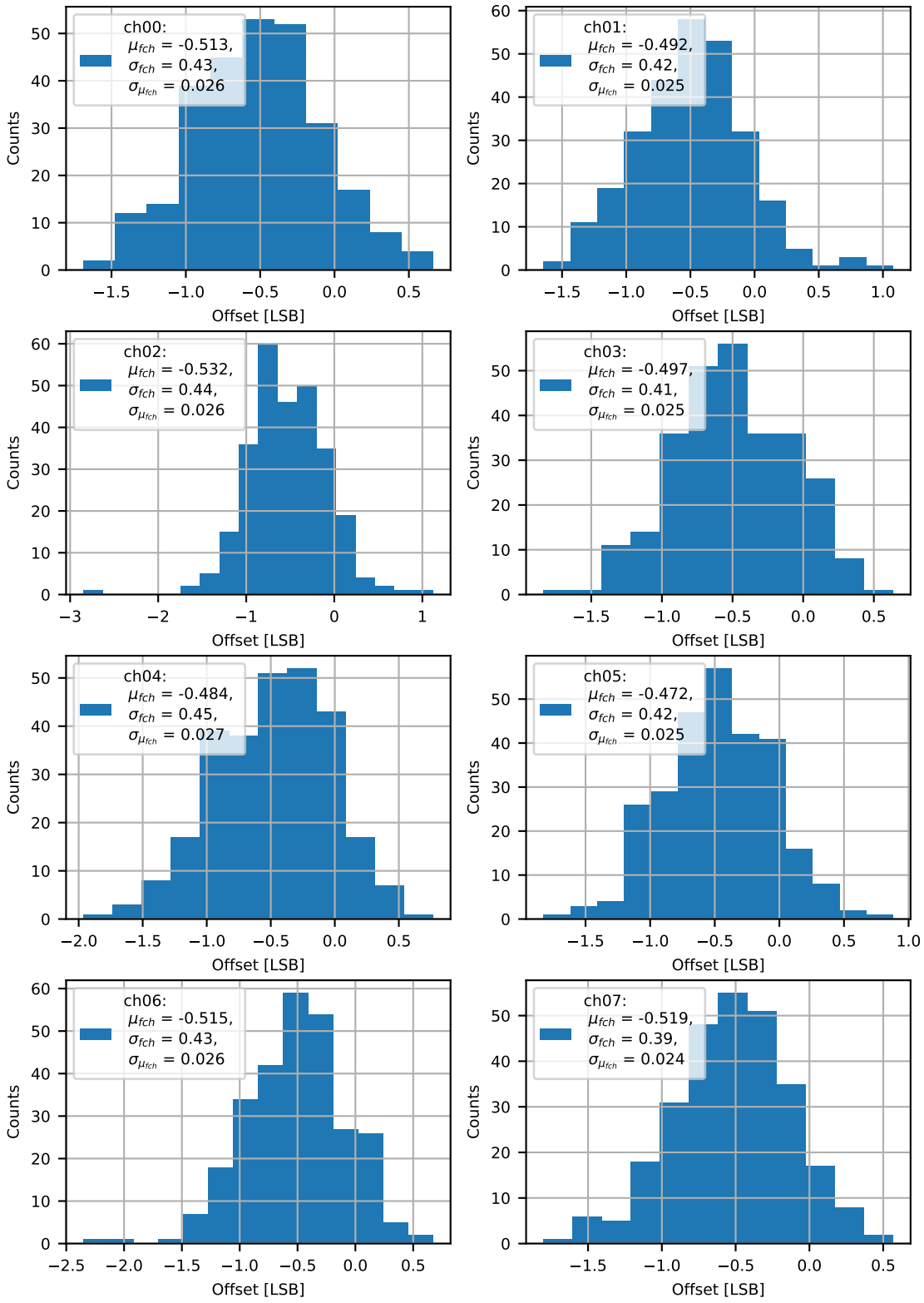


Figure 2.23: Distribution of the offset value for the groups of individual ASIC channels and its statistical parameters (μ_{fch}, σ_{fch}, and $\sigma_{\mu_{fch}}$).

Noise

Example noise results for selected FEB (E019) and different configurations are shown in Figure 2.24 (for Th = 40 mV). Noise for higher gain is smaller because the signal-to-noise ratio increases. The only exception is seen for the configuration *4mV15ns*. Since the default configurations were those with 20 ns peaking time, the configurations with 15 ns peaking time were not studied in detail. However, the change of peaking time and tail cancellation can strongly affect signal shaping and noise.

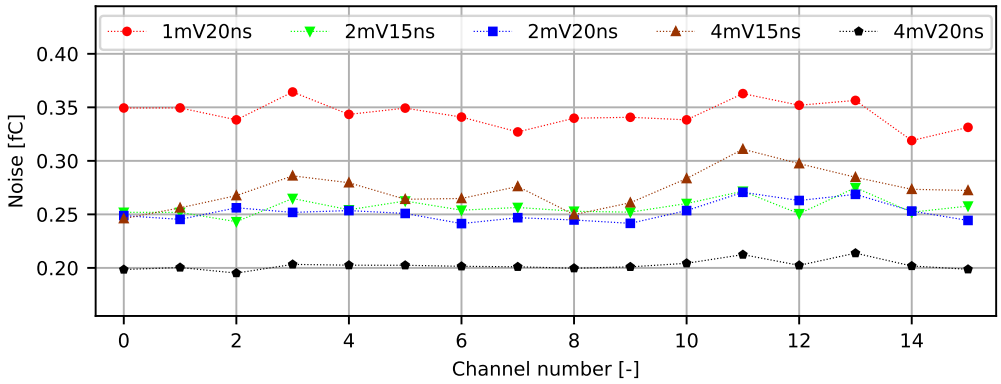
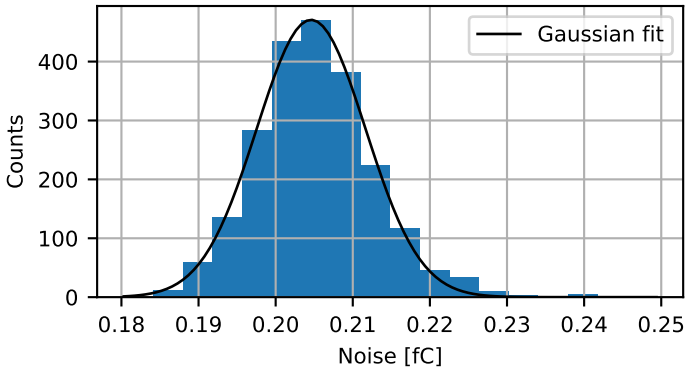


Figure 2.24: Noise values for selected FEB (E019) for five different configurations.

The noise value results for all channels and the default configuration *4mV20ns* are presented in the histogram in Figure 2.25, together with their statistical parameters (μ_n, σ_n, σ_{μ_n}). The statistical parameters obtained for individual channels are shown in Figure 2.26 and Table 2.6.



Parameter	Value
μ_n [fC]	0.20525
σ_n [fC]	0.0077
σ_{μ_n} [fC]	0.00016

Figure 2.25: Distribution of noise values for all (2216) channels (left) and its statistical parameters (right). Mean μ_n, standard deviation σ_n, and standard deviation of the mean σ_{μ_n} were calculated as unbiased estimator. Gaussian fit was added only for clarity [10].

Table 2.6: Statistical parameters (μ_{nch}, σ_{nch}, and $\sigma_{\mu_{nch}}$) of the noise value distributions for the groups of individual ASIC channels [10].

Parameter	ASIC channels							
	ch0	ch1	ch2	ch3	ch4	ch5	ch6	ch7
μ_{nch} [fC]	0.20148	0.20344	0.20502	0.20755	0.20712	0.20517	0.20448	0.20775
σ_{nch} [fC]	0.0070	0.0073	0.0079	0.0073	0.0075	0.0080	0.0071	0.0070
$\sigma_{\mu_{nch}}$ [fC]	0.00042	0.00044	0.00048	0.00044	0.00045	0.00048	0.00043	0.00042

The difference between the mean values for individual channels and the mean value for all channels is even greater than 10 $\sigma_{\mu_{nch}}$ for some channels. Noise parameters differ from all previously studied parameters because they depend on many factors. The baseline, gain, and offset parameters depend only on the operating point of the front-end, while noise depends also on other, especially external factors; for example, the middle channels may not pick up the same disturbances as the edge channels. External factors can easily affect the noise dispersion and can cause such a wide spread between channels. This analysis was performed for other configurations, which led to the same conclusions. The results for other configurations for all channels and statistical parameters for individual channels are presented in Figures D.45 - D.49 and Tables D.15 - D.19 in the Appendix.

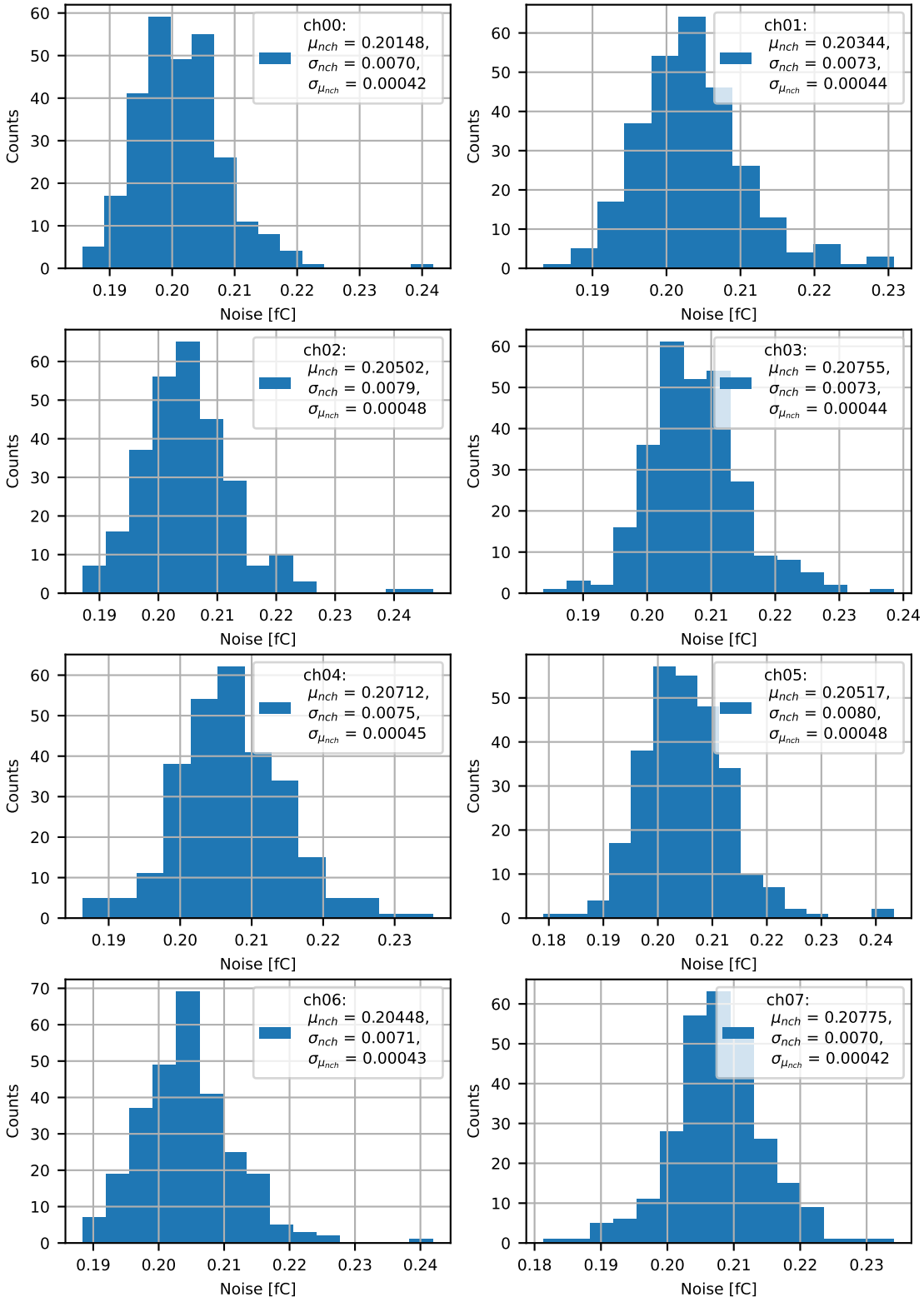


Figure 2.26: Distribution of the noise values for the groups of individual ASIC channels and its statistical parameters (μ_{nch}, σ_{nch}, and $\sigma_{\mu_{nch}}$).

2.5 Measurements with straw tubes and ^{55}Fe source

2.5.1 Measurement setup

In the next step, measurements with the complete detector chain were performed. The goal of them was to verify the results obtained from the mass tests (especially the baseline corrections) and to optimise the detector configuration for the experiments to achieve the best energy resolution based on the optimisation of the separation of peaks from the radioactive source ^{55}Fe.

Measurements were made in the Jagiellonian University laboratory. One module of 32 straws with connected 2 FEBs (used in FT in $\overline{\mathrm{P}}$ANDA and STS in HADES) was irradiated with ^{55}Fe source (setup shown in Figure 2.27). The gas mixture used in the straws gives ∼200 electron-ion pairs for the ^{55}Fe source, which corresponds to the number of pairs generated by Minimum-Ionising Particle (MIP) in the experiment. Gain in the straws (for the $\overline{\mathrm{P}}$ANDA experiment) can be approximated as (more can be found in [33]):

$$G = \mathrm{e}^{0.009 \cdot U - 5.3525} \tag{2.1}$$

where U is the high voltage at the anode. Therefore, the charge produced by ^{55}Fe can be calculated:

$$Q = 200 \cdot G \cdot 1.6 \cdot 10^{-19}[\mathrm{C}] \tag{2.2}$$

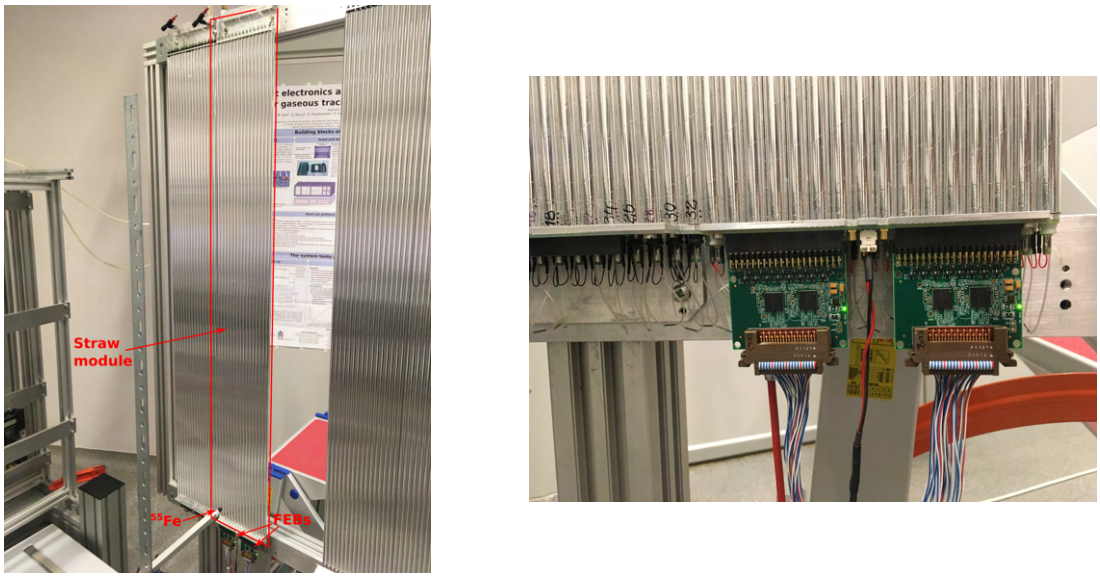


Figure 2.27: Measurement setup in the Jagiellonian University laboratory with two FEBs connected to one straw tube module and ^{55}Fe source.

In $\overline{\mathrm{P}}$ANDA experiment, two criteria, efficiency and level of misidentifications, were decided to be factors to evaluate the quality and performance of the detector - more details are given in the report of the particle identification at $\overline{\mathrm{P}}$ANDA experiment [34]. The basis for definitions is the assumption that the observed peaks from two particles are approximately two Gaussian distributions. Therefore, taking two normalised Gaussian distributions $G_0(x)$ and $G_1(x)$ (of peak P0 and P1, respectively, where $\mu_0 < \mu_1$), one can calculate the efficiency as follows.

$$\epsilon = \int_{-\infty}^{x_0} G_0(x)dx \tag{2.3}$$

and misidentifications level as:

$$\mathrm{misid} = \int_{-\infty}^{x_0} G_1(x)dx \tag{2.4}$$

where, x_0 is the point between peaks P0 and P1. To find x_0, the separation power S was defined and calculated as:

$$S = \frac{|\mu_1 - \mu_0|}{\sigma_{avg}} = \frac{|\mu_1 - \mu_0|}{\frac{1}{2}(\sigma_1 + \sigma_0)}, \tag{2.5}$$

where μ_0 and μ_1 are mean positions and σ_0 and σ_1 are standard deviations of the two peaks (for ^{55}Fe spectrum it is the escape peak of the argon and the main peak, respectively) fitted with Gaussian distributions. In general, the separation power defines the distance between two peaks (their means) in units of their average standard deviations; e.g., $S = 2$ is 2σ distance between peaks, $S = 4$ is 4σ distance between peaks, etc. In conclusion, the larger the S, the more distance there is between the peaks and the better the identification of the peaks. Then, one can take $x_0 = \mu_0 + S \cdot \sigma_{avg}/2$ and calculate ϵ or misid.

The common method in the $\overline{\mathrm{P}}$ANDA and HADES experiments to measure the energy of the particles is the measurement of TOT. Therefore, the straws irradiated with the ^{55}Fe source allowed to collect its TOT spectra for different configurations. The spectra collected after 20 million events were recorded in the read-out system. The ^{55}Fe spectrum has two peaks, the main peak (5.9 keV) and the argon escape peak (2.9 keV). Since the TOT as a function of the injected charge is non-linear, the separation power S (calculated from (2.5)) of these two peaks was taken as the main parameter to define the quality of the measurement in this work. The TOT measurement is strongly non-linearly dependent on the particle momentum and discrimination level, therefore, the separation power of ^{55}Fe peaks is not equivalent to the separation of pions, kaons, and protons in a real experiment. However, the separation power studies of ^{55}Fe give a general overview of the operation of the detector.

The baseline correction verification with TOT scans is presented in 2.5.3 and TOT separation studies for different configurations in 2.5.4.

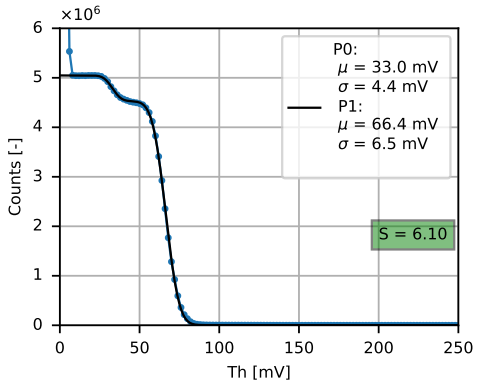
2.5.2 Threshold scan

Since TOT is not linear as a function of energy, a threshold scan was performed first to obtain linear energy deposition measurements with the entire detector chain and the ^{55}Fe source. It also allowed to get the reference separation power and verify the operation of the system with the detector. The straws were irradiated with the same ^{55}Fe source, but instead of TOT, the number of counts was read. During measurement, the threshold DAC setting was changed from 0 to 127 LSB every 1 LSB and the counts were read every 1 minute. The results obtained in this way formed two s-curves whose fit allowed one to calculate the separation power of the peaks.

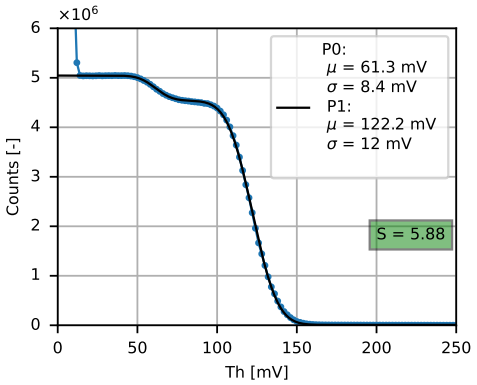
Measurements were made for the following configurations:

1. *4mV20ns* and *2mV20ns* at HV = 1550V (Figure 2.28),
2. *2mV20ns* and *1mV20ns* at HV = 1600V (Figure 2.29),
3. To get the main peak (P1) in almost the same position (about 120 mV): *4mV20ns* at HV = 1550 V, *2mV20ns* at HV = 1610 V and *1mV20ns* at HV = 1690 V (Figure 2.30).

The cumulative scan results, for all 32 channels, are presented together with the mean (μ) and standard deviation (σ) of both peaks and their separation power (S). Furthermore, all important parameters are presented in Table 2.7.

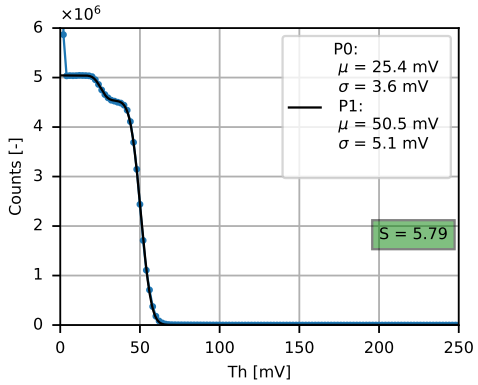


(a) *2mV20ns* configuration.

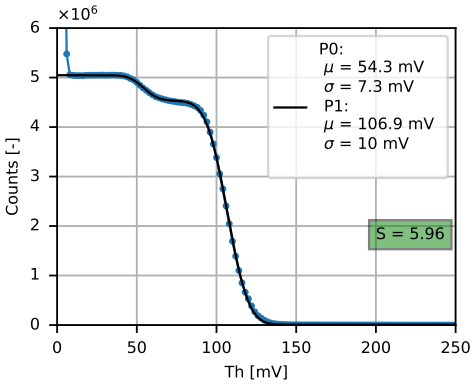


(b) *4mV20ns* configuration.

Figure 2.28: Cumulative threshold scans at HV = 1550 V. The μ and σ were obtained from s-curves fit and separation power S calculated according to the formula (2.5).



(a) *1mV20ns* configuration.



(b) *2mV20ns* configuration.

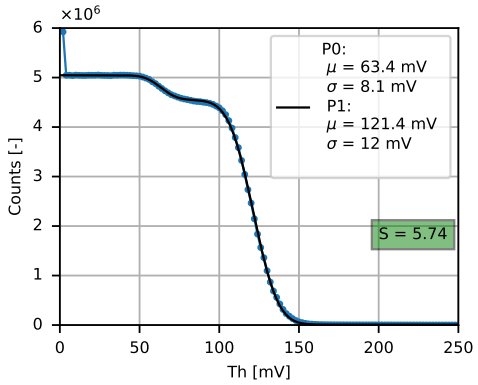
Figure 2.29: Cumulative threshold scans at HV = 1600 V. The μ and σ were obtained from s-curves fit and separation power S calculated according to the formula (2.5).

As was mentioned before, for the ^{55}Fe source two peaks are expected: the main (P1) at 5.9 keV energy and the argon escape peak (P0) at 2.9 keV; therefore, the P1/P0 ratio should be approximately 2. For all the measurements performed, the ratio is around 2 which confirms the linearity of this method as a function of energy.

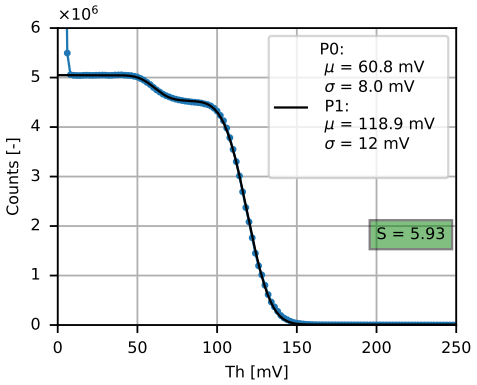
Regardless of the high voltage setting on the straws, the separation power and the σ/μ ratio are similar and differ less than 5% (see Table 2.7). The S is in the range from 5.7 to 6.1. A small decrease in the separation power (increase of noise) is observed with increasing HV. It is caused by the increasing dispersion of gas detector amplification; the front-end electronic noise is independent of the HV. Moreover small increase of separation power is seen for the lowest gain configuration; the electronic noise is larger, smaller signal-to-noise ratio.

Table 2.7: Threshold scan parameters. The μ and σ were obtained from s-curves fit (for the main peak (P1) and the argon escape peak (P0) of the ^{55}Fe source) and separation power S calculated according to the formula (2.5).

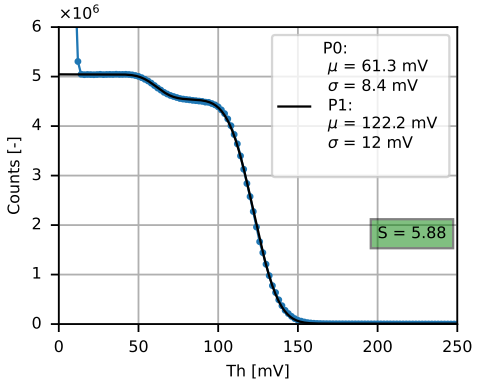
Setting	HV [V]	μ_{P0} [mV]	σ_{P0} [mV]	μ_{P0}/σ_{P0} [-]	μ_{P1} [mV]	σ_{P1} [mV]	μ_{P1}/σ_{P1} [-]	S [-]
1mV20ns	1600	25.4	3.6	7.1	50.5	5.1	9.9	5.79
2mV20ns	1600	54.3	7.3	7.4	106.9	10	10.7	5.96
2mV20ns	1550	33.0	4.4	7.5	66.4	6.5	10.2	6.10
4mV20ns	1550	61.3	8.4	7.3	122.2	12	10.2	5.88
1mV20ns	1690	63.4	8.1	7.8	121.4	12	10.1	5.74
2mV20ns	1610	60.8	8.0	7.6	118.9	12	9.9	5.93



(a) *1mV20ns* configuration (HV = 1690 V).



(b) *2mV20ns* configuration (HV = 1610 V).



(c) *4mV20ns* configuration (HV = 1550 V).

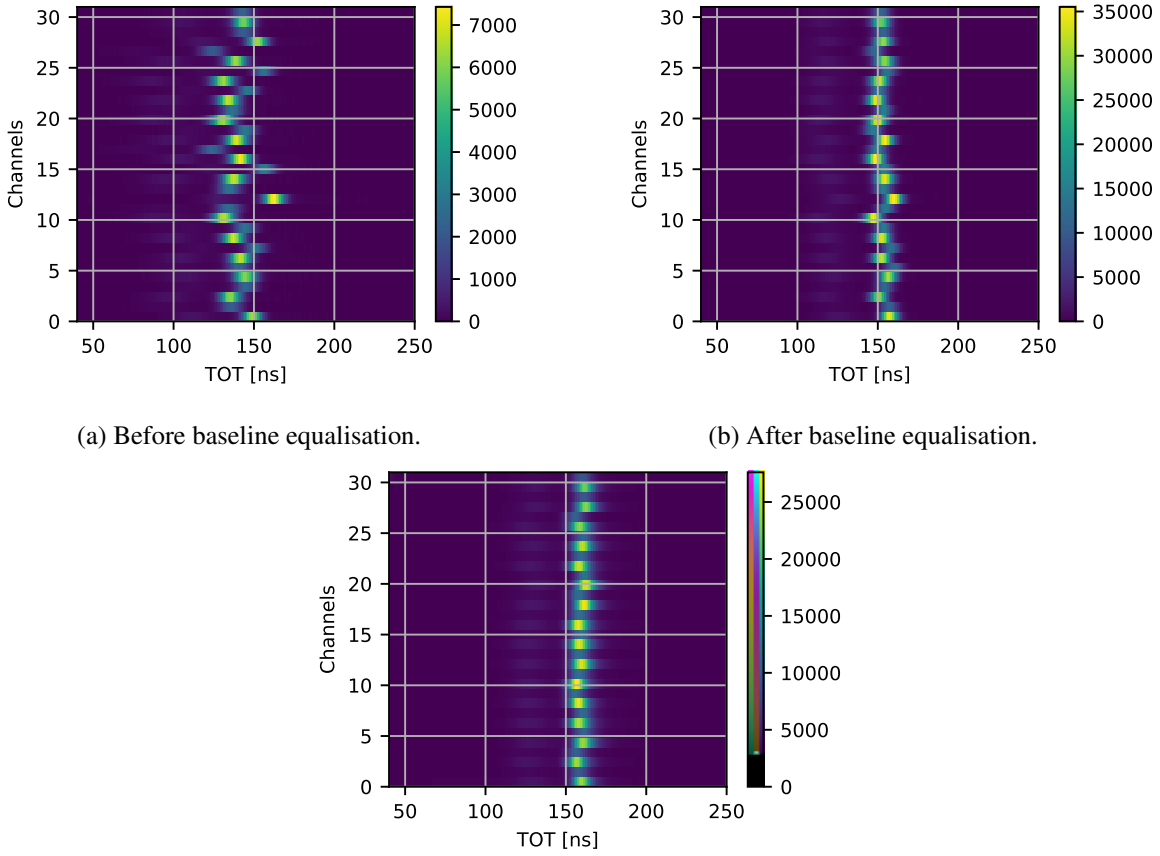
Figure 2.30: Cumulative threshold scans for *1mV20ns*, *2mV20ns* and *4mV20ns* with the main peak (P1) at the same position (∼120 mV). The μ and σ were obtained from s-curves fit and separation power S calculated according to the formula (2.5).

2.5.3 TOT scan - baseline correction verification

To verify the baseline correction parameters obtained in the mass tests, ^{55}Fe TOT spectra were collected before and after baseline equalisation. 2D spectra are shown in Figure 2.31 and the cumulative spectra for all 32 channels together with the Gaussian fit in Figures 2.32 (before baseline equalisation) and 2.33 (after baseline equalisation). The alignment of the main peak positions is visible in the 2D spectra (Figure 2.31a and Figure 2.31b). Additionally, one can observe that every second channel has a smaller number of counts, which is the effect of the architecture of the straw module. The module forms two rows of straws, which causes every second straw to receive less radiation from the source (back straws) than those placed in the front.

The improvement in spectrum quality after baseline equalisation and peak separation is clearly visible. Separation power increases from 3.88 to 4.33 (see Figures 2.32 and 2.33). This confirms the usefulness of the baseline scan procedure.

At the end, the $\pm$1-2 LSB mannual corrections were made to verify whether further improvement in baseline equalisation can be introduced. The results of these small modifications are shown in the 2D spectra in Figure 2.31c and in the cumulative spectrum for all channels together with the Gaussian fit in Figure 2.34. The slight improvement can be seen in separation power increase from 4.33 to 4.39. The baseline equalisation scan is made at $\mathrm{Th} = 0$ mV and then in the experiment the threshold is set to $\mathrm{Th} = 20 - 40$ mV, hence small difference in the gains of individual channels may cause differences between the baselines of individual channels. The differences are very small, but some improvement can be made in future procedures.

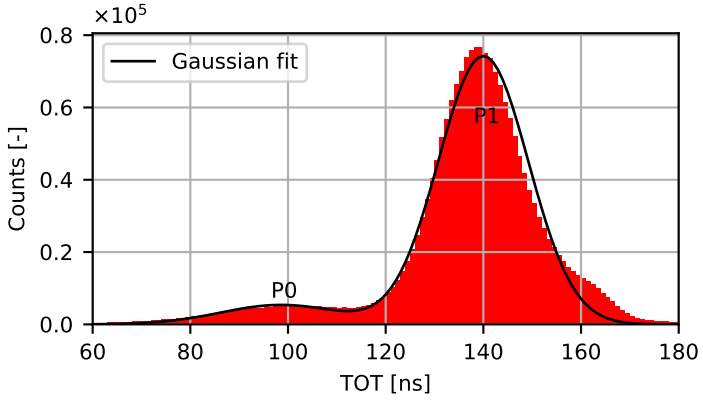


(a) Before baseline equalisation.

(b) After baseline equalisation.

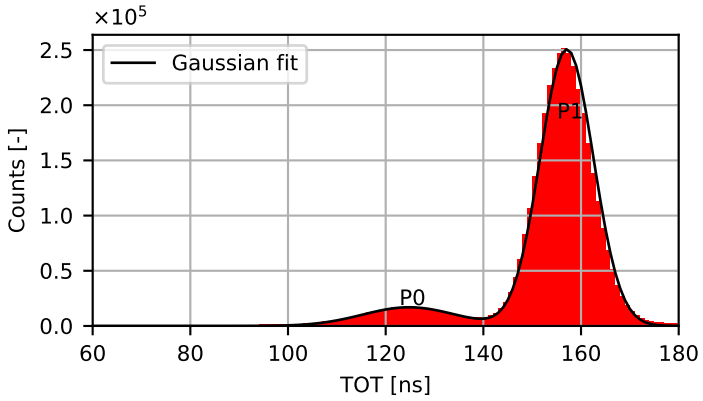
(c) After baseline equalisation and mannual corrections.

Figure 2.31: ^{55}Fe 2D spectra for a straw module (32 channels).



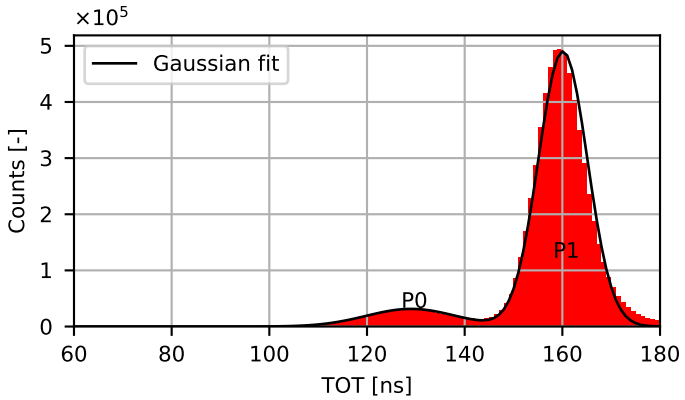
Parameter	Value
μ_0 [ns]	98
σ_0 [ns]	12
μ_1 [ns]	140.0
σ_1 [ns]	9.2
S [-]	3.88

Figure 2.32: ^{55}Fe cumulative spectrum for all 32 channels without baseline equalisation (left) and Gaussian fit parameters for both peaks P0 and P1 (right). Separation power S of the peaks was calculated according to the formula 2.5 [10].



Parameter	Value
μ_0 [ns]	124.8
σ_0 [ns]	9.4
μ_1 [ns]	157.1
σ_1 [ns]	5.5
S [-]	4.33

Figure 2.33: ^{55}Fe cumulative spectrum for all 32 channels after baseline equalisation (left) and Gaussian fit parameters for both peaks P0 and P1 (right). Separation power S of the peaks was calculated according to the formula 2.5 [10].



Parameter	Value
μ_0 [ns]	129.0
σ_0 [ns]	9.1
μ_1 [ns]	160.1
σ_1 [ns]	5.0
S [-]	4.39

Figure 2.34: ^{55}Fe cumulative spectrum for all 32 channels after baseline equalisation and mannual corrections (left) and Gaussian fit parameters for both peaks P0 and P1 (right). Separation power S of the peaks was calculated according to the formula 2.5.

2.5.4 TOT scan - separation studies

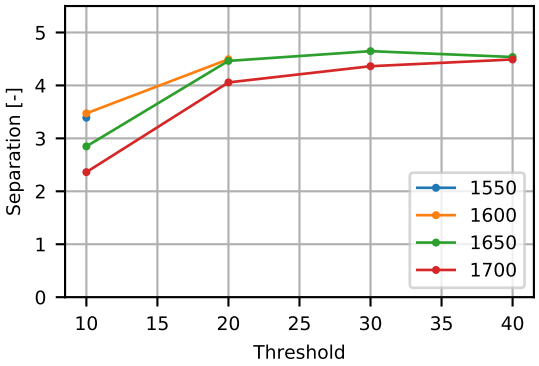
The ^{55}Fe TOT spectra were measured for different HV settings, different threshold settings, and configurations: *1mV20ns*, *2mV20ns* and *4mV20ns*. Configuration combinations are shown in Table 2.8. For not every configuration and setting combination visible in the table, it was possible to collect the spectrum or it was not possible to calculate the separation power. The reason was, for example, a too high threshold setting for a lower gain configuration, which caused the escape peak to be not visible or too low HV and gain combination.

Table 2.8: Setting combinations used in the TOT scan separation studies with ^{55}Fe source.

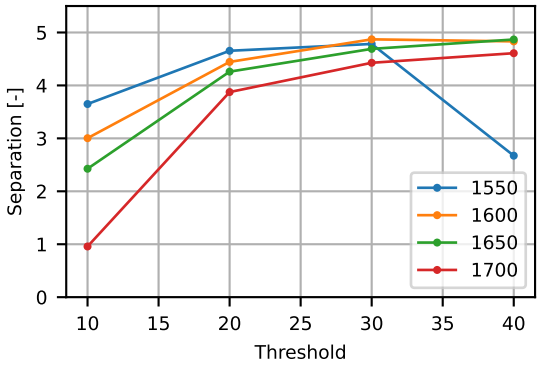
Configuration	HV [V]	Threshold [mV]
$1mV20ns$	1550, 1600, 1650, 1700	10, 20, 30, 40
$2mV20ns$	1550, 1600, 1650, 1700	10, 20, 30, 40
$4mV20ns$	1550, 1600, 1650, 1700	20, 30, 40

For each scan, the separation power was calculated as (2.5). The separation power as a function of threshold for *1mV20ns*, *2mV20ns* and *4mV20ns* configurations and for different HV settings is shown in Figure 2.35. The lower the threshold is set, the closer the threshold is to the baseline level, which may cause that noise exceeds the threshold level and worsens the standard deviation of TOT spectra. The effect can be seen in Figure 2.36. The increase in separation power with increasing threshold is observed until the maximum is obtained, as, for example, for *1mV20ns* at HV = 1650 V which has the maximum for Th = 30 mV, and then S slightly decreases. It is caused by the worsening of the standard deviation of the escape peak and, finally, the loss of it, which can be observed in Figure 2.37 for *2mV20ns* configuration at HV = 1550 V (for threshold 40 mV the escape peak is not visible). This way for lower gain settings and higher thresholds, part of the spectrum can be lost (for lower energies).

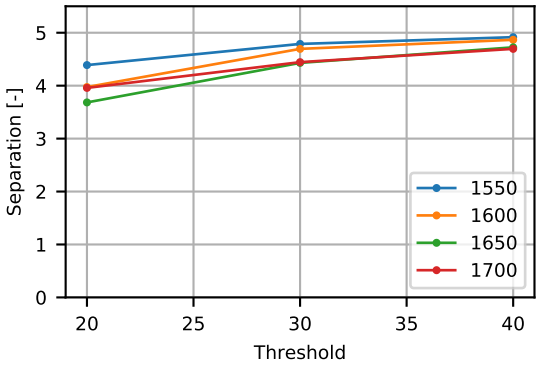
When the results are compared for different HV within one configuration and threshold setting, it is seen that a larger separation is usually obtained for the lower HV. The results are slightly better for the *2mV20ns* and *4mV20ns* configurations. The maximum separation power was obtained for the $4mV20ns$ configuration at HV = 1550 V and for Th = 40 mV. It is 20% lower than the maximum separation power obtained in the threshold scan.



(a) *1mV20ns*.

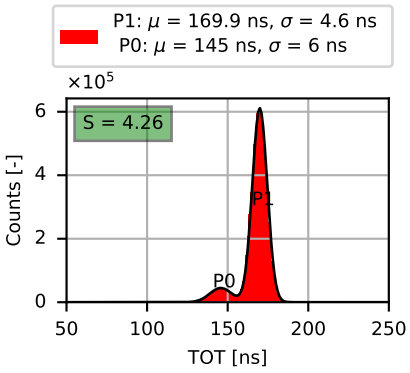


(b) *2mV20ns*.

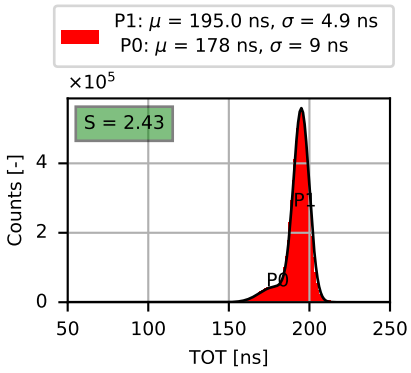


(c) *4mV20ns*.

Figure 2.35: Separation power in function of threshold setting for *1mV20ns*, *2mV20ns* and *4mV20ns* configurations and different HV settings. Separation power calculated according to the formula (2.5).



(a) *2mV20ns* configuration, Th = 20 mV.



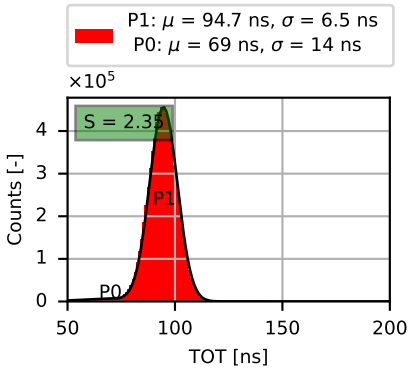
(b) *2mV20ns* configuration, Th = 10 mV.

Figure 2.36: ^{55}Fe cumulative TOT spectra for all 32 channels for *2mV20ns* configuration and two different threshold settings (at HV = 1650 V) with Gaussian fit parameters (for P0 and P1). Separation power S calculated according to the formula (2.5).

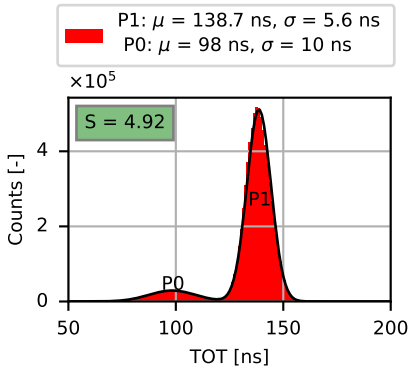
Since the separation power results for the *2mV20ns* and *4mV20ns* configurations were slightly better than for the *1mV20ns* configuration, a more detailed comparison of them was made. The spectra for these configurations at HV = 1550 V are presented in Figure 2.37. Similar separation power can be achieved using one of these configurations. When the obtained results are compared, it can be concluded that the better separation power is achieved for lower HV and larger threshold settings.

However, taking into account the spatial resolution of the straws and the detection performance, which was verified in [33], threshold level, and HV directly affect TOA, causes that resolution and performance to worsen with increasing threshold level and decreasing HV. Higher threshold settings and lower HV can cause the primary electron clusters to not reach the threshold level and to not be registered by the detector.

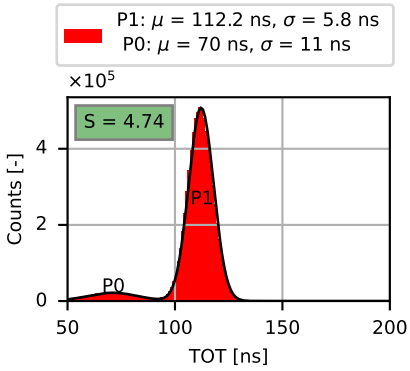
Taking into account all the above arguments, the compromise needs to be found. The lowest possible threshold level should be chosen where the electronic noise is not visible by the system. The lowest possible HV should also be chosen to reduce the ageing effect, but to keep the detection performance at a reasonable level (97%). However, the chosen configuration might not be efficient enough for separation of protons and charge pions and kaons in the experiment. In that case, additional optimisation of settings will be required, for example, increase of threshold level or decrease of HV.



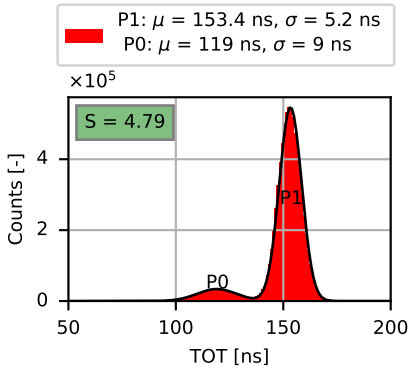
(a) *2mV20ns* configuration, Th = 40 mV.



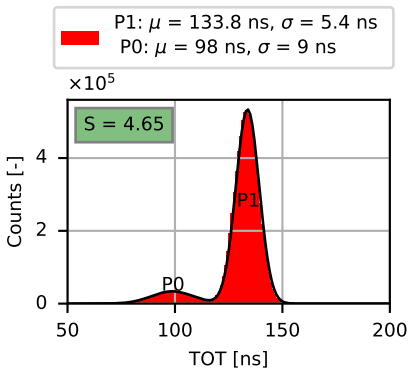
(b) *4mV20ns* configuration, Th = 40 mV.



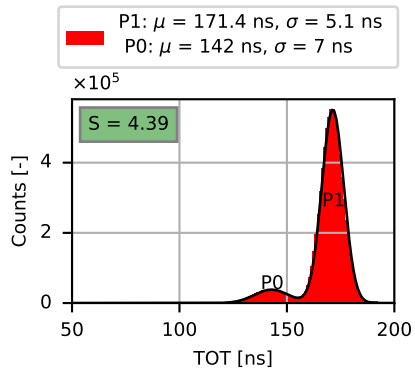
(c) *2mV20ns* configuration, Th = 30 mV.



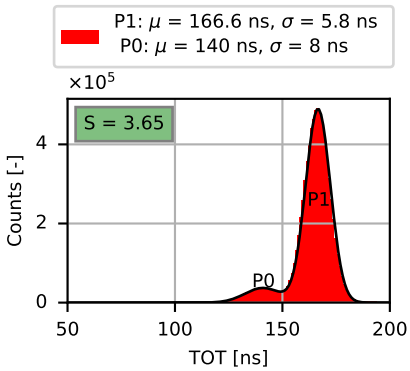
(d) *4mV20ns* configuration, Th = 30 mV.



(e) *2mV20ns* configuration, Th = 20 mV.



(f) *4mV20ns* configuration, Th = 20 mV.



(g) *2mV20ns* configuration, Th = 10 mV.

Figure 2.37: ^{55}Fe cumulative TOT spectra for all 32 channels for *2mV20ns* and *4mV20ns* configurations and different threshold settings (at HV = 1550 V) with Gaussian fit parameters (for P0 and P1). Separation power S calculated according to the formula (2.5).

2.6 HADES beamtime detector monitoring

From January to March 2022, there was a beamtime at the GSI facility and the upgraded HADES was working with the entire Forward Detector part (as described in more detail in Section 1.2). During this time, the shifts on monitoring the system were required. The Data Acquisition (DAQ) operator is a person who monitors the entire detector system and controls it in case of issues or standard beamtime procedures. The tactical overview of the entire system is presented in Figure 2.38. Every important part of the detector is monitored there, and in case of issues, the colour is changed from green to yellow, and in the critical case to red. The HV of STS is monitored there (second column, second row from bottom).

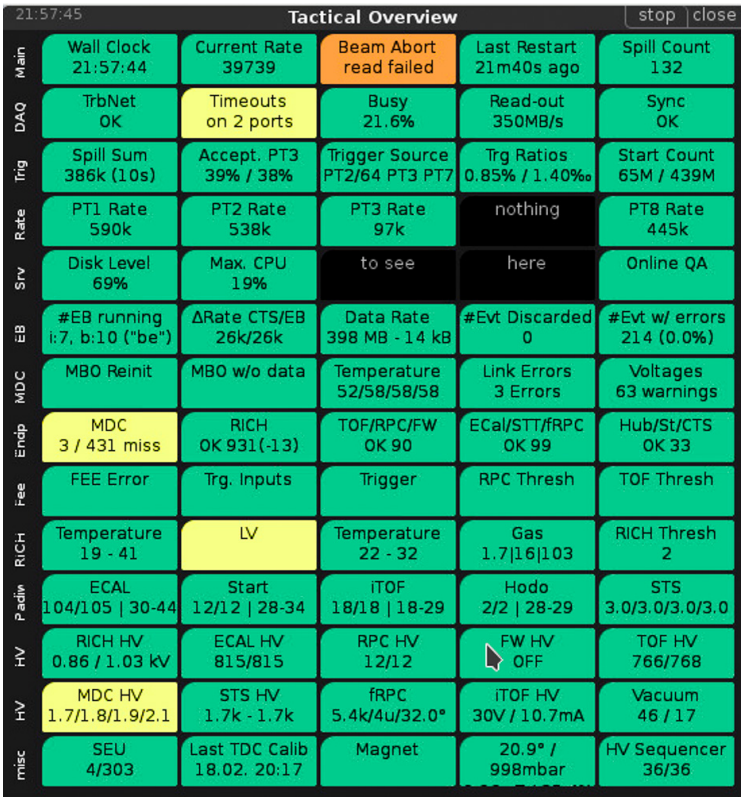


Figure 2.38: Screenshot of HADES tactical overview of whole detector system. In case of issues, the colour of the box is changed from green to yellow, and in the critical case to red. The HV of STS is monitored there (second column, second row from bottom) [in courtesy of HADES collaboration].

During the HADES beamtime, the STS worked with the following settings:

- Straws:
  - 90% Ar + 10% CO_2 gas mixture,
  - Pressure (absolute): 2 bar,
  - HV: 1700 V (gas gain about $2 \cdot 10^4$),
- PASTTRECs:
  - Configuration: *4mV20ns* (4 mV/fC gain and 20 ns peaking time),
  - Threshold: 10 mV (STS1), 20 mV (STS2),
  - Baselines were equalised by the baseline scan procedure before beamtime (then, no change in settings was required) [in courtesy of HADES collaboration].

Due to the fact that it was one of the first beams of the STS detector, it required an additional person to monitor only this part. It allowed to collect more information about the operation of STS and to improve the system. Furthermore, in case of any unexpected problem, action could be taken immediately.

Several parameters were monitored and displayed in the windows. The first (Figure 2.39) was to monitor the high-voltage and gas system. In the top of the Figure 2.39 there is a Gas System Control window. The gas ratio $Ar : CO_2$ is 9:1, therefore, the Ar flow (top left corner) should be around 9 times larger than the CO_2 flow (below Ar). The figure presents the case without beam, so the values are not fully correct. The pressure of the gases in the straws should be 2 bar, and the output flow around 200 ml/min. Pressure and flow were monitored separately for STS1 (top) and STS2 (bottom). In the bottom part, there is the High Voltage Control window. The nominal High Voltage is equal to 1700 V. In case of no beam, it should be set to stand-by mode, 100 V. There is also a monitor of high-voltage currents. Each STS part has 4 layers (which was described in detail in Section 1.4), STS1 layers are supplied in two by one power supply, and in STS2 each layer has its own power supply, therefore the current consumption is slightly higher for STS1 (green numbers on the left are to monitor, black on the right are to set). During beamtime, current consumption was up to 9 μA (STS1) and 8 μA (STS2) between spills, with spikes of up to 15 μA with beam.

In addition to gas system control and high voltage control, there were the time diagrams of the mentioned quantities - Figure 2.40. It allowed to check the gas flow and pressure (top) or supply voltage and currents (bottom) in the last 30-60 minutes.

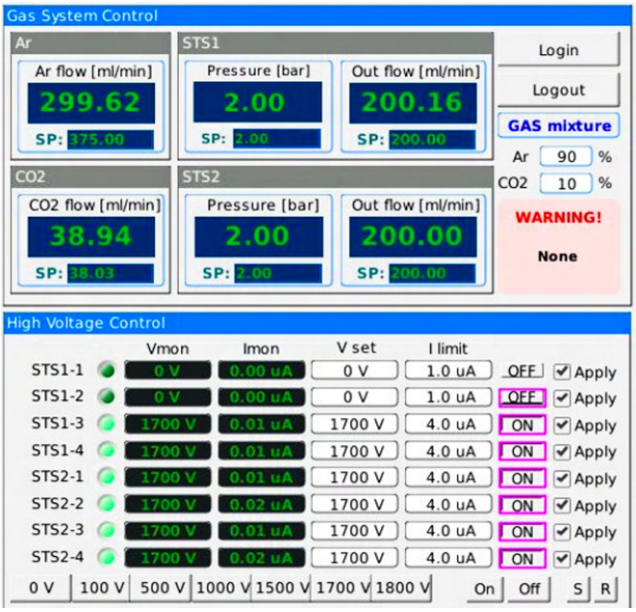


Figure 2.39: Screenshot of STS monitor desktop 1. Gas System Control (top) with gas flow and pressure monitor, and High Voltage Control (bottom) with supply high voltage and current for each part of STS [in courtesy of HADES collaboration].

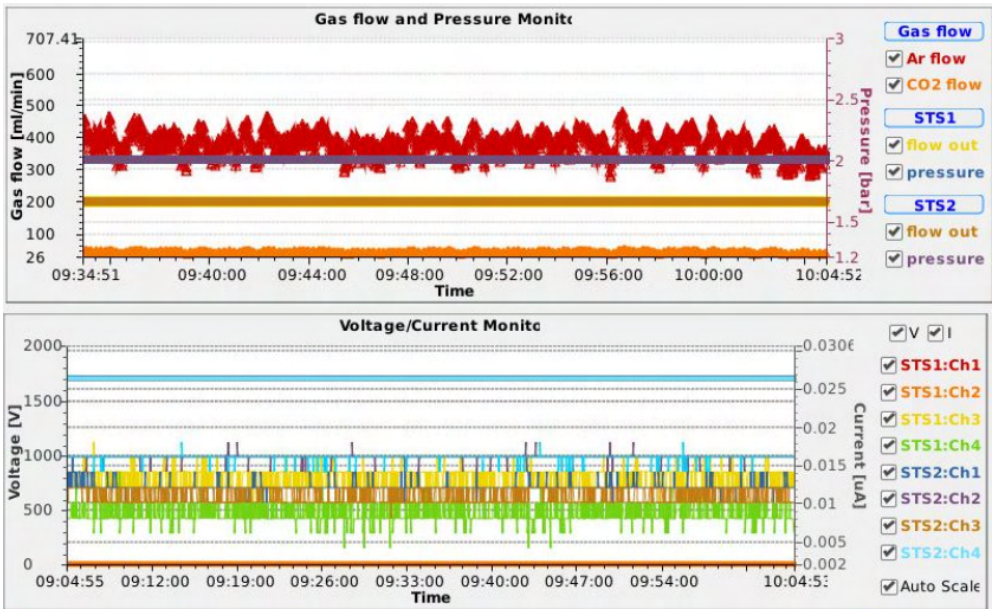


Figure 2.40: Screenshot of STS monitor desktop 1. The time diagrams of the gas flow and pressure (top) or supply voltage and currents (bottom) in the last 30-60 minutes. In the bottom part, the same colours are used for voltage and current monitor. In the presented screenshot, all STS layers have 1700 V and current up to about 15 μA [in courtesy of HADES collaboration].

The next part was to monitor the hit rate of particular channels – Figures 2.41 and 2.42. Each block shown in these figures represents one of the layers of STS – STS1 are the top 4 blocks and STS2 are the bottom 4 blocks. Each small square represents one channel. During beam spills, the hit rates were up to 10^5 (Figure 2.41) and between spills lower than 10^2 (Figure 2.42). There were two dead channels, visible in both figures, in the second and third layers of STS1 (blue ones).

During the first month of beamtime, STS has shown some problems with noisy channels. Between spills, the hit rate on some channels was much higher than 10^2 and a reset and reload of the FEBs threshold values were required. The issue was found to usually occur after restarting the entire DAQ system. Therefore, the script to reset and reload the threshold values was prepared and added to the DAQ restart sequence. Then, in the following days, almost no problems were observed.

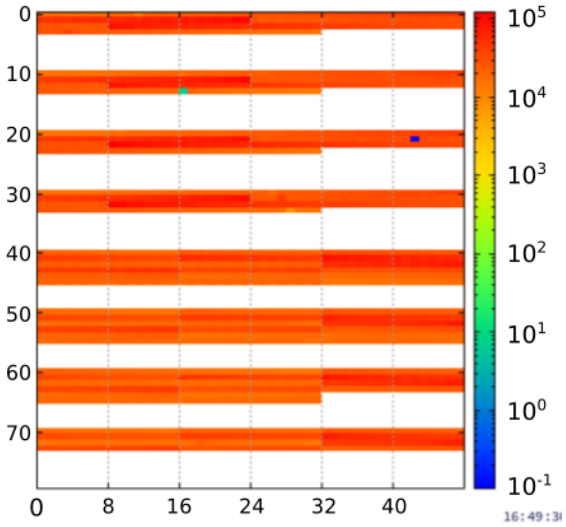


Figure 2.41: Screenshot of STS hit rate with beam (hit rates up to 10^5). Each block represents one of the STS layers, the top 4 blocks STS1 and the bottom 4 blocks STS2 [in courtesy of HADES collaboration].

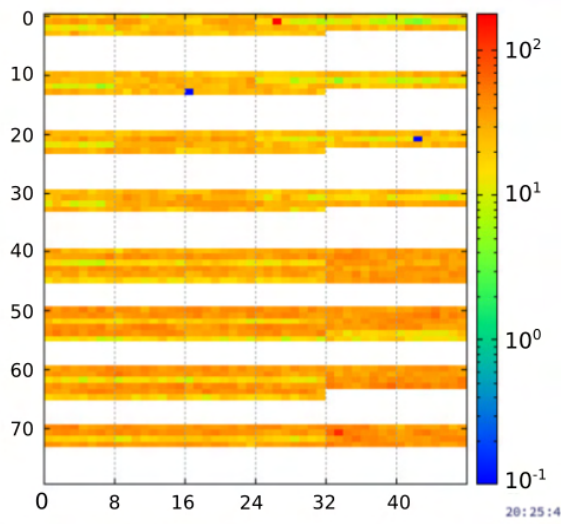


Figure 2.42: Screenshot of STS hit rate between beam spills (hit rates up to 10^2). Each block represents one of the STS layers, the top 4 blocks STS1 and the bottom 4 blocks STS2. Two dead channels (marked blue) in the second and third layers of STS1 [in courtesy of HADES collaboration].

Additionally, data such as raw TOT spectra (Figure 2.43 and 2.44) and drift time spectra (Figure 2.45 and 2.46) were collected continuously and monitored during data taking as part of on-line Quality Assurance (QA) monitor. These windows allowed one to additionally real-time monitor the data collection.

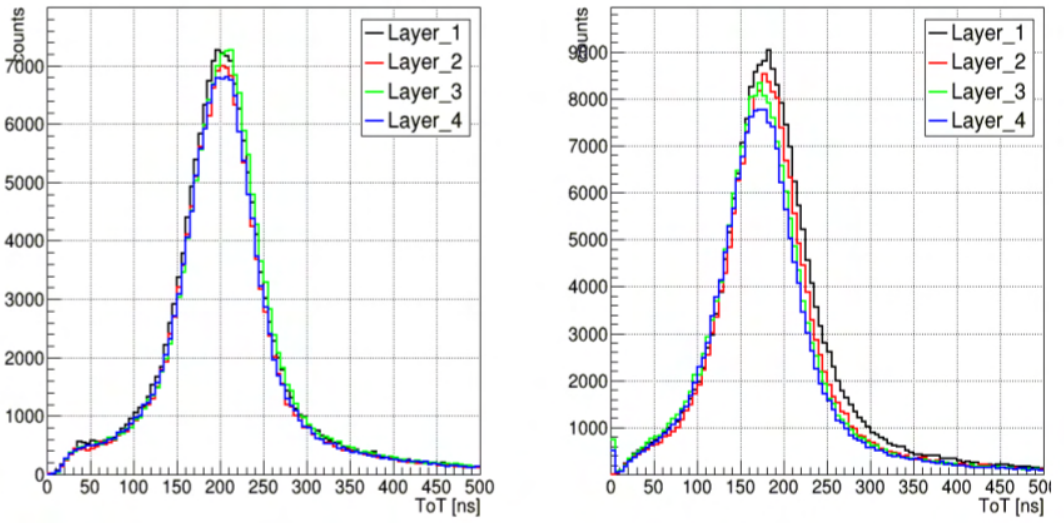
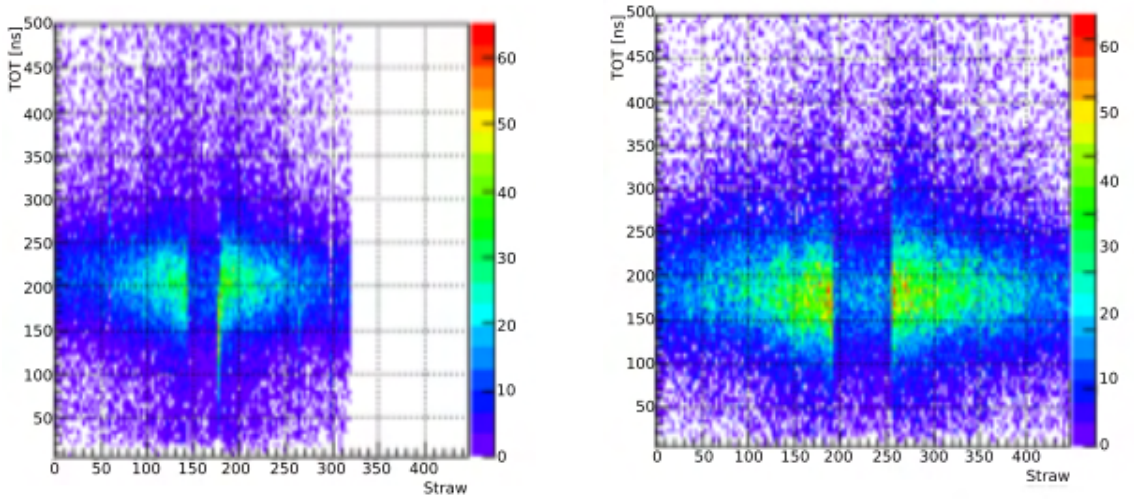


Figure 2.43: Screenshot of cumulative TOT spectra for STS1 layers (left) and STS2 layers(right) observed during HADES beamtime [in courtesy of HADES collaboration].



(a) STS1, layer 1.

(b) STS2, layer 1.

Figure 2.44: Screenshot of 2D spectra of TOT as a function of straw number for STS1 layer 1 (right) and STS2 layer 1 (left) observed during HADES beamtime [in courtesy of HADES collaboration].

Figure 2.43 shows the cumulative TOT spectra for each layer of STS separately (4 layers of STS1 on the left and 4 layers of STS2 on the right). The mean value of TOT for the settings used for PASTTREC and the detector was approximately 200 ns and the distribution width was approximately 200 ns. The aim was to observe any changes in its shape such as a different mean value, wider distribution or more counts of the lower values of TOT (usually below 100 ns) and

whether the spectrum no longer had a Gaussian shape. Figure 2.44 presents the 2D spectra of TOT as a function of the straw number. Each subplot represented one layer; Figure 2.44 shows only one layer for each station: STS1 layer 1 (left) and STS2 layer 1 (right). This view allowed one to observe additionally if no missing group of channels occurred (the smaller number of counts for middle straws is caused by the detector geometry).

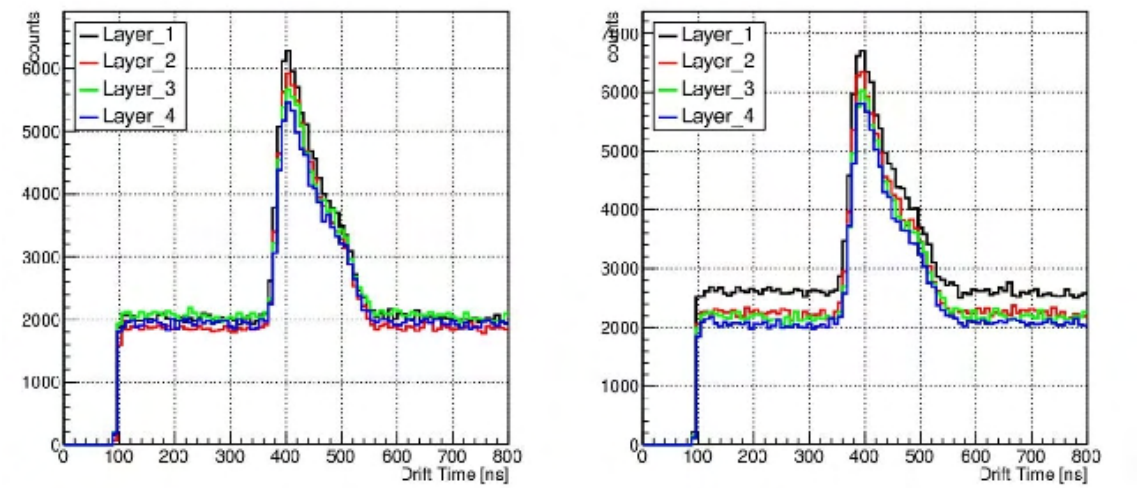
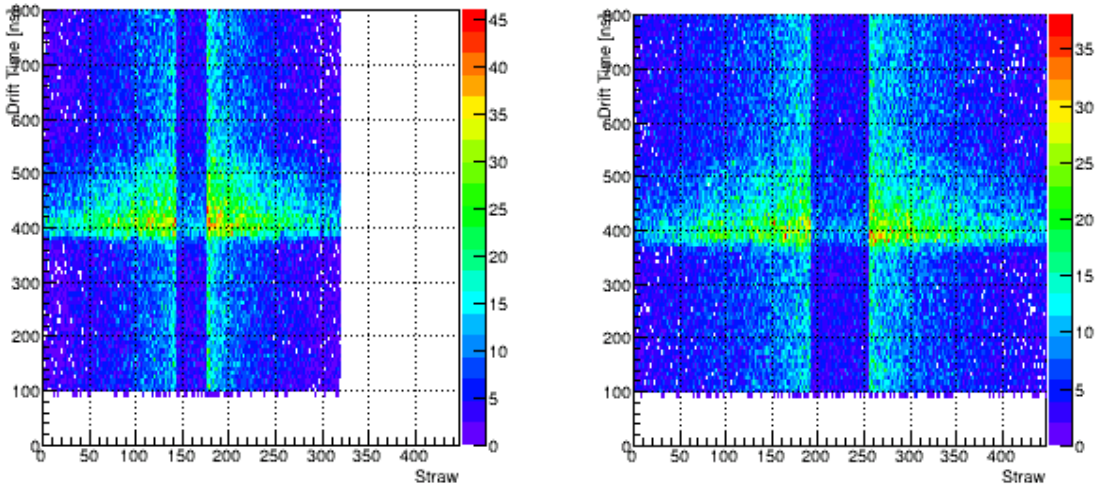


Figure 2.45: Screenshot of STS1 (left) and STS2 (right) drift time spectra observed during HADES beamtime [in courtesy of HADES collaboration].



(a) STS1, layer 1.

(b) STS2, layer 1.

Figure 2.46: Screenshot of 2D spectra of drift time as a function of straw number for STS1 layer 1 (right) and STS2 layer 1 (left) observed during HADES beamtime [in courtesy of HADES collaboration].

Figure 2.45 shows the cumulative drift time distribution for each layer of STS separately (4 layers of STS1 on the left and 4 layers STS2 on the right, analogous to TOT spectra). The drift time is the difference between time of arrival of the signal from straw and reference time stamp. All

layers had offset caused by the noise (in the exemplary screenshot about 2000 counts). The drift time started from about 390 ns and had maximum number of counts at 400 ns, which was arbitrary value caused by delays in the DAQ system. The longest time that electron needs to drift to the anode is about 180 ns. Therefore, the maximum drift time had to be below 200 ns. The Figure 2.46 presents the 2D spectra of the drift time as a function of the straw number. Each subplot represented one layer, in the Figure 2.46 only one layer is shown: STS1 layer 1 (left) and STS2 layer 1 (right). This view allowed one to observe if no missing group of channels occurred (the smaller number of counts for middle straws is caused by the detector geometry, analogous to TOT spectra).

In case of any distortion or missing group of channels, caused usually by aforementioned noisy channels, action had to be taken (usually, the reset of the thresholds was enough).

Chapter 3

Development of Dedicated ASICs for Future Experiments

The ASICs are one of the most important part of modern particle physics detectors. Therefore, the second part of this thesis is focused on the research and development of dedicated readout circuits, containing also the study of ASICs to improve their performance in detector systems.

One of the most important features of current particle physics experiments is the measurement of the particle's amplitude, which is usually done with ADCs. The AGH University group has developed very well working 10-bit Successive Approximation Register (SAR) ADC at 130 nm CMOS technology [1, 2] which is described in detail in 3.1. The ADC is used in a few projects, including the High Granularity Calorimeter Read-Out Circuit (HGCROC) ASIC in the CMS experiment. The HGCROC ASIC was designed due to the fact that the LHC is entering a new High Luminosity (HL) phase [35] that will allow more detailed studies in high-energy particle physics, determined especially by the discovery of the Higgs boson, but also observation of new rare phenomena. To replace existing endgap calorimeters, in the HL phase the CMS collaboration [36] is designing High Granularity Calorimeter (HGCAL) [37]. The new calorimetry system has to deal with two main issues: high radiation and high intensity of new data, causing the time pile-up. In response to these challenges, a dedicated readout ASIC HGCROC was developed [12] by the OMEGA group from Ecole Polytechnique in collaboration with the CEA-IRFU Institute in Saclay, CNRS from Paris, CERN and AGH University. The AGH University group was responsible for the aforementioned 10-bit SAR ADC design. The measurements of ADC in the HGCROC prototype are described in Section 3.2.

Nowadays, in the time of constant particle physics development, not only the information about particle passage is required or the amplitude of the signal provided by ADC, but also the precise time information provided by Time-to-Digital Converter (TDC). Therefore, the development of TDC prototype was started. Since the very well-working 10-bit SAR ADC was already developed by the AGH University group (the one mentioned above), the TDC architecture with analogue interpolators was chosen. The simplest topology contains two parts, Time-to-Analog Converter (TAC) and ADC. The main focus in this work was on the TAC design with slight modifications in ADC that are presented in section 3.1.

3.1 Design of precise Time-to-Digital Converter (TDC)

There are many possible architectures for the Time-to-Digital Converter (TDC). Many modern TDCs use a digital delay line or a ring oscillator [38], but TDC with analogue interpolators was chosen for this project. The basic architecture consists of two main parts, Time-to-Analog Converter (TAC) and Analog-to-Digital Converter (ADC), shown in Figure 3.1. TAC provides a conversion of the time difference (for example, between the particle and the reference signal) into the amplitude V_{out} which is then digitised by ADC. The basic TAC design contains a capacitor C, a constant current source I, and a start-stop logic. At first, the capacitor is reset to the common mode voltage (usually 0 V) by closing S_R. In idle mode, the current source is disconnected from the capacitor and the current flows to the ground (S_1 open, S_2 closed). When the start signal arrives (t_{start}), the current source is switched to the capacitor (S_1 closed, S_2 open), and the capacitor is charged by constant current until the stop signal arrives (t_{stop}) and turns off the S_1 (turns on S_2). The voltage amplitude on the capacitor has the following relation to time:

$$V_{out} = \frac{I}{C}(t_{stop} - t_{start}) \tag{3.1}$$

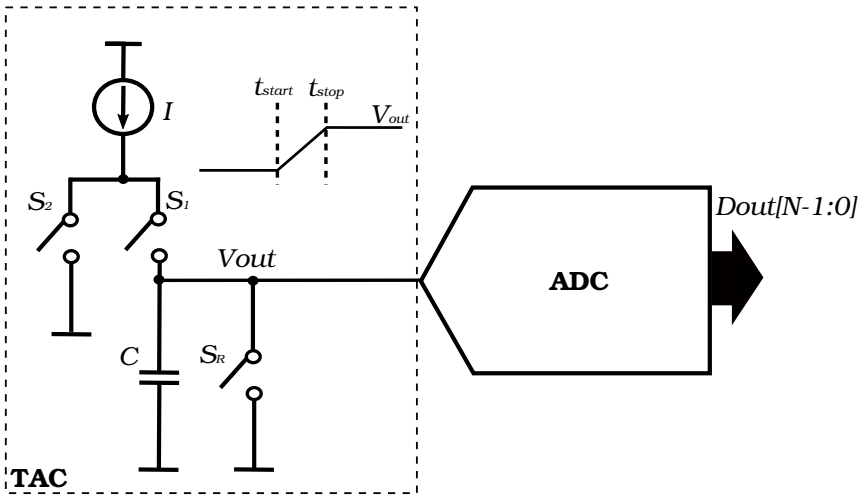


Figure 3.1: Basic block diagram of TDC with analogue interpolators containing two main parts, TAC and ADC.

The 10-bit SAR ADC, designed by the AGH University group, is an ultra-low power and fast differential ADC that works asynchronously. It consumes around 700 μW power when operating at a 40 MHz frequency. It offers excellent dynamic performance (Signal-to-Noise and Distortion Ratio (SINAD) ≈ 58dB, Effective Number of Bits (ENOB) ≈ 9.5 at 40 MS/s) and static performance (Integral Non-Linearity (INL) $<$ 0.5 LSB, DNL $<$ 0.5 LSB) [1]. Due to these advantages, it was chosen for the TDC design and the main focus of this work is on the design of TAC.

The chosen ADC architecture imposed some additional requirements on the design of TAC. The SAR ADC design was made in 130 nm CMOS technology and is differential. It already contains capacitors in its architecture ($C_{total} \approx 2.4$ pF of internal capacitive DAC) and, in order to simplify the design, they were used as capacitors that convert time to amplitude (C from the basic

TAC design in Figure 3.1). Therefore, TAC had to provide only complete start-stop logic and two separate branches with current sources, one to charge and the other to discharge the capacitors in a single cycle. The TAC has two input signals, *InU* and *InD*. Furthermore, the used SAR ADC does not provide a reset of the capacitors to the common mode voltage ($V_{CM} = \frac{1}{2}V_{DD} \approx 600\,mV$), hence this block also had to be added to TAC. The goal of the TDC design was to allow configurable time resolution with a minimum resolution at the level of tens to more than 100 ps. This requirement causes the use of currents of about 200-20 μA. Currently, the TDC is developed as the Research and Development (R&D) block to be added in the future as one of the key blocks of the complex ASIC.

The TDC operates in U2 coding; hence, the Most Significant Bit (MSB) corresponds to the sign value; the output range for 10-bit is -512-511. When *InU* arrives first, the output values are positive; in the opposite case, when the *InD* signal arrives first, the values are negative, the code 0 corresponds to the time difference of 0 s between the signals.

3.1.1 Time-to-Analog Converter (TAC)

Taking into account the requirements mentioned above, the TAC architecture was selected through topologies based on TDC designs with SAR ADC [39, 40]. The chosen architecture contains two main blocks: Phase Frequency Detector (PFD) and Charge Pump (CP) with an additional Voltage Common Mode (VCM) Reset block (Figure 3.2).

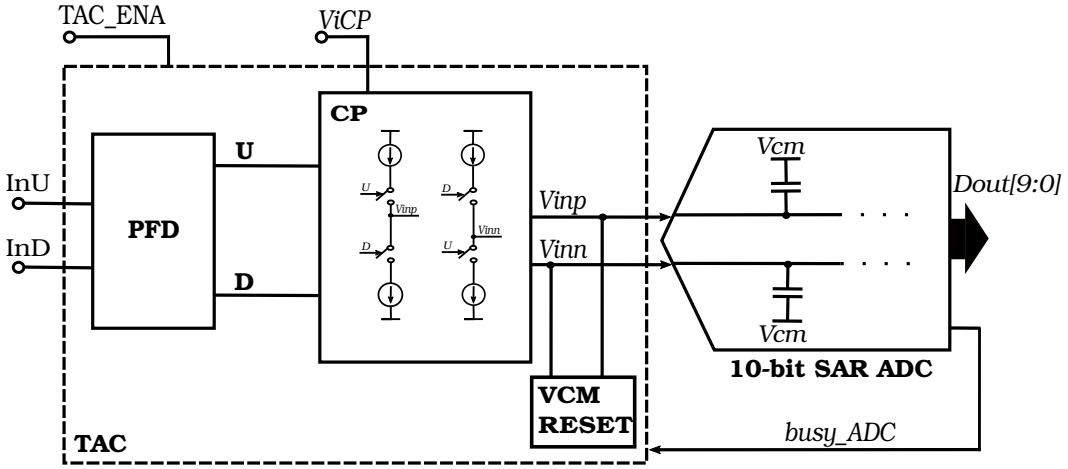


Figure 3.2: Basic block diagram of prototype TAC with connected 10-bit SAR ADC. The TAC contains PFD, CP and VCM Reset block.

The PFD detects the time difference between the input signals *InU* and *InD* and then produces the *U* and *D* signals. The CP contains two branches of current sources that are driven by the *U* and *D* signals from PFD and are responsible for charging or discharging the ADC capacitors through *Vinp*/*Vinn*. The charging current is determined by the bias voltage *ViCP*. The VCM Reset block discharges the capacitors to V_{CM} when ADC ends the conversion and disconnects them before the arrival of next *InU*/*InD*. To communicate about its conversion, ADC sends a *busy_ADC* signal to TAC. The signal is high during the ADC conversion and goes low after finishing it, giving the information to TAC that the reset to V_{CM} can be performed and the next signals can be accepted.

Furthermore, TAC consists of the *TAC_ENA* signal that allows TDC to operate. The state 0 disables TDC and sets it to default mode: Signals cannot be processed; *Vinp* and *Vinn* are reset to V_{CM}. The time diagram of the TDC operation is presented in Figure 3.3.

When the difference between the input signals of PFD is very small, the PFD may fail to detect this difference, which is called the dead zone effect. To remove this effect, the T_{ON} delay is added (to the *U*/*D* signals) during which both sources are connected to *Vinp*/*Vinn*. However, during T_{ON}, voltage noise accumulates in the capacitors, so it must be reduced as much as possible.

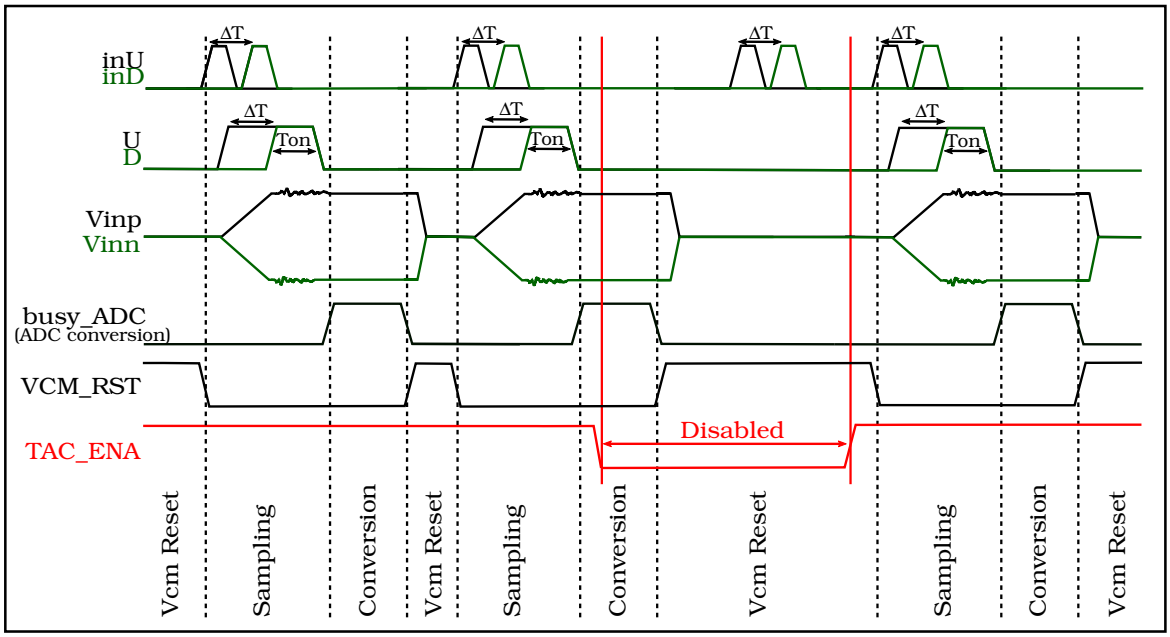


Figure 3.3: Time diagram of TDC operation with the most important signals.

The TAC uses three 7-bit DACs to control the bias currents in the CP block. *ViCP* sets the bias voltage of the current sources in CP to provide an output current in the range of 0-250 μA. The time resolution obtained as a function of the ViCP DAC code is presented in Figure 3.4.

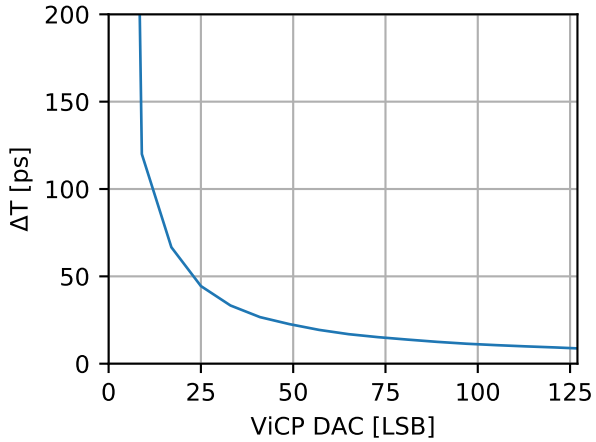


Figure 3.4: Time resolution ΔT as a function of the ViCP DAC code.

All blocks are described in more detail in the following subsections. In all of them, the critical part was the layout design. Therefore, parameter optimisation and simulation were done iteratively together with layout.

Phase Frequency Detector (PFD)

The PFD circuit detects the difference in phase and frequency of the two input signals *InU* and *InD*. In this application, it is used to detect the time difference between the input signals. Its architecture is presented in Figure 3.5. The standard architecture contains two flip-flops that operate on the rising edge (F2-F3) and an AND gate in the feedback to reset them with the *and* signal. As the output, the *U* /*D* and inverted $\overline{U}$/$\overline{D}$ signals are generated which then drive the switches in the CP block. This standard topology was enhanced with additional logic.

The first two flip-flops (F0-F1) respond to the rising edges of *InU*/*InD* signals and any other signals are not accepted until the reset is triggered by the falling edge of *busy_ADC* (F4) or *TAC_ENA* in the `0` state. If either of these two cases occur, PFD is reset to default. *Qinup*/*Qindn* are transmitted to the main flip-flops only when *TAC_ENA* is in active mode (state `1`) - see Figure 3.3.

The signals *U*/*D* and $\overline{U}$/$\overline{D}$ are preceded by an increasing size chain of inverters (not shown on the schematic in Figure 3.5) to allow large switches to be driven in the CP block. Furthermore, the *and* signal, delayed by the group of inverters, triggers the ADC *sampling clock* signal to start conversion.

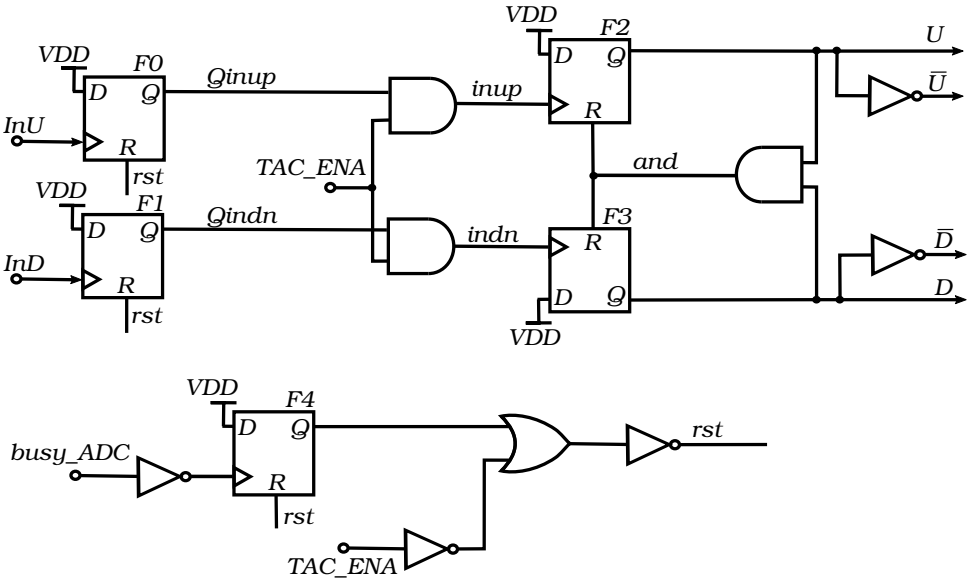


Figure 3.5: Simplified schematic of the PFD.

Charge Pump (CP)

The CP is responsible for converting digital signals from the PFD and generating current to charge or discharge the capacitors in the ADC. It is one of the most important blocks in the TAC architecture. It has to ensure a constant and stable current. Due to the fact that the SAR ADC is differential, the CP has to provide two separate current branches. As in typical CP, each branch has a source and sink type of current mirrors with switches. The CP architecture is presented in Figure 3.6.

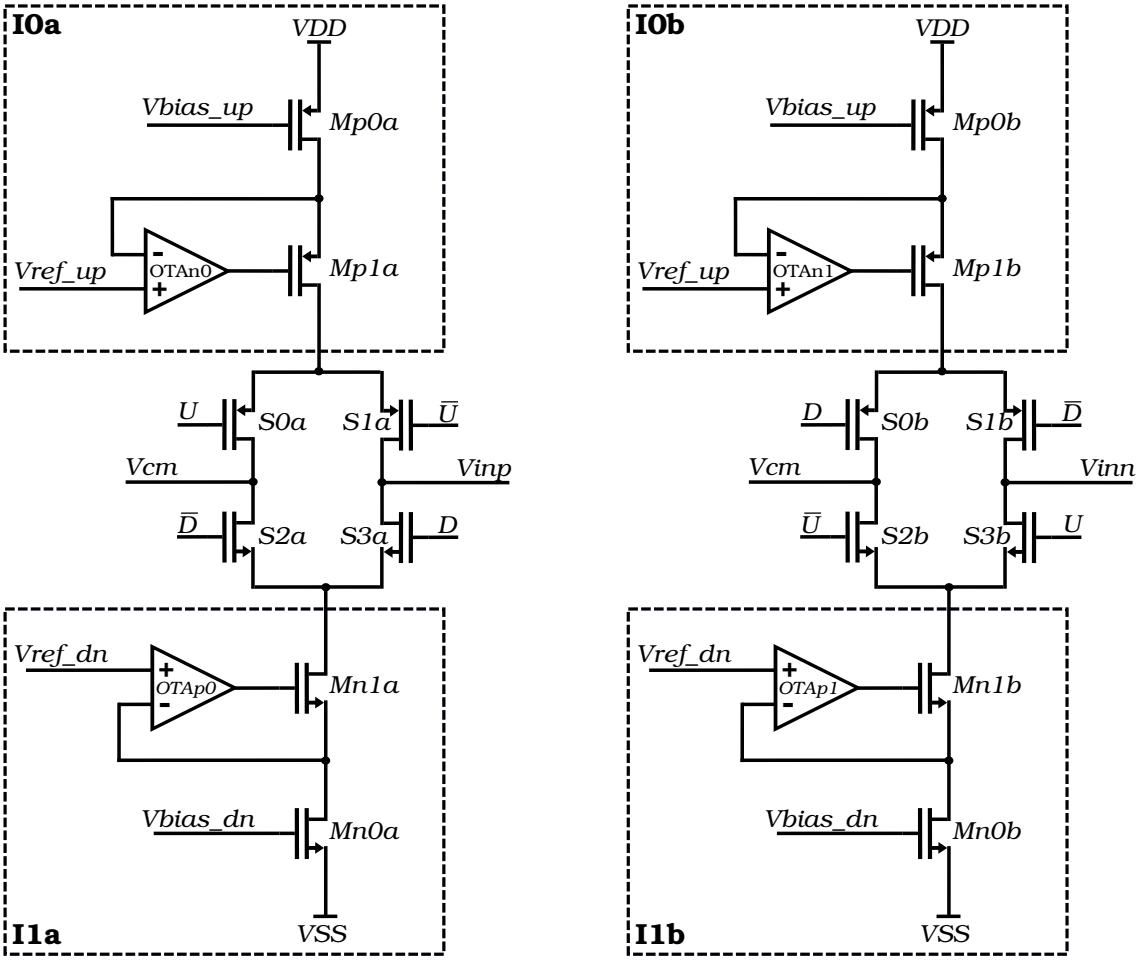


Figure 3.6: Simplified schematic of CP.

Both current branches are the same, the only difference is in the logic of the switches to provide one branch for charging and the other for discharging of ADC capacitors. In the idle mode when there is no signal on the input of TAC, U and D are low, $\overline{U}$ and $\overline{D}$ are high, hence the transistor switches S0a, S2a and S0b, S2b are ON (S1a, S3a and S1b, S3b are OFF) and all current sources ($\mathrm{I_{0a}}$, $\mathrm{I_{1a}}$, $\mathrm{I_{0b}}$, $\mathrm{I_{1b}}$) are connected to V_{CM}. In this way, the current mirrors are constantly in an active state and, after the arrival of the start signal, they are only switched to appropriate nodes to charge or discharge the ADC capacitors.

Assume that the start signal is *InU*. When start signal arrives, $\overline{U}$ goes low, U goes high, the S1a and S3b switches turn on (S0a and S2b turn off) what causes charging of capacitors connected to *VinP* and discharging the ones connected to *Vinn*. After arrival of the stop signal (*InD* in this case), D goes high ($\overline{D}$ goes low) and for short moment (about 200 ps) both current mirrors are connected

to respective ADC inputs (*Vinp* and *Vinn*), which removes the dead-zone effect. Next, everything goes back to idle mode, all current sources are connected to V_{CM}. When *InD* arrives as the start signal, the opposite switching of the current mirrors occurs.

The requirement for current mirrors for this purpose is to provide a stable, constant current flow with high resistance. To ensure the best linearity in the entire range, maximum headroom is necessary for the output signal. For this purpose, the gain-boosted cascode mirror with wide swing and Operational Transconductance Amplifier (OTA) in feedback was chosen [41, 42]. The same considerations are made for both NMOS and PMOS based current mirrors; hence, the following focus will be on the $\mathrm{I_{1a}}$ current mirror. The Mn0a and Mn1a transistors form the cascode output. The Mn0a (as well as Mn0b in the second branch) is biased by *Vbias_dn* which is equivalent to *ViCP*. The use of OTAp0 amplifier, connected in feedback to the gate and the source of Mn1a, provides a high output resistance, approximately: $R_{out} \approx K g_{m1a} r_{d1a} r_{d0a}$, where K is the gain of the amplifier. OTAp0 ensures also that Mn0a V_{DS} remains constant and low. It is controlled by the reference voltage *Vref_dn* (*Vref_up* for OTAn0 and OTAn1) provided by the control DAC. The biasing of Mp0a and Mp0b is carried out by *Vbias_up* and is generated internally in the CP block from *ViCP*. The block diagrams of the designed OTA amplifiers together with their parameters are presented in the Appendix (Figure D.50 and D.51, Table D.20).

VCM Reset

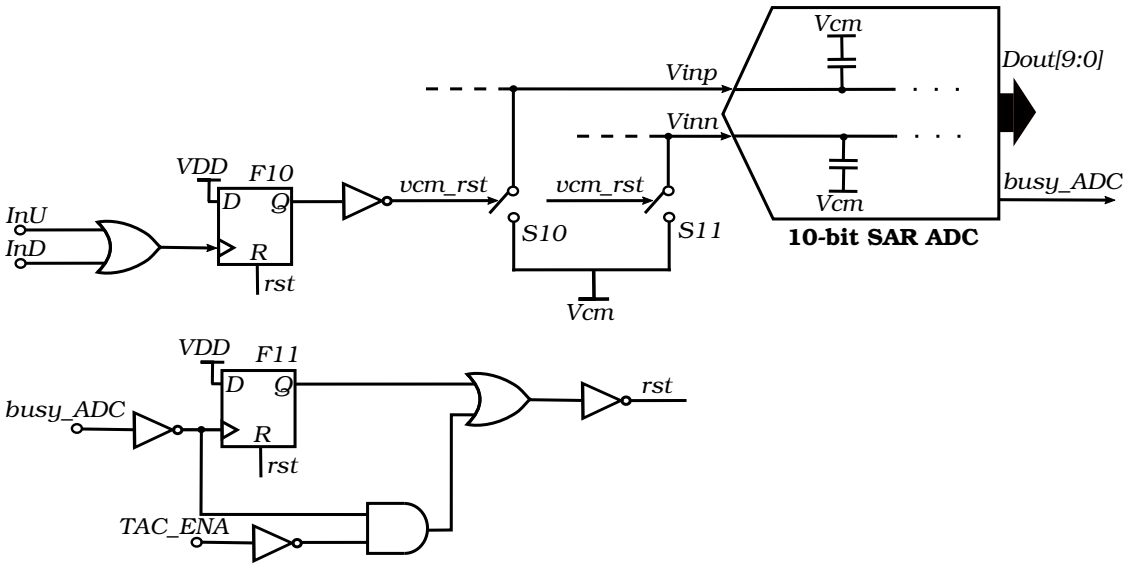


Figure 3.7: Simplified schematic of VCM Reset.

The VCM Reset block consists of two flip-flops triggered by rising edges and few logic gates in its reset logic, block diagram in Figure 3.7. Flip-flop F10 is triggered by the rising edge of the *InU* or *InD* signals. The processing time of the input signal in the PFD and VCM Reset blocks is optimised to ensure that the output switches (S10 and S11) are turned off before charging the capacitors by CP. *Vinp*/*Vinn* are reset to V_{CM} when the falling edge of *busy_ADC* is detected (F11) or *TAC_ENA* is in disabled mode `0`. It is provided that in case *TAC_ENA* is set to `0` while ADC is still converting the data, the reset to V_{CM} occurs after the end of conversion.

The output switches (S10 and S11) have an appropriate size to discharge capacitors SAR ADC to V_{CM} in a reasonable time (about 2.5 ns). The size of the switches causes the problem with charge injection while the *vcm_rst* signal turns them off. Therefore, dummy switches are added to cancel the charge injection (not shown in the block diagram).

TAC layout design

The critical part was the layout of TAC presented in Figure 3.8. On the front, there is the PFD and VCM Reset logic (1). Near them, just behind the PFD block, there are the CP switches (2), to provide the shortest paths for driving signals ($U/\overline{U}$ and $D/\overline{D}$) and to prevent delays or time mismatches. Current sources consist of multiple transistors. To provide the most homogeneous current in the output, the corresponding transistors from both branches are placed mixed up alternately (source type - 3, sink type - 4). Behind them, there are OTA blocks (OTAn - 5, OTAp - 6) and VCM Reset switches (7). The size of the block is $166 \times 100\,\mu\mathrm{m}$.

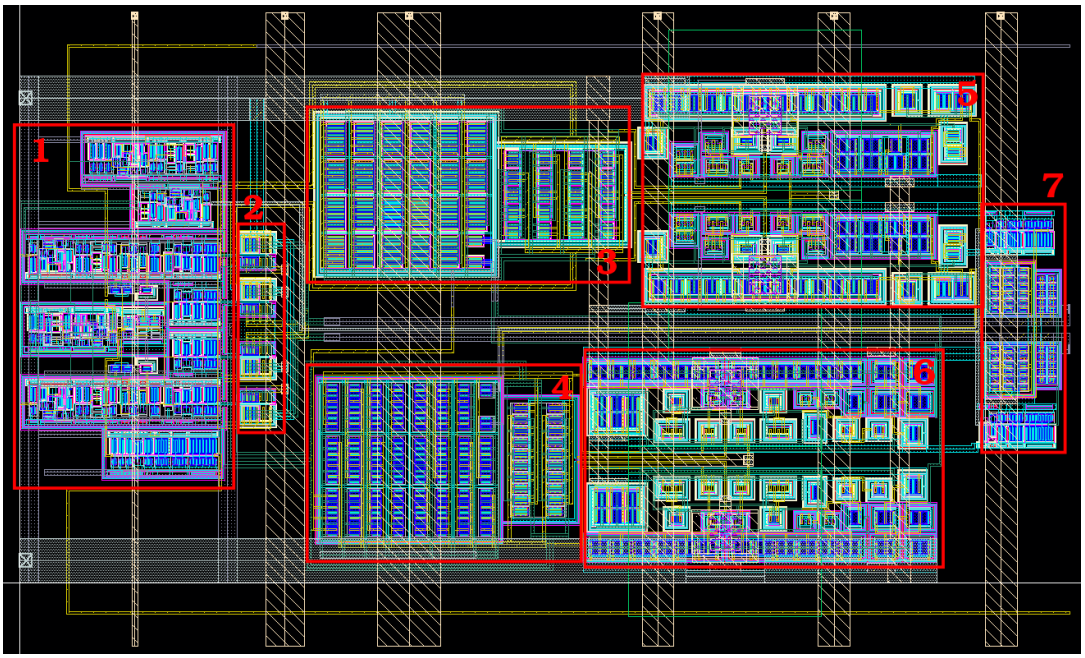


Figure 3.8: Layout of TAC consisting following blocks: (1) PFD with VCM Reset logic, (2) CP output switches, (3) Current PMOS mirrors, (4) Current NMOS mirrors, (5) OTAn, (6) OTAp, (7) VCM Reset switches. TAC width = 100 μm and length = 166 μm

3.1.2 10-bit SAR ADC

The second block of the TDC design is the fast ultra-low power 10-bit Successive Approximation Register (SAR) Analog-to-Digital Converter (ADC), already existing, and used in other applications [1, 2]. The original ADC contained the input bootstrap switch, capacitive DAC, dynamic comparator, and SAR asynchronous dynamic logic - Figure 3.9.

The ADC is based on the SAR architecture with differential input to minimise disturbances. Bootstrap switches are used to provide good linearity. The DAC consists of Metal-Insulator-Metal (MIM) capacitors that are divided into Most Significant Bit (MSB) (6 capacitors) and Least Significant Bit (LSB) (3 capacitors), as shown in the block diagram (Figure 3.9). The Merge Capacitor Switching scheme [43] is implemented in order to decrease power consumption. The fast operation is provided by asynchronous logic, there is no need for clock, which not only speeds up but also reduces power consumption, power is consumed only during the conversion. To start the conversion, only the sampling clock (rising edge) is necessary, which in the present application is generated by the TAC logic described before (signal *and* from PFD block). During conversion, configurable delays are added to give enough time for the DAC voltage to settle, but at the same time to minimise this time as much as possible to ensure the shortest conversion time. They are divided into four groups to control the respective bit conversion: $D9$ for MSB, $D87$ for 8th and 7th bits, $D65$ for 6th and 5th bits, $D40$ for bits from 4 to 0. Their delays can be configured externally from 0 to 7 unit delays. Longer delays are preferred for MSB (larger capacitance). After the last conversion, the logic is reset and ready for the next sample; the *busy_ADC* signal, which informs about the ADC operation, is set to 0. The required V_{REF+}/V_{REF-} reference voltages are set respectively to 1.2 V and 0 V, while $V_{CM} \approx 0.6$ V.

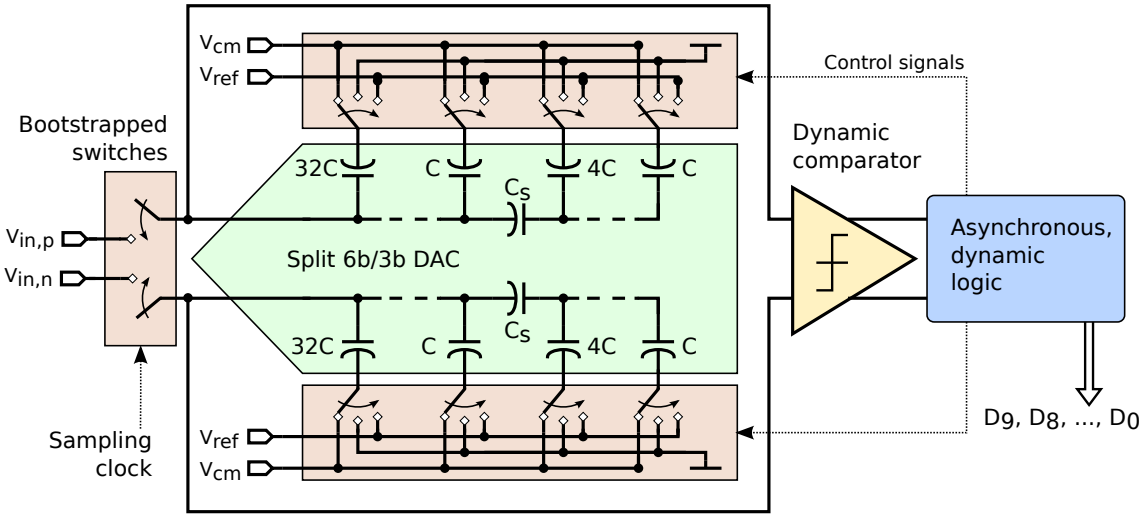


Figure 3.9: Block diagram of 10-bit SAR ADC [11].

The ADC shows excellent proven static (INL $<$ 0.5 LSB, DNL $<$ 0.5 LSB) and dynamic (SINAD ≈ 58dB, ENOB ≈ 9.5 at 40 MS/s) performance. It provides a sampling frequency range from 10 kS/s to 40 MS/s with around 700 μW power consumption at 40 MS/s (power is linearly scaled with sampling rate) [1].

In the present application, few modifications were introduced to the SAR ADC design. The main change was to remove the bootstrap switch since it was no longer necessary - TAC has its own switches in the CP block. Furthermore, some slight changes were made to the output signals to improve signal communication with TAC and synchronise the signals in the multichannel design.

3.1.3 TDC layout

In the end, the two blocks TAC and SAR ADC were merged together, as shown in Figure 3.10. The whole block has 100 μm width and 737 μm length. It is ready to operate on multichannel chip. The decoupling capacitors of ADC are placed above and below its analogue block.

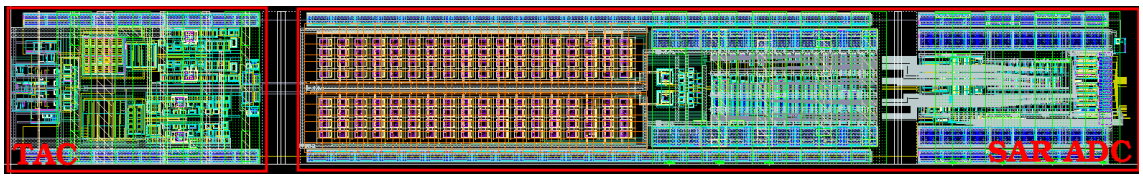


Figure 3.10: Layout of the TDC channel (channel width = 100 μm).

3.1.4 Simulation results

Simulation model and test methodology

The TDC design was done in the CADENCE software using 130 nm CMOS technology. The nominal supply is 1.2 V. The design was simulated using the cell presented in Figure 3.11. The supply was distributed in the same way as in the testing setup. The circuit is supposed to measure very short time differences, so taking into account parasitic parameters, especially inductance ($L_{bond} = 2nH$) and resistance ($R_{bond} = 5m\Omega$) of the bonds was crucial and made the simulation more physically correct. The supply of TAC, the analogue part of ADC and the reference voltages of ADC, as well as the common mode voltages of TAC and ADC were distributed separately adding the inductance and resistance of the corresponding bonds. The digital part of ADC is supplied from the digital part of the chip. The input signals were also connected via the corresponding bond inductance.

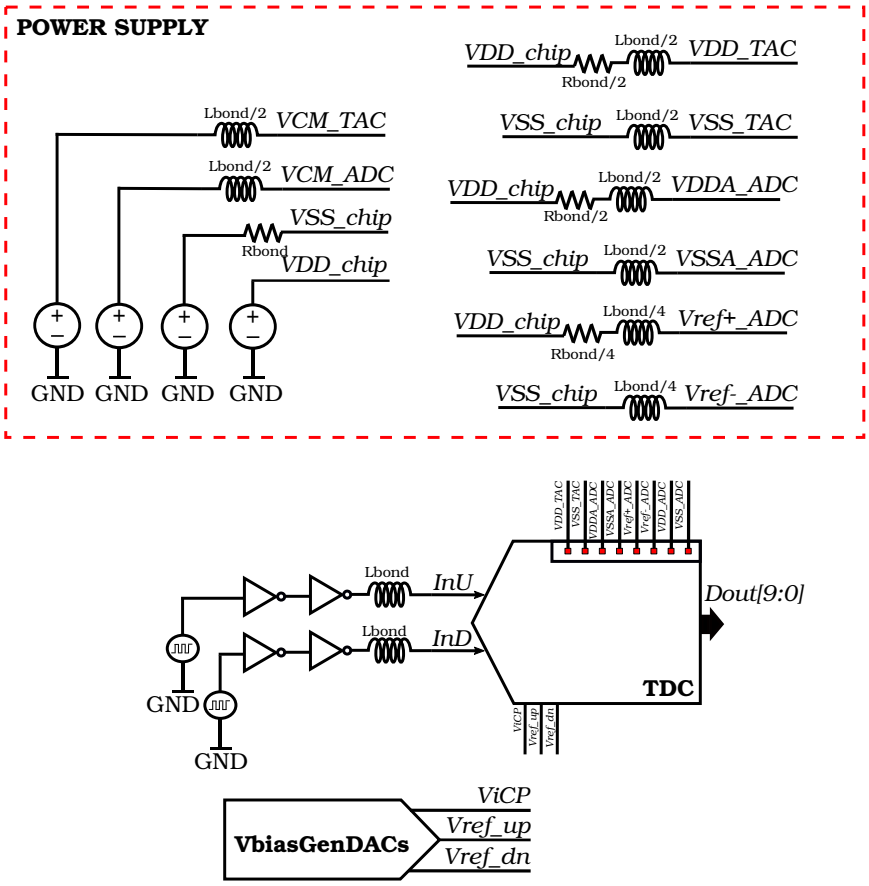


Figure 3.11: Block diagram of the TDC simulation cell.

As input, two square signals with a proper frequency difference were given to create a time ramp. Due to the fact that the post-layout simulation takes a lot of time, the comparison of time difference between input signals was done for 10 ps time resolution. The first case was performed for the time difference step T_{sample} =5 ps, which gives about two samples per ADC code. This time difference was achieved by input signals of frequency $f_1 = 20\,\text{MHz}$ and $f_2 = 19.998\,\text{MHz}$. The second was done for T_{sample} =100 ps time difference between the next samples ($f_1 = 20\,\text{MHz}$,

$f_2 = 19.96$ MHz) what gives a sample every 8 ADC codes. Measurements were made only for the positive code range of TDC (Figure 3.12). Both cases show similar TDC linearity up to 4.43 ns and 376 ADC code. Therefore, in the further linearity studies' simulations the larger time difference between samples (smaller number of samples) was used to fasten the simulation process.

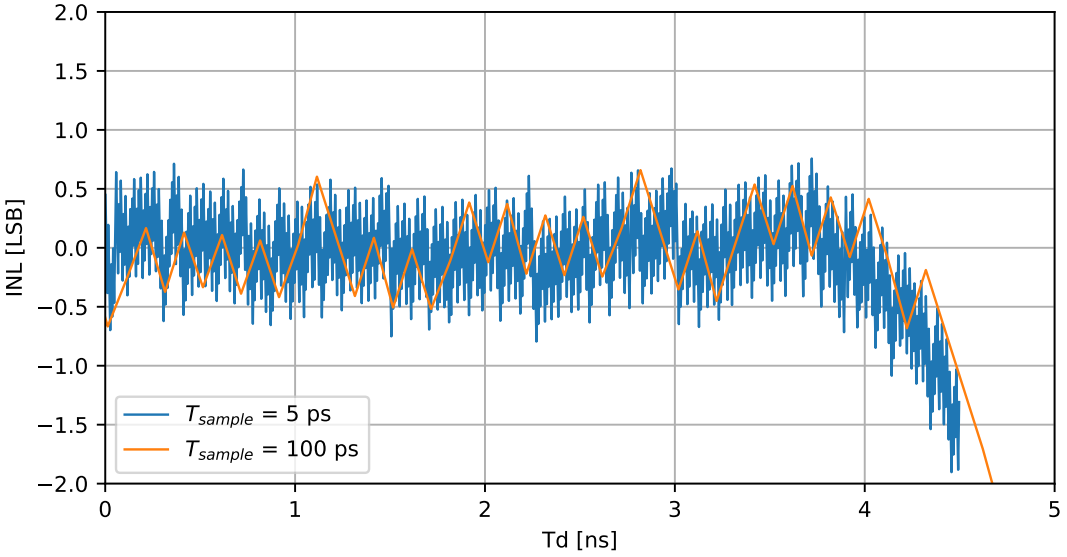


Figure 3.12: INL post-layout simulation results comparing time difference between samples (T_{sample}) for $\Delta T \approx 10$ ps.

In the following simulations for measurements of INL, the input signals were:

- $\Delta T = 10$ ps: $f_1 = 20$ MHz and $f_2 = 19.96$ MHz (T_{sample} =100 ps),
- $\Delta T = 100$ ps: $f_1 = 5$ MHz and $f_2 = 4.975$ MHz (T_{sample} =1 ns).

The simulations for the measurements of DNL were carried out with the appropriate time difference between the input signals to get about 2 samples per ADC code and only for the positive TDC range. The input signals were:

- $\Delta T = 10$ ps: $f_1 = 20$ MHz and $f_2 = 19.998$ MHz (T_{sample} =100 ps),
- $\Delta T = 100$ ps: $f_1 = 5$ MHz and $f_2 = 4.99875$ MHz (T_{sample} =1 ns).

In all simulations, the longest ADC delays were set.

Simulation results

The designed TDC provides configurable time resolution from about 10 to 100 ps (larger can be achieved, but it was not verified). Real-simulated time resolution is about 12 ps (for the 10 ps setting) and 112 ps (for the 100 ps setting).

The power consumption of TAC in post-layout simulation (it should be similar to power consumption obtained in real measurements) is:

- For the 10 ps time resolution is $\sim 820\,\mu$W at 20 MHz signal. About 770 μW comes from CP: $\sim 240\,\mu$W from each branch and $\sim 70\,\mu$W from each OTA. The rest comes from the digital part (PFD and VCM Reset block)
- For the 100 ps time resolution $\sim 130\,\mu$W at 5 MHz signal. About 90 μW comes from CP: $\sim 25\,\mu$W from each branch and $\sim 10\,\mu$W from OTA. The rest comes from digital part (PFD and VCM Reset block)

The post-layout DNL results for time resolution $\Delta T = 10$ ps and $\Delta T = 100$ ps are presented in Figure 3.13. The simulation was carried out only for part of the positive TDC range - up to 380 ADC code for $\Delta T = 10$ ps and 450 ADC code for $\Delta T = 100$ ps. In both cases, almost all DNL values were within ± 0.5 LSB range. No missing codes were observed.

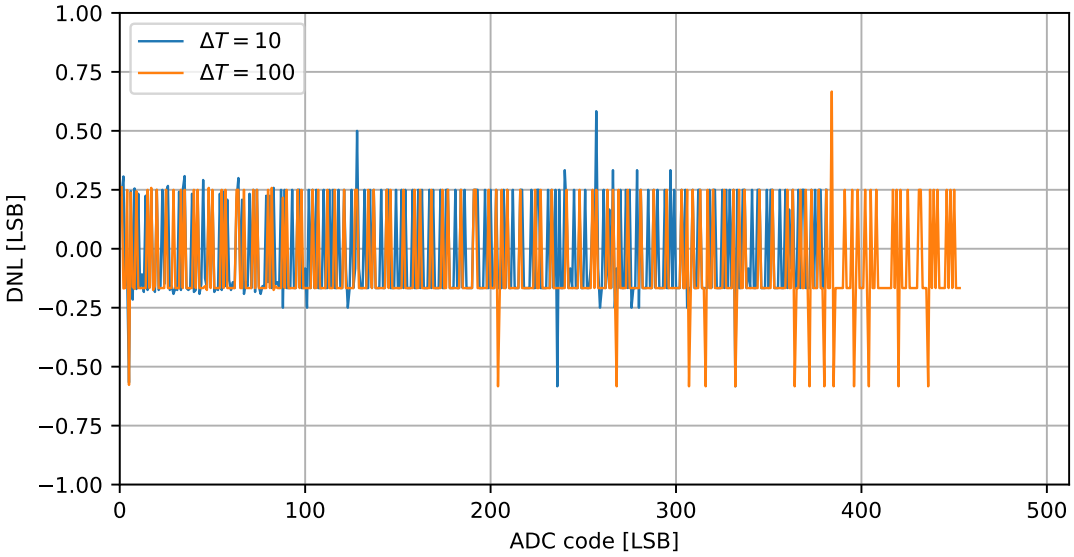


Figure 3.13: DNL post-layout simulation results for time resolution settings $\Delta T = 10$ ps and $\Delta T \approx 100$ ps.

The INL results for the 10 ps resolution are shown in Figure 3.14 for the schematic and post-layout simulation. Schematic simulation gives INL of about ±1.5 LSB in the range of about -4.0 (-357 LSB) ns to 3.82 ns (340 LSB). However, the results for the post-layout simulation show INL within ± 0.5 LSB in the entire range from about -4.29 ns (-365 LSB) to 4.42 ns (375 LSB). The design was optimised in layout, so the performance of TDC is much better in post-layout simulation.

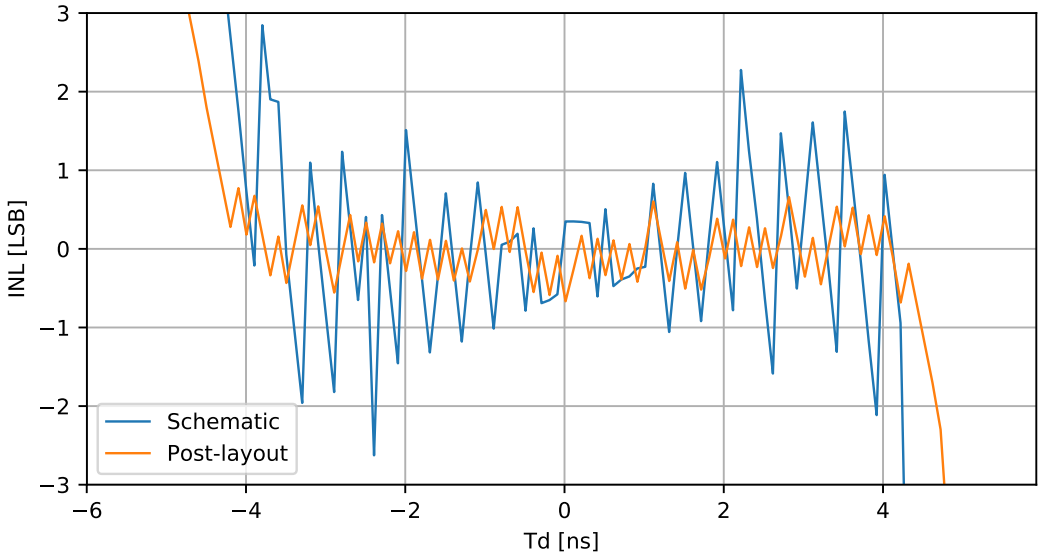


Figure 3.14: INL schematic and post-layout simulation results of $\Delta T = 10$ ps.

The results for the 100 ps time resolution are presented in Figure 3.15. In the schematic simulation, we obtain about ± 4 LSB INL fluctuation in the range of about ± 46 ns (-432 to 445 LSB). In the post-layout simulation, the performance enhances slightly to ± 3 LSB. Moreover, the linear range is wider, approximately ± 53 ns. It gives the ADC linear range from -478 to 483 LSB, which is almost the whole ADC range.

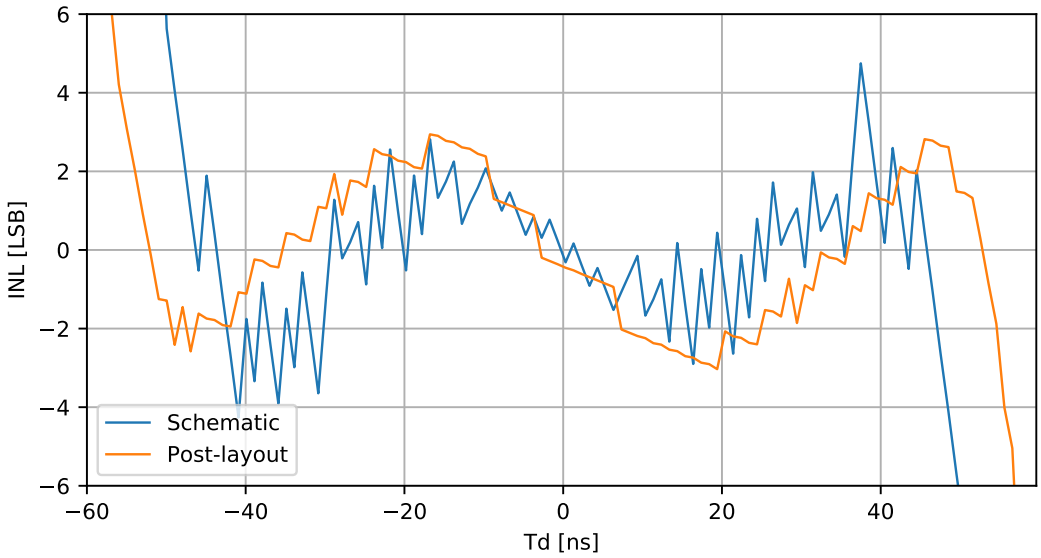


Figure 3.15: INL schematic and post-layout simulation results of $\Delta T \approx 100$ ps.

The performance of TDC was optimised to $\Delta T = 10\,\text{ps}$. This causes the performance for $\Delta T = 100\,\text{ps}$ to be much worse. However, it is seen that the whole range can be wider and that current mirrors can provide more headroom, whereas a smaller current provides less potential drop on the current mirrors. Furthermore, the DNL results were almost within $\pm 0.5\,\text{LSB}$ range and no missing codes were observed for both settings. Due to the fact that the final purpose of the designed prototype ASIC is not yet known, only the prototype ASIC was designed, optimisation was performed to achieve the lowest possible time resolution. If in the final system a larger resolution is required, further optimisation might be done.

Since the simulations for DNL measurement take a lot of time, only INL measurements were done for corners and Monte Carlo simulations.

Corners' simulation results

To verify the operation of TDC under various extreme conditions, the corner simulation is performed. Corners represent the extreme conditions in which ASIC could be found. There were 14 corner settings (C0-C13) in the performed simulations with an additional nominal one (C14). Corners vary in temperature, voltage supply, and transistor models (details in Table 3.1). The circuit has to operate in all corners, if the performance is worse than expected, the conditions may be tuned. Post-layout corner simulation was performed for the setting of a time resolution of 10 ps. The INL results for individual corners are presented in Figure 3.16.

Table 3.1: Parameters of corners' simulation.

Corner	Temp. [°C]	V_{DD} [V]	model	Corner	Temp. [°C]	V_{DD} [V]	model
C0	85	1.14	ss_fs	C8	0	1.14	tt
C1	85	1.14	ss_sf	C9	25	1.2	tt
C2	0	1.14	ss	C10	-20	1.26	ff_fs
C3	85	1.14	ss	C11	0	1.26	ff_fs
C4	0	1.14	ff	C12	-20	1.26	ff_sf
C5	-20	1.26	ff	C13	0	1.26	ff_sf
C6	0	1.26	ff	C14	27	1.2	-
C7	85	1.26	ff				

The TDC operates in all tested corners. Only 5 of 14 corners show significantly worse results of INL than in the nominal setting. However, their INL value is usually not larger than $\pm$ 2 LSB. The only exception is corner C2 where we observe INL of even about $\pm$ 3 LSB. Moreover, corner C7 shows a worse linearity range; however, the charging currents are larger in that case compared to the nominal ones (almost 50 μA larger), which also causes the real-time resolution to be less than 10 ps.

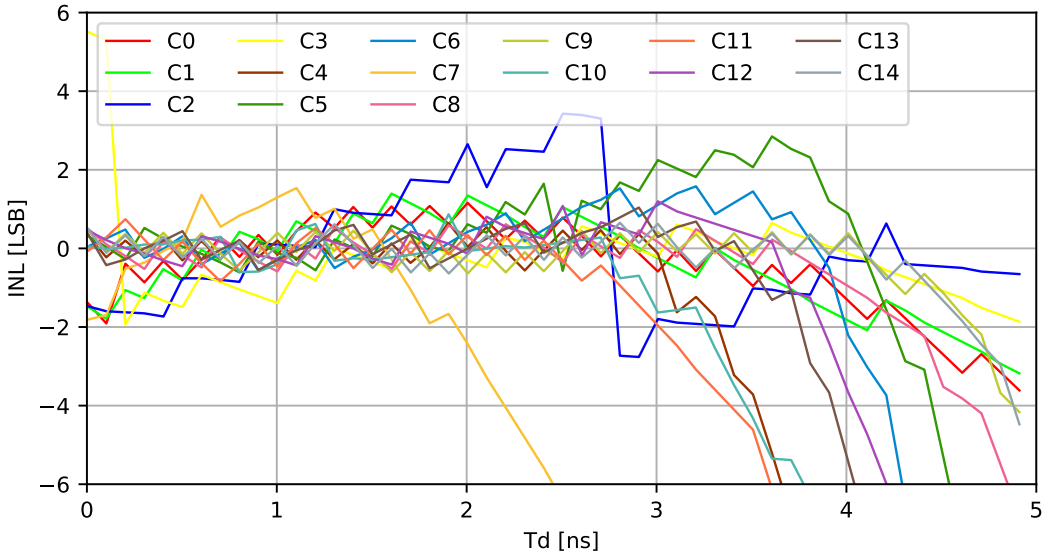


Figure 3.16: Corners' INL post-layout results for $\Delta T = 10$ ps.

The voltage supply and temperature are conditions that can be easily changed. The only parameter that cannot be changed is the model of transistors. Therefore, an additional simulation was performed for different transistor models at the nominal value of the voltage supply 1.2 V and the temperature 25°C - Figure 3.17. The INL results for all of them are within $\pm$ 0.5 LSB range. The difference is in the linear range of the particular model. For models containing fast transistors (*ff, ff_fs, ff_sf*) the range is much smaller (to about 2.3 ns). However, these models cause larger currents that load capacitors; time resolution is smaller, less than 10 ps (the nominal value is about 12 ps in the post-layout simulation).

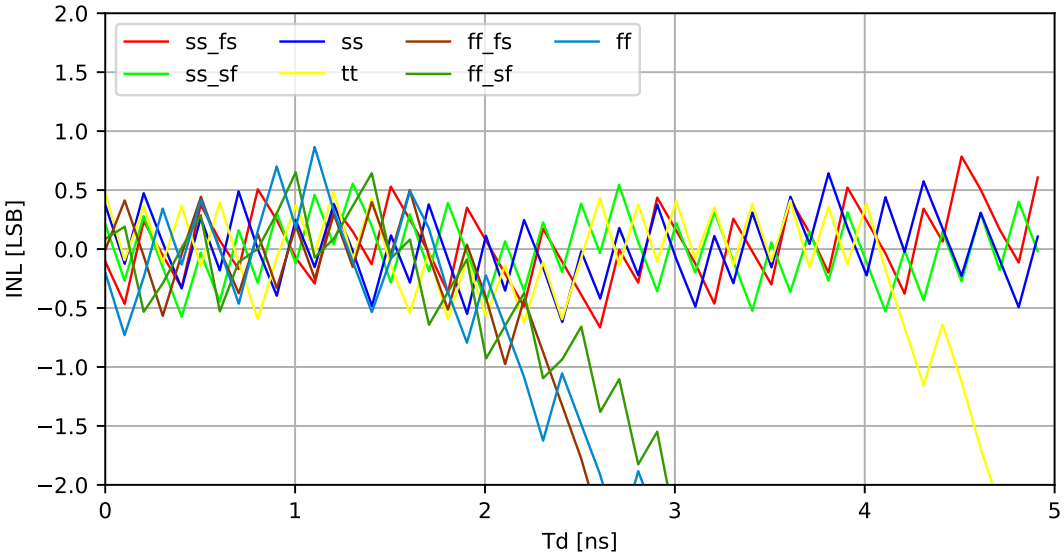


Figure 3.17: INL post-layout results for $\Delta T = 10$ ps - comparison for different transistor models at the nominal voltage supply and temperature.

Monte Carlo simulation results

To verify the TDC operation in the production process, a Monte Carlo mismatch simulation was performed. It was done for the positive TDC code range for the 10 ps time resolution setting with 100 simulation points.

During the first Monte Carlo simulation of TDC with the longest ADC conversion delays ($D9$, $D87$, $D65$, $D40$: 7777), the 12% of the conversion of ADC failed. ADC was frozen after MSB conversion. Setting a lower delay of MSB (6777 or 3777) still caused 12% of the conversions to fail (but in the 8 bit conversion). Using the most optimal setting of ADC delay (3333) has shown correct results and no failed conversions. Further investigation has shown that a change of one of the asynchronous logic blocks in SAR logic was necessary. After the change, the system worked correctly. The summary results are shown in Table 3.2. This change also improved the work of HGCROC ASIC (described in the next section) that uses the same ADC block. All results presented in this chapter are shown after the modifications of ADC.

Version	Old				New
ADC delay	7777	6777	3777	3333	7777
Failed cases [%]	12	12	12	0	0

Table 3.2: Number of failed cases before (old) and after (new) modification of one of the asynchronous logic blocks in the SAR logic.

During further Monte Carlo simulations, the dispersion of the calculated time resolution was verified (see Figure 3.18). The mean value of the obtained time resolution is 11.90 ps and its standard deviation σ is 0.65 ps. The time-resolution values range from about 10 to 14 ps. Such a large dispersion is caused by the spread of the charging currents from CP.

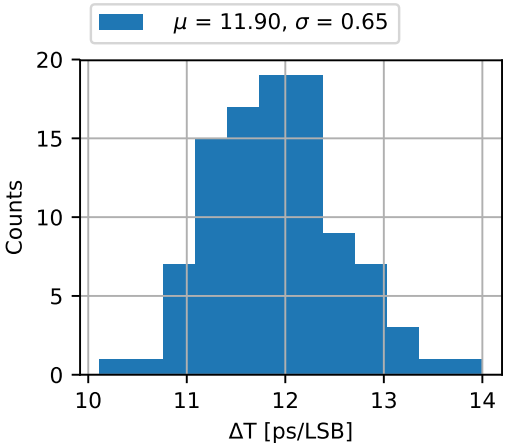


Figure 3.18: Time resolution distribution from Monte Carlo simulations (for $\Delta T = 10$ ps and 100 simulation points).

The TDC linear code range, the time difference in which the values of INL are within the ± 1 LSB, was also verified (see Figure 3.19 - the beginning of the linear range on the left and the end linear range on the right). Since only the positive part of the TDC codes was simulated at the beginning of the linear range, we expect that all values are equal to 0.0 ns. 90% of the cases have the beginning of the linear range equal to 0.00 ns, meaning that there should be no problems with non-linearity at the shortest time in these cases. At the end of the TDC linear code range, the mean value is 4.28 ns (about 360 ADC LSB). σ is equal to 0.36 ns, which means a rather large dispersion from about 3.2 ns to even 5.36 ns. However, as was seen above, the time resolution can vary from 10 to 14 ps, causing the faster or slower saturation, the smaller or larger end of the TDC linear range.

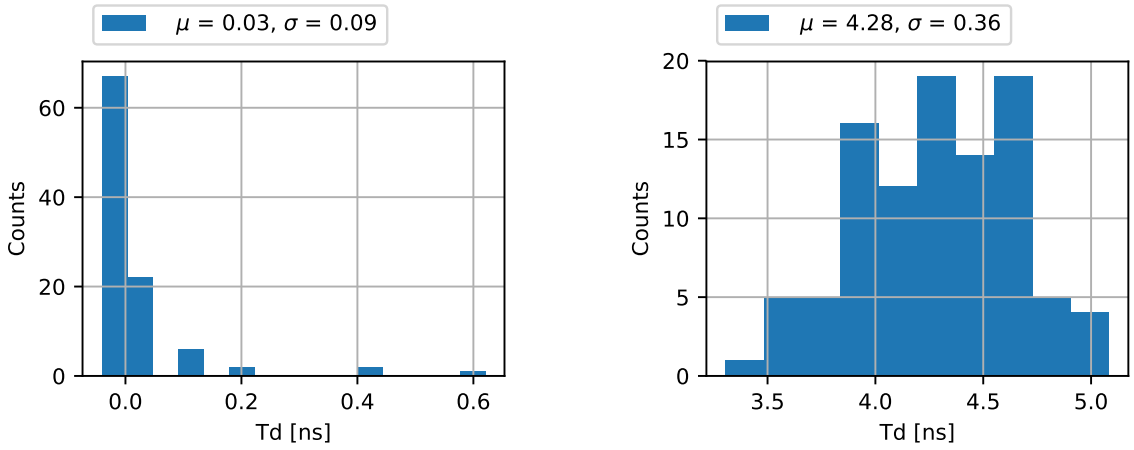


Figure 3.19: TDC linear range distribution (for $\Delta T = 10\,\text{ps}$ and 100 simulation points) from Monte Carlo simulations (the beginning of the range - left, the end of the range - right).

3.1.5 Prototype TDC ASIC design

The 8-channel prototype ASIC was accomplished and its layout is presented in Figure 3.20. In addition to the eight channels, the three DACs were placed above them, which are responsible for the TACs reference voltages. They are distributed to all channels. Around the TDC channels, the decoupling capacitors were placed, mainly connected to *Vref+* and *Vref-* of ADC. The analogue part of the prototype ASIC is part of this thesis, the digital part was designed by another person (dr Krzysztof Świentek). The input pads are directly connected to the inputs of the respective TDCs. The supply of TAC, the analogue part of ADC and the reference voltages of ADC, as well as the common mode voltages of TAC and ADC were distributed separately to one pad in the top and one pad in the bottom of prototype ASIC (except the reference voltages of ADC which had two pads on each side, two in the top and two in the bottom). The digital supply voltage of ADC was connected to the digital part of ASIC. The *TAC_ENA* signal is driven via an external pad and distributed to all channels.

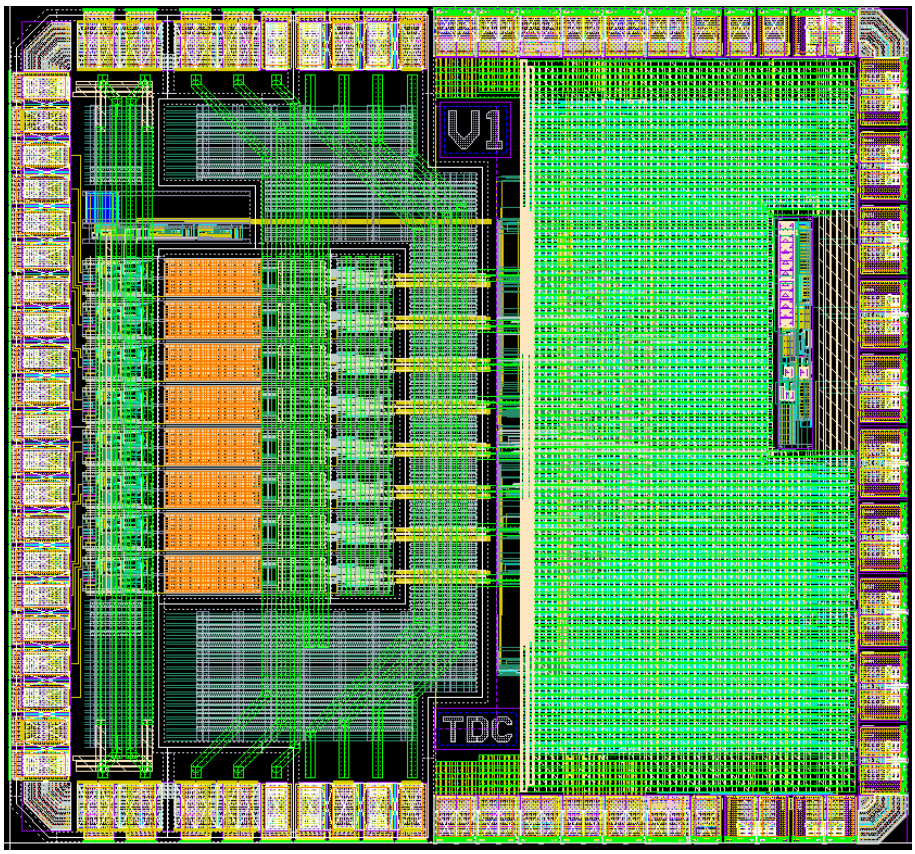


Figure 3.20: Layout of 8-channel prototype TDC ASIC.

The same simulation cell, as shown in the simulation of one channel (Figure 3.11), was used to simulate the analogue part of ASIC - 8 channels of TDC with pads. The INL results for the positive part of TDC are shown in Figure 3.21. All channels have INL within the ± 1 LSB range. The TDC shows good linearity up to about 3.7 ns. The results are worse than for a single channel of about 0.6 ns. The TDC inputs are connected directly to pads that have additional capacitance and can

cause a worsening of the linearity range. However, TDC will not be used as separate ASIC, but as a block in more complex ASIC and will not be connected directly to the pads in the final project.

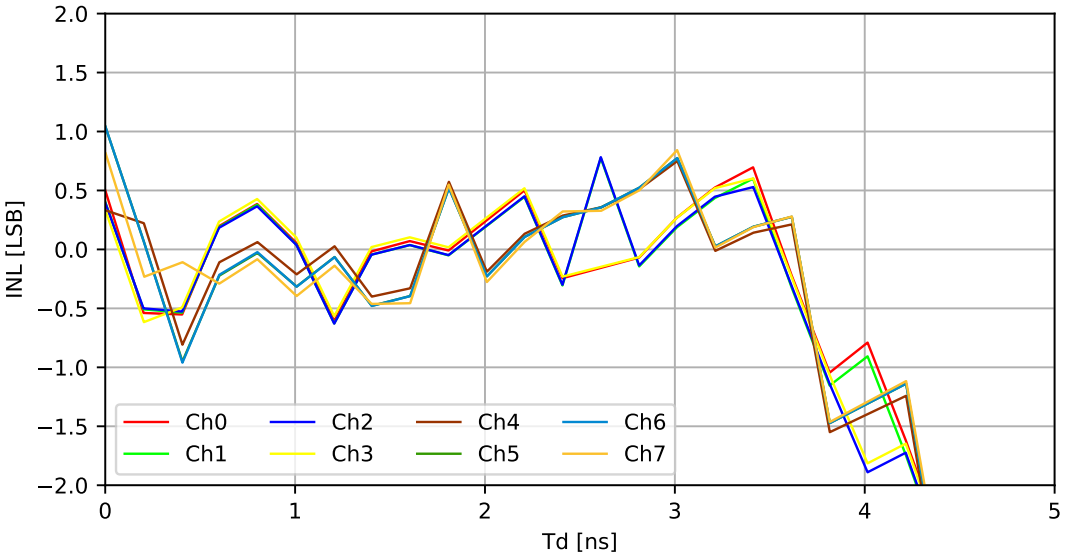


Figure 3.21: INL results for post-layout 8-channel prototype TDC ASIC.

3.1.6 Prototype measurements - preparations

The preparation of the measurement setup of the prototype TDC ASIC is still in progress. One of the steps was the design of the test board, whose layout is shown in Figure 3.22. The board consists of a prototype TDC ASIC (U1), decoupling capacitors (C1-C16) and 50 Ω termination resistors (R1-R21). The board is connected to two additional boards: to a dedicated board (through the J1 connector on the right) which provides power supply to TDC ASIC and to the board (through the PCI_EX1 connector on the top) which provides communication with FPGA (read output signals, slow-control communication and control of $\mu ASIC$ power distribution).

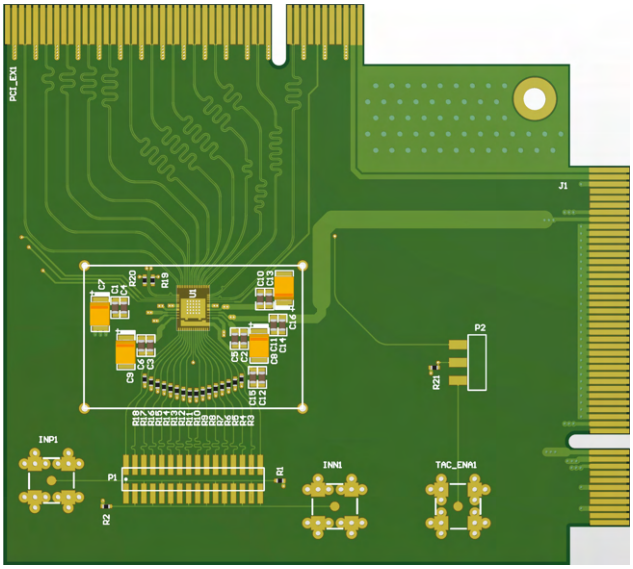


Figure 3.22: Layout of test board for 8-channel prototype TDC ASIC (top).

As input, two square signals from the generator with a proper frequency difference are given to create a time ramp (through the INP1, INN1 connectors), analogous to the simulation methodology in Section 3.1.4. The input signal can be given to the selected channel through the jumper on the P1 connector. *TAC_ENA* can be given as an external signal from the generator (TAC_ENA1 connector) or as a signal generated by FPGA - selected through the jumper on connector P2.

The measurement setup is still in progress, but the first measurements of the prototype TDC will be performed in the near future.

3.2 Measurements of 10-bit ADC for HGCROC ASIC in for HGCAL readout

3.2.1 HGCROC

High Granularity Calorimeter Read-Out Circuit (HGCROC) is a 72-channel readout ASIC radiation tolerant (block diagram Figure 3.23) developed by the OMEGA group from Ecole Polytechnique in collaboration with the groups from the CEA-IRFU Institute in Saclay, CNRS from Paris, CERN and AGH University. In addition to the 72 standard channels, it also contains two additional channels for the calibration of MIP and four common mode channels to subtract the common noise. The ASIC delivers charge and time (TOA) measurements from silicon and Silicon Photo Multipliers (SiPM) sensors in HGCAL.

HGCROC provides noise below 2500 e^- and low power consumption (below 15mW/channel). Due to the high dynamic range, it works in two ranges. In the low-end charge range, charge measurement is performed by a low-noise amplifier with configurable gain and shaper. The signal is then converted by 10-bit SAR ADC [2] (marked red in the block diagram). In the high range, the amplifier is saturated and TOT measurement is made using 12-bit TDC (time resolution 50 ps). Furthermore, the high-precision time information of TOA is obtained by 10-bit TDC with a time resolution of 25 ps. All data are transmitted at the end through two high-speed links.

The 10-bit SAR ADC, used in the low-end charge range, is the same design that was used in TDC in Section 3.1 and was developed by the AGH University group. Therefore, the focus was on the ADC and optimisation of its performance. The tests were carried out with the HGCROC2 version that contained two slightly different types of ADC: new (channels 0-35) and old (channels 36-71). Based on the version containing the latest ADC, upgraded HGCROC3 was produced [12].

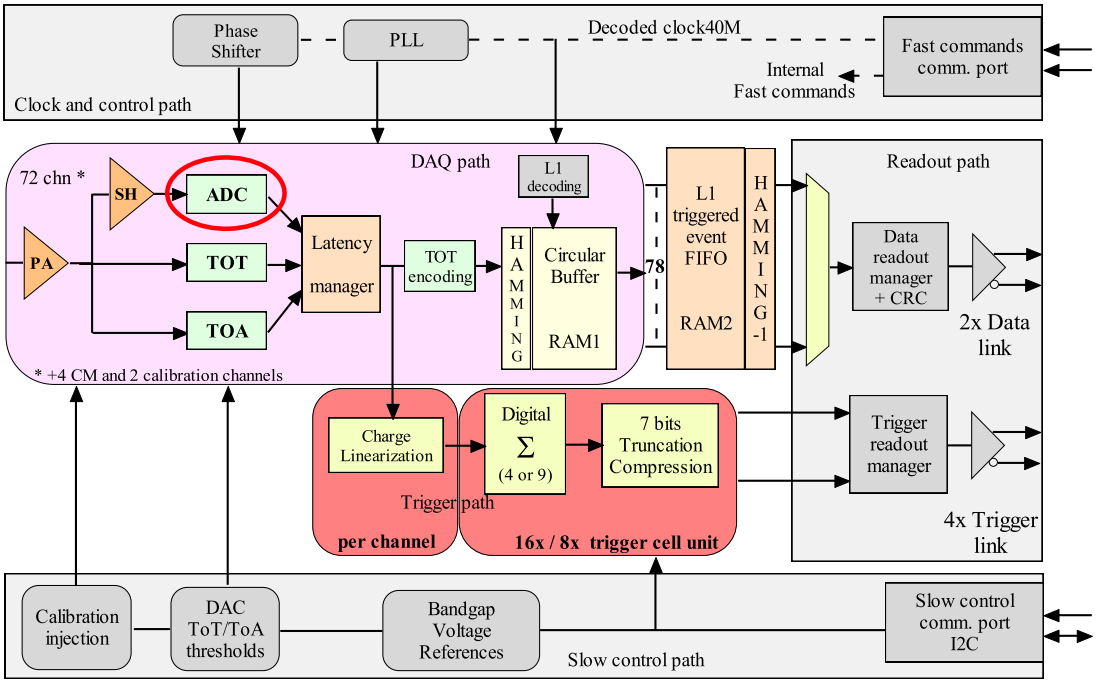


Figure 3.23: Block diagram of HGCROC [12].

3.2.2 Measurement setup and results

Measurements were performed using the Ball Grid Array (BGA) test board (Figure 3.24) where the BGA HGCROC chip was placed, full communication and testing were carried out by XILINX FPGA KSU105.

Figure 3.24: HGCROC V2 BGA testing board [13].

As mentioned in the previous section 3.1.2, the used SAR ADC has configurable delay parameters which can be set from 0 to 7 LSB. The default setup was 2222, but did not provide the best linearity performance - 4 missing codes were observed and very large INL (see example of results for channel 10 in Figures 3.25 and 3.26), so optimisation was required. Linearity was measured with two different injection signal methods, external 16-bit DAC and internal charge injection. In both, DNL and INL were calculated. Due to the large values of INL, which most probably reflected the non-linearity of the input signal not the ADC itself, DNL was chosen as the metrics more related to ADC performance, because it is less exposed to external factors. The measurements were performed under normal conditions, with all parameters set to default in the low charge range. The calibration channels were turned off. Optimisation was performed for channel 10 - the middle channel chosen from the new ADC version. The ADC clocks on the channels other than the measured one were turned off.

In the first stage, measurements were performed with an external DAC. The input data ranged from 0 to the end of the DAC range (16-bit DAC) every 100 points with 500 events per point. First, every ADC delay setting was changed from 0 to 7 (other delays in the default setup 2) to find the best performing delay setting: the shortest delay with the smallest number of missing codes and the smallest minimum and maximum DNL values. In the second step, every delay was changed $\pm$ 2 LSB from the previous best configuration. After each iteration, the best configuration was chosen, and the measurements were repeated until there were no missing codes with the shortest possible delay configuration.

Then, internal charge injection measurements were performed for the delay settings chosen as the best in external DAC measurement. The input data ranged from 0 to the end of the calib DAC range (1000) every 1 point with 500 events per point. Since the results obtained for the chosen setting still had missing codes, further optimisation was performed. The delay settings were changed $\pm$2 LSB until there were no missing codes for the shortest possible delay.

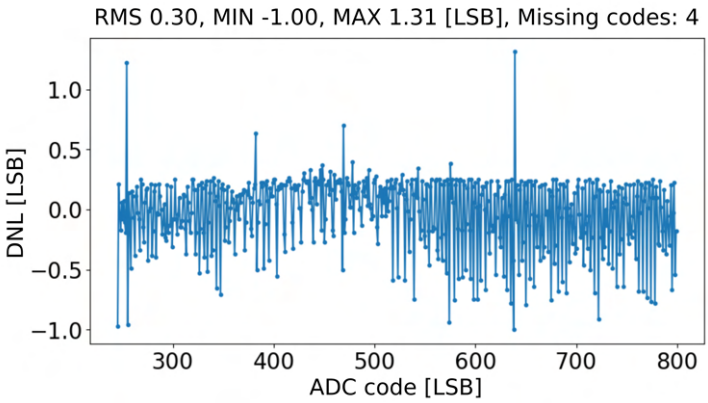


Figure 3.25: DNL results for channel 10 of HGCROC V2 made with external DAC.

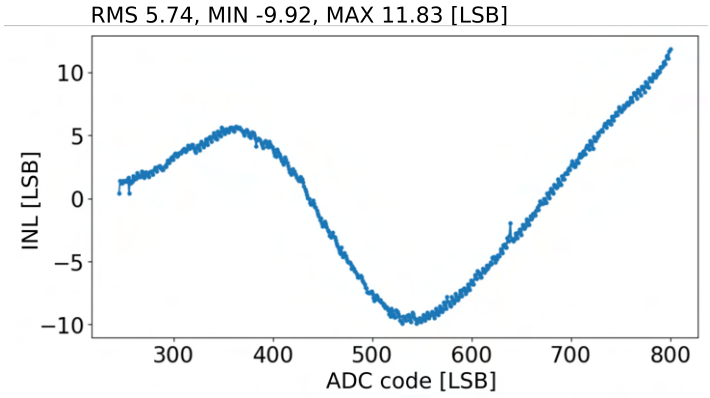


Figure 3.26: INL results for channel 10 of HGCROC V2 made with external DAC.

After all the optimisation steps, the final delay setting was chosen as 3432. Subsequently, measurements were also made with the final setup for all other channels. The results for selected channels with external DAC are presented in Figures 3.27 (DNL) and 3.29 (INL) and with charge injection Figures 3.28 (DNL) and 3.30 (INL).

In most of the charge range, the DNL is within the ± 0.5 LSB range. For the new version of ADC (channels 0-35) no missing codes are observed with the charge injection method, except for two channels with the same missing code, some slight optimisation still might be needed. In the old version ADC (channels 36-71) two similar missing codes are observed in most cases - there is a need for longer delays.

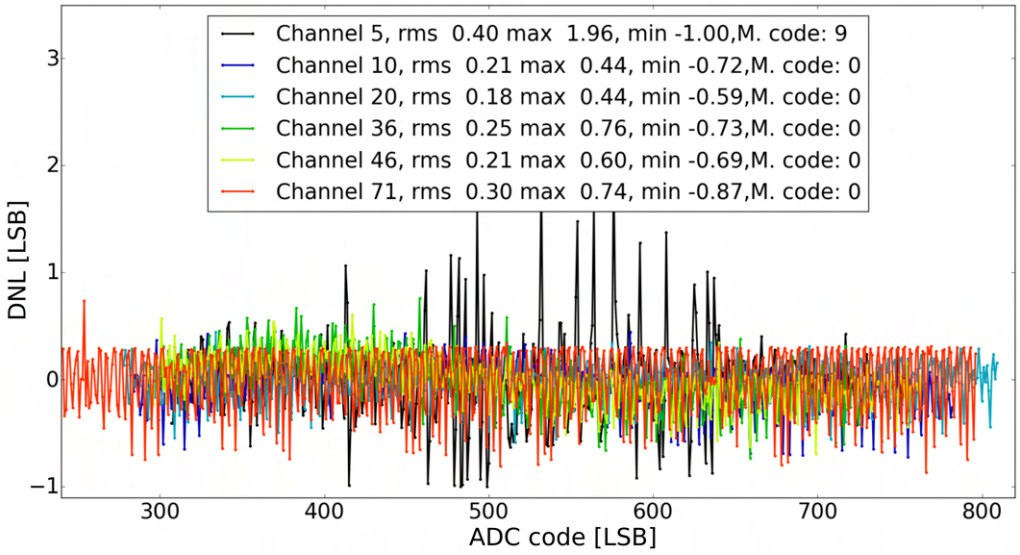


Figure 3.27: DNL results for selected channels of HGCROC V2 made with external DAC.

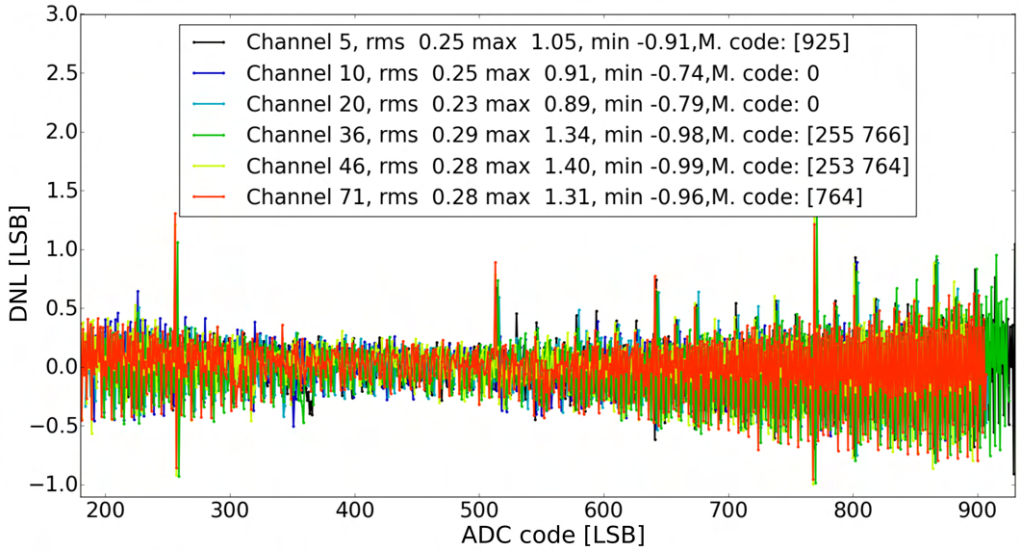


Figure 3.28: DNL results for selected channels of HGCROC V2 made with charge injection.

The INL in both measurements (Figures 3.29 and 3.30) has larger values than expected. In the charge injection method, different values are observed for particular channels, but a similar trend is visible. Typically, in most of the range ± 4 LSB non-linearity is seen. The INL results with external DAC are different for each channel – no pattern between channels is visible, probably the external DAC is 'fighting' with the front-end to inject the signal, which causes such a large non-linearity. It confirms that the non-linearity is not connected to the ADC performance and rather to the input signal, since measurements of only the ADC [2] show INL < 0.5 LSB.

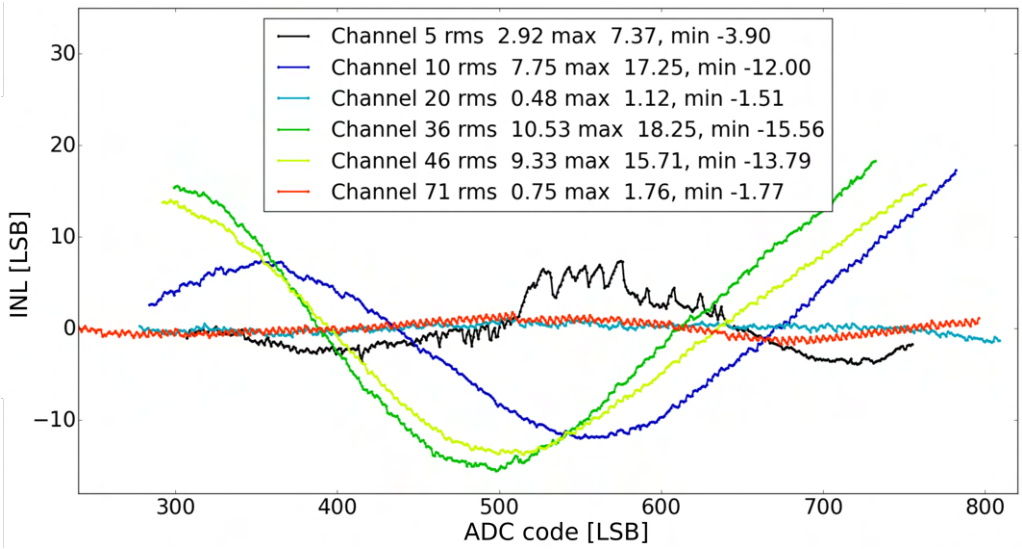


Figure 3.29: INL results for selected channels of HGCROC V2 made with external DAC.

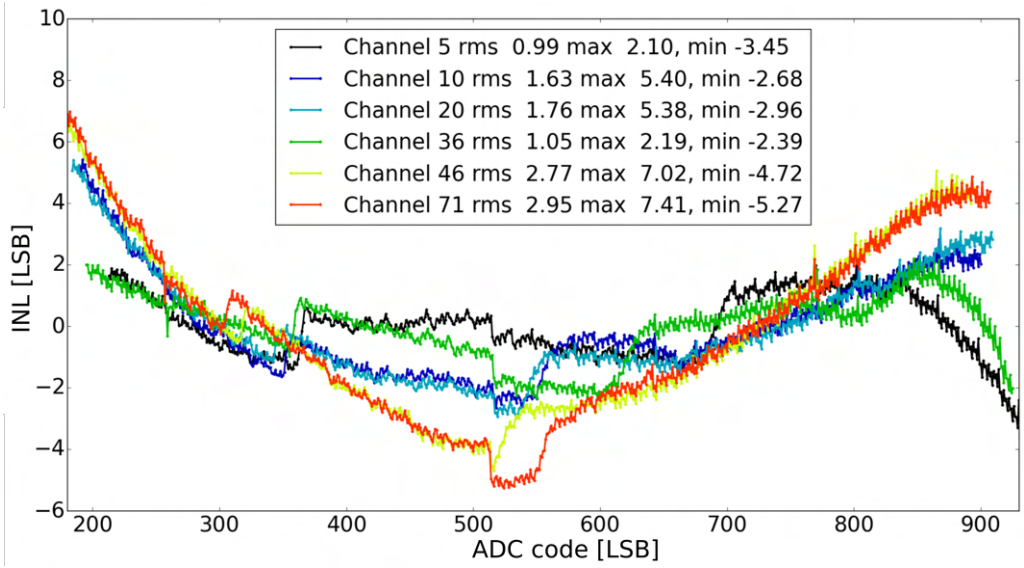


Figure 3.30: INL results for selected channels of HGCROC V2 made with charge injection.

Measurements with optimised delay settings were also performed for different front-end ranges (different gain): 80 fC (high gain), 160 fC (default setting) and 320 fC. DNL results (results for channel 10 in Figure 3.31) are very similar, no missing codes are observed. INL results (Figure 3.32) vary from each other. The lower the gain (higher ADC range) is set, the bigger non-linearity is observed.

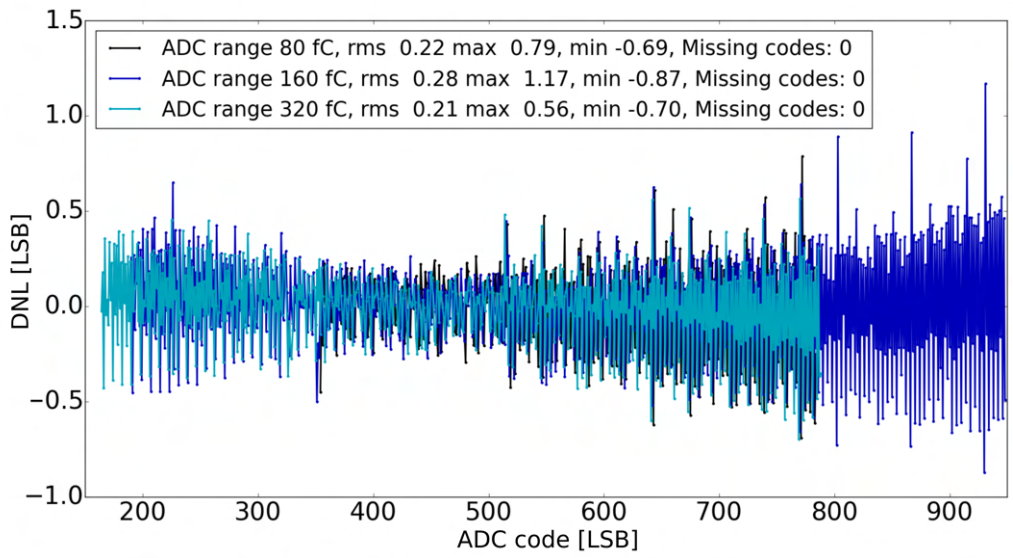


Figure 3.31: DNL results for channel 10 of HGCROCV2 made for different charge range.

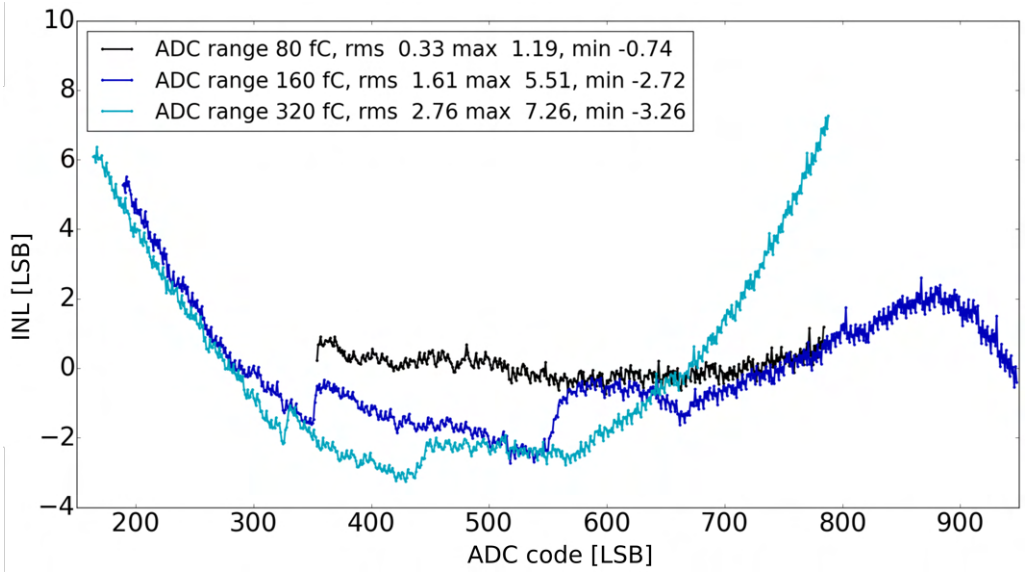


Figure 3.32: INL results for channel 10 of HGCROC V2 made for different charge range.

Summary

The aim of this thesis was the development of detector readout systems for particle physics experiments using advanced CMOS technologies. Author took part in a few different projects that allowed to participate in various phases of developing readout system. The author was involved in designing circuits in submicron CMOS technology (TDC design), testing and optimisation of ASIC (PASTTREC and HGCROC measurements), final readout system and the whole detector module tests (measurements of electronic readout system for $\overline{\mathrm{P}}\mathrm{ANDA}$ and HADES experiments), and monitoring of detector operation during beamtime of HADES experiment.

In the first chapter, the author presents the theoretical introduction to the topic of particle physics experiments with an overview of experiments important for this thesis: CMS, HADES and $\overline{\mathrm{P}}\mathrm{ANDA}$ with particular attention to the straw tube tracking detectors used in the HADES and $\overline{\mathrm{P}}\mathrm{ANDA}$ experiments.

In the second chapter, the author describes the measurements associated with the $\overline{\mathrm{P}}\mathrm{ANDA}$ and HADES experiments. First, the author performed the optimisation of FEBs, which led to reducing the number of components and resizing the board. During the tests, a lower voltage supply was also proposed which significantly reduced the power consumption of the entire system. In the main part of this project, the author was involved in the preparation of the mass test setup, which allows one to measure up to 8 FEBs (16 PASTTRECs) in parallel. In the primary tests in 2021, 140 FEBs (280 PASTTRECs) were tested, which provided quite a large number of ASICs for statistical analyses of their parameters and functionality. As a result of the analysis performed by the author, the 97% production yield of PASTTRECs was obtained. Parameters such as baseline, gain, offset, and noise were analysed and appropriate baseline equalisation factors were found. No significant differences were observed between different ASIC channels taking into account the baseline, gain, and offset parameters. These parameters depend only on the operating point of the front-end electronics, while noise can also be affected by other factors, for example, the middle channels may not pick up the same disturbances as the edge channels. Therefore, the noise difference between the channels was greater.

In the next step, the author participated in the measurements with the straw tube module and the ^{55}Fe source in the Jagiellonian University laboratory. The author performed data analysis and the first part of the tests confirmed the correctness of the baseline equalisation settings. The aforementioned results were presented by the author during the TWEPP conference in September 2022 in the form of the poster [28] and then published in JINST in May 2023 [10]. The author also presented progress of the work during four $\overline{\mathrm{P}}\mathrm{ANDA}$ collaboration meetings.

During the next part of the measurements with straw tubes and ^{55}Fe source, the author carried out in-depth separation studies of peaks from the radioactive source. Since the TOT measurements are non-linear as a function of injected charge, the first part of the measurements was performed using the linear threshold scan method to obtain reference separation power values ($S \approx 5.7 - 6.1$). Next, TOT scans were performed for different gain, HV and threshold settings. The separation power obtained by this method was approximately 20% lower than that obtained by the linear threshold scan method. The best separation power results were obtained for lower HV and a larger threshold at the highest gain setting. However, previous studies [33] showed that spatial resolution and detector performance worsen with increasing threshold and decreasing HV. Due to these reasons, compromise settings should be used in the future. In all the above parts of the project, the author's main task was data analysis, but also participation in measurements and preparation of measurement setup.

Furthermore, in February-March 2022, the author participated in a one-week internship in the HADES experiment during beamtime. The author was involved in the monitoring of the STS detector. The internship also gave the opportunity to become familiar with the operation of the HADES experiment.

In the third chapter, the author focusses on the development of dedicated ASICs for future experiments. The main part of this chapter was the design of a Time-to-Digital Converter (TDC). The design was based on the analog interpolators architecture, which consist of two parts, TAC and ADC. The 10-bit SAR ADC designed by the AGH University group [1, 2] was taken as the basis and the author was involved mainly in the TAC design (schematic and layout), merging both parts and making small modifications in ADC (removing the bootstrap and providing the proper propagation of signals responsible for communication between TAC and ADC). Furthermore, the author performed schematic and post-layout simulations. The designed TDC operates in U2 coding, which means that MSB corresponds to the sign value and the output code range is from -512 to 511. There are two input signals (*InU* and *InD*) that can be interpreted as, for example, the particle arrival signal and the reference signal. The TDC measures the time difference between their rising edges and converts it to the digital output. The circuit has a configurable time resolution from 10 ps to 100 ps. The author performed a series of simulations, including corner and Monte Carlo simulations, to verify the performance for the two time resolution settings (10 ps and 100 ps). For both cases, the values of DNL were within $\pm$ 0.5 LSB throughout the entire range and no missing codes were observed. The 10 ps time resolution setting showed INL values $\pm$0.5 LSB within -365 to 375 LSB range, which covers more than 70% of the ADC code range. For 100 ps, INL values are $\pm$3 LSB from -478 to 483 LSB, which is almost entire ADC range. Better results were obtained for finer time resolution since the optimisation was done for this configuration. However, further optimisation can be done in the future for the longer time resolution if required.

Based on the TDC design, the 8-channel prototype TDC ASIC was prepared. The author was responsible for the analog part of the chip. Additionally, the author designed the test board for prototype testing. The preparation of measurement setup is in progress and it is hoped that in the near future the TDC ASIC will be verified. The TDC was designed with the possibility of being

part of one of the ASICs for future experiments, since time measurement is becoming one of the most important features of modern particle physics designs, next to amplitude measurements.

In the last part of the third chapter, the author presents the ADC measurements of the HGCROC readout for the HGCAL detector in the upgraded CMS experiment. In connection with measurements, the author took part in a one-week internship at the OMEGA group of Ecole Polytechnique in 2020. The ADC used as part of HGCROC is the same 10-bit SAR ADC that was used in the aforementioned TDC design and was developed by the AGH University group. Based on the obtained INL and DNL results, the most optimal ADC delay settings were found. The author performed ADC measurements and data analysis of the obtained results. All results were presented by the author to the HGCROC collaboration during two HGCAL electronic meetings and internal meetings with the OMEGA group. Furthermore, during the TDC Monte Carlo simulation a small issue was found in the ADC design, which caused a small modification to its design and improved the HGCROC ASIC operation.

In summary, the research presented in this thesis is the result of the collaboration between the KOiDC group from AGH University and other institutes, including the Jagiellonian University group ($\overline{\mathrm{P}}$ANDA and HADES experiments) and the OMEGA group from Ecole Polytechnique (HGCROC for the detector HGCAL in the CMS experiment of CERN). The author's contribution to the mentioned thesis projects was the following:

- Measurements and data analysis of the results obtained in: (1) FEB optimisation, (2) mass tests measurements and qualification of electronics readout system for straw tubes for HADES and $\overline{\mathrm{P}}$ANDA experiments, and (3) measurements with straw tubes and ^{55}Fe source.
- Participation in the monitoring of the straw tube detector for one week in the HADES experiment during beamtime.
- Design of the schematic and layout of TAC (part of the TDC circuit), small changes in the SAR ADC design (removing the bootstrap and providing the proper propagation of signals responsible for communication between TAC and ADC), merge both parts of TDC, simulations of the TDC circuit together with data analysis, and design of TDC test board.
- ADC measurements of the HGCROC ASIC and data analysis of the obtained results.

Appendix

PASTTREC mass test - results

Baseline correction

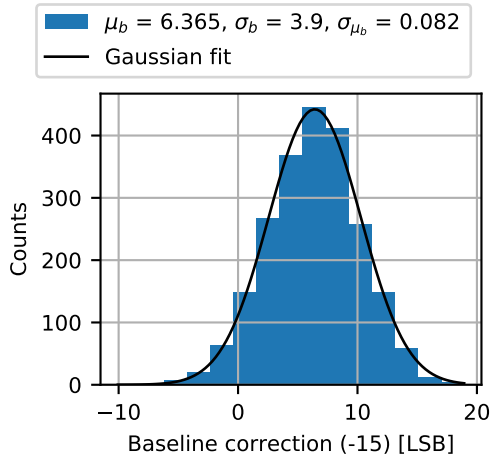


Figure D.33: Distribution of baseline correction (*1mV20ns*) for all 2216 channels (values shifted by -15 LSB).

Table D.3: Statistical parameters (μ_{bch}, σ_{bch}, $\sigma_{\mu_{bch}}$) of baseline correction values for the groups of individual ASIC channels (*1mV20ns*).

ASIC channel	μ_{bch} [LSB]	σ_{bch} [LSB]	$\sigma_{\mu_{bch}}$ [LSB]
ch0	6.29	3.9	0.24
ch1	6.33	3.7	0.23
ch2	6.45	4.0	0.24
ch3	6.24	3.7	0.22
ch4	6.48	4.1	0.24
ch5	6.30	3.9	0.23
ch6	6.53	3.7	0.22
ch7	6.32	3.9	0.24

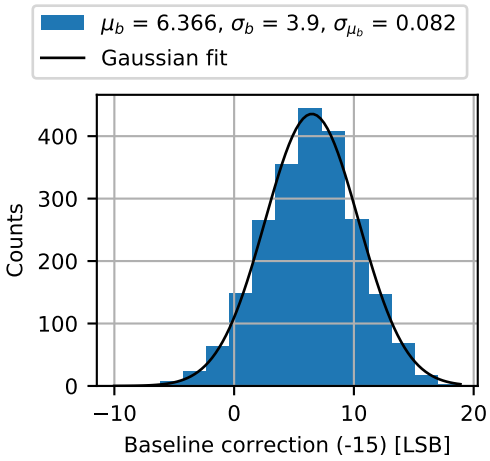


Figure D.34: Distribution of baseline correction (*2mV15ns*) for all 2216 channels (values shifted by -15 LSB).

Table D.4: Statistical parameters (μ_{bch}, σ_{bch}, $\sigma_{\mu_{bch}}$) of baseline correction values for the groups of individual ASIC channels (*2mV15ns*).

ASIC channel	μ_{bch} [LSB]	σ_{bch} [LSB]	$\sigma_{\mu_{bch}}$ [LSB]
ch0	6.28	3.9	0.24
ch1	6.33	3.7	0.22
ch2	6.44	4.0	0.24
ch3	6.25	3.7	0.23
ch4	6.47	4.1	0.24
ch5	6.30	3.9	0.23
ch6	6.53	3.7	0.22
ch7	6.32	3.9	0.24

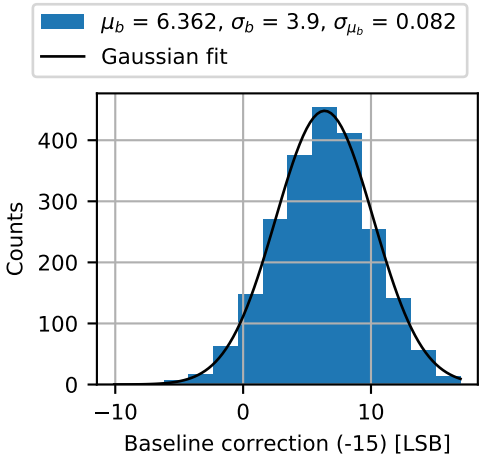


Figure D.35: Distribution of baseline correction (*2mV20ns*) for all 2216 channels (values shifted by -15 LSB).

Table D.5: Statistical parameters (μ_{bch}, σ_{bch}, $\sigma_{\mu_{bch}}$) of baseline correction values for the groups of individual ASIC channels (*2mV20ns*).

ASIC channel	μ_{bch} [LSB]	σ_{bch} [LSB]	$\sigma_{\mu_{bch}}$ [LSB]
ch0	6.29	3.9	0.24
ch1	6.33	3.7	0.23
ch2	6.45	4.0	0.24
ch3	6.23	3.7	0.22
ch4	6.48	4.1	0.25
ch5	6.30	3.9	0.23
ch6	6.53	3.7	0.22
ch7	6.30	3.9	0.24

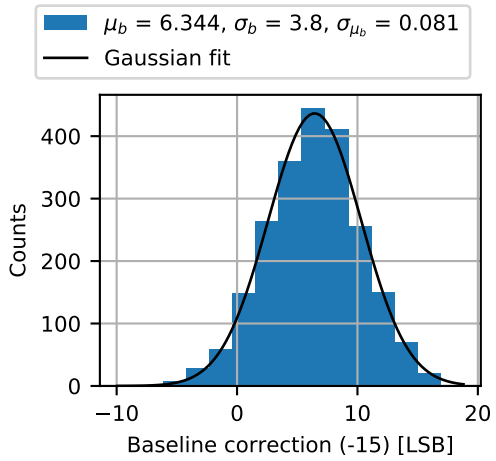


Figure D.36: Distribution of baseline correction (*4mV15ns*) for all 2216 channels (values shifted by -15 LSB).

Table D.6: Statistical parameters (μ_{bch}, σ_{bch}, $\sigma_{\mu_{bch}}$) of baseline correction values for the groups of individual ASIC channels (*4mV15ns*).

ASIC channel	μ_{bch} [LSB]	σ_{bch} [LSB]	$\sigma_{\mu_{bch}}$ [LSB]
ch0	6.26	3.9	0.23
ch1	6.32	3.7	0.22
ch2	6.43	4.0	0.24
ch3	6.23	3.7	0.22
ch4	6.45	4.0	0.24
ch5	6.29	3.8	0.23
ch6	6.52	3.7	0.22
ch7	6.26	3.9	0.23

Gain

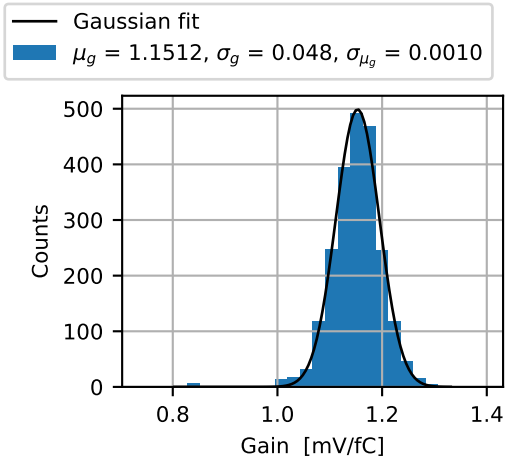


Figure D.37: Distribution of gain values (*1mV20ns*) for all 2216 channels.

Table D.7: Statistical parameters (μ_{gch}, σ_{gch}, $\sigma_{\mu_{gch}}$) of gain values for the groups of individual ASIC channels (*1mV20ns*).

ASIC channel	μ_{gch} [mV]	σ_{gch} [mV/fC]	$\sigma_{\mu_{gch}}$ [mV/fC]
ch0	1.1515	0.048	0.0029
ch1	1.1517	0.048	0.0029
ch2	1.1546	0.049	0.0029
ch3	1.1466	0.048	0.0029
ch4	1.1520	0.048	0.0029
ch5	1.1493	0.048	0.0029
ch6	1.1543	0.048	0.0029
ch7	1.1494	0.047	0.0028

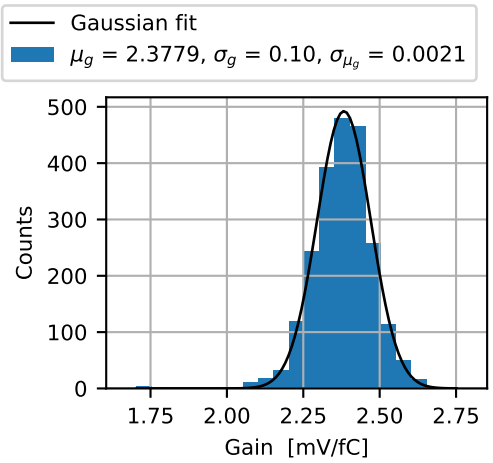


Figure D.38: Distribution of gain values (*2mV15ns*) for all 2216 channels.

Table D.8: Statistical parameters (μ_{gch}, σ_{gch}, $\sigma_{\mu_{gch}}$) of gain values for the groups of individual ASIC channels (*2mV15ns*).

ASIC channel	μ_{gch} [mV/fC]	σ_{gch} [mV/fC]	$\sigma_{\mu_{gch}}$ [mV/fC]
ch0	2.3777	0.10	0.0059
ch1	2.3787	0.10	0.0060
ch2	2.3848	0.10	0.0061
ch3	2.3688	0.10	0.0061
ch4	2.3800	0.10	0.0061
ch5	2.3748	0.10	0.0060
ch6	2.3841	0.10	0.0060
ch7	2.3742	0.10	0.0058

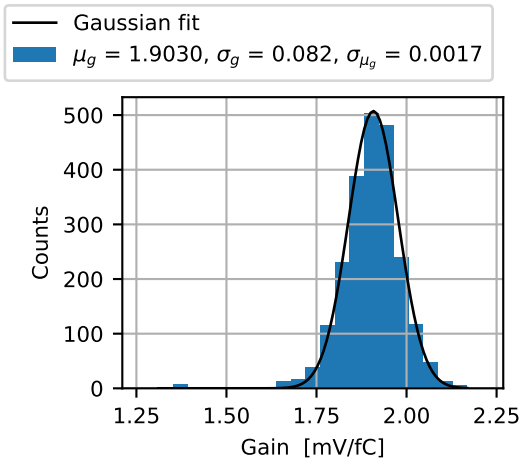


Figure D.39: Distribution of gain values (*2mV20ns*) for all 2216 channels.

Table D.9: Statistical parameters (μ_{gch}, σ_{gch}, $\sigma_{\mu_{gch}}$) of gain values for the groups of individual ASIC channels (*2mV20ns*).

ASIC channel	μ_{gch} [mV/fC]	σ_{gch} [mV/fC]	$\sigma_{\mu_{gch}}$ [mV/fC]
ch0	1.9033	0.081	0.0048
ch1	1.9041	0.082	0.0049
ch2	1.9092	0.083	0.0050
ch3	1.8957	0.082	0.0049
ch4	1.9046	0.083	0.0050
ch5	1.9005	0.081	0.0049
ch6	1.9077	0.082	0.0049
ch7	1.8993	0.080	0.0048

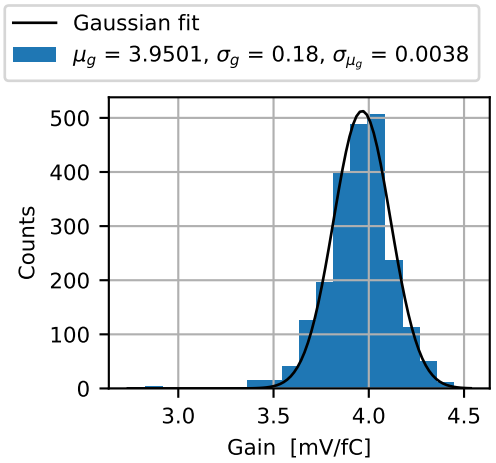


Figure D.40: Distribution of gain values (*4mV15ns*) for all 2216 channels.

Table D.10: Statistical parameters (μ_{gch}, σ_{gch}, $\sigma_{\mu_{gch}}$) of gain values for the groups of individual ASIC channels (*4mV15ns*).

ASIC channel	μ_{gch} [mV/fC]	σ_{gch} [mV/fC]	$\sigma_{\mu_{gch}}$ [mV/fC]
ch0	3.951	0.18	0.011
ch1	3.952	0.18	0.011
ch2	3.964	0.19	0.011
ch3	3.938	0.18	0.011
ch4	3.955	0.18	0.011
ch5	3.944	0.18	0.011
ch6	3.958	0.18	0.011
ch7	3.939	0.18	0.011

Offset

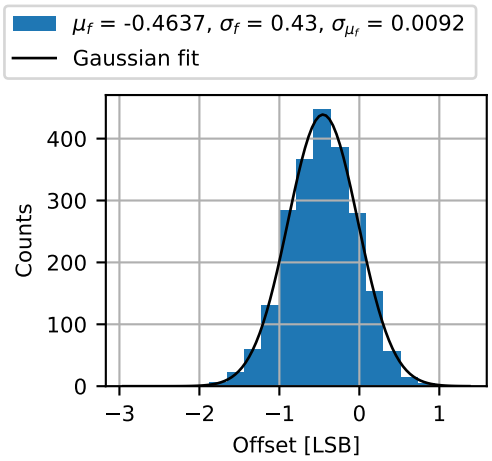


Figure D.41: Distribution of offset values (*1mV20ns*) for all 2216 channels.

Table D.11: Statistical parameters (μ_{fch}, σ_{fch}, $\sigma_{\mu_{fch}}$) of offset values for the groups of individual ASIC channels (*1mV20ns*).

ASIC channel	μ_{fch} [LSB]	σ_{fch} [LSB]	$\sigma_{\mu_{fch}}$ [LSB]
ch0	-0.464	0.42	0.025
ch1	-0.461	0.43	0.026
ch2	-0.509	0.42	0.026
ch3	-0.454	0.44	0.026
ch4	-0.444	0.46	0.027
ch5	-0.416	0.42	0.025
ch6	-0.480	0.44	0.026
ch7	-0.480	0.43	0.024

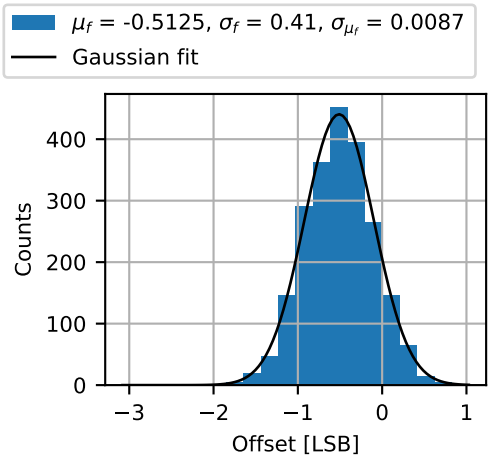


Figure D.42: Distribution of offset values (*2mV15ns*) for all 2216 channels.

Table D.12: Statistical parameters (μ_{fch}, σ_{fch}, $\sigma_{\mu_{fch}}$) of offset values for the groups of individual ASIC channels (*2mV15ns*).

ASIC channel	μ_{fch} [LSB]	σ_{fch} [LSB]	$\sigma_{\mu_{fch}}$ [LSB]
ch0	−0.526	0.43	0.026
ch1	−0.511	0.39	0.024
ch2	−0.533	0.43	0.026
ch3	−0.484	0.41	0.024
ch4	−0.500	0.43	0.026
ch5	−0.512	0.40	0.024
ch6	−0.502	0.40	0.024
ch7	−0.532	0.38	0.023

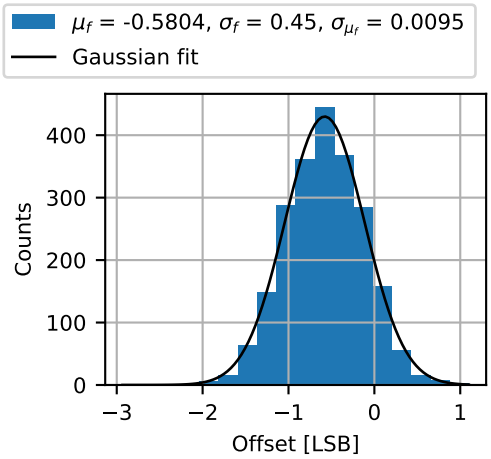


Figure D.43: Distribution of offset values (*2mV20ns*) for all 2216 channels.

Table D.13: Statistical parameters (μ_{fch}, σ_{fch}, $\sigma_{\mu_{fch}}$) of offset values for the groups of individual ASIC channels (*2mV20ns*).

ASIC channel	μ_{fch} [LSB]	σ_{fch} [LSB]	$\sigma_{\mu_{fch}}$ [LSB]
ch0	−0.576	0.45	0.027
ch1	−0.572	0.43	0.026
ch2	−0.608	0.47	0.028
ch3	−0.564	0.42	0.025
ch4	−0.558	0.47	0.028
ch5	−0.556	0.44	0.026
ch6	−0.588	0.46	0.028
ch7	−0.622	0.43	0.026

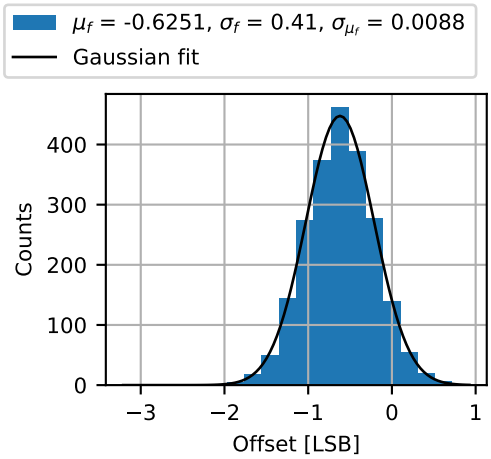


Figure D.44: Distribution of offset values (*4mV15ns*) for all 2216 channels.

Table D.14: Statistical parameters (μ_{fch}, σ_{fch}, $\sigma_{\mu_{fch}}$) of offset values for the groups of individual ASIC channels (*4mV15ns*).

ASIC channel	μ_{fch} [LSB]	σ_{fch} [LSB]	$\sigma_{\mu_{fch}}$ [LSB]
ch0	−0.641	0.43	0.026
ch1	−0.619	0.42	0.025
ch2	−0.645	0.44	0.026
ch3	−0.601	0.41	0.025
ch4	−0.604	0.451	0.027
ch5	−0.597	0.42	0.025
ch6	−0.638	0.43	0.026
ch7	−0.657	0.39	0.024

Noise

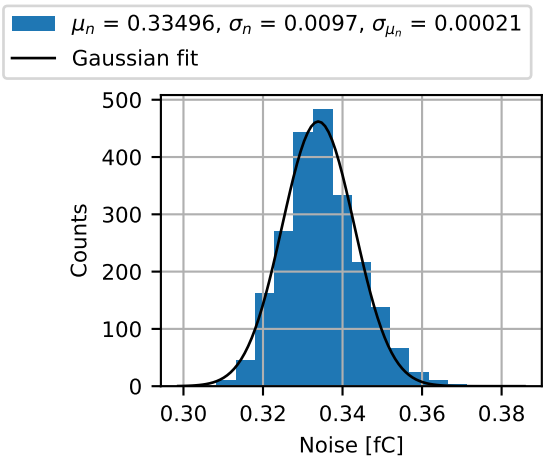


Figure D.45: Distribution of noise values (*1mV20ns*) for all (2216) channels (Th = 10).

Table D.15: Statistical parameters (μ_{nch}, σ_{nch}, $\sigma_{\mu_{nch}}$) of noise values for the groups of individual ASIC channels (*1mV20ns*, Th = 10).

ASIC channel	μ_{nch} [fC]	σ_{nch} [fC]	$\sigma_{\mu_{nch}}$ [fC]
ch0	0.33356	0.0095	0.00057
ch1	0.33389	0.0103	0.00062
ch2	0.33375	0.0096	0.00057
ch3	0.33633	0.0097	0.00058
ch4	0.33565	0.0087	0.00052
ch5	0.33551	0.0097	0.00059
ch6	0.33397	0.0092	0.00055
ch7	0.33704	0.0101	0.00061

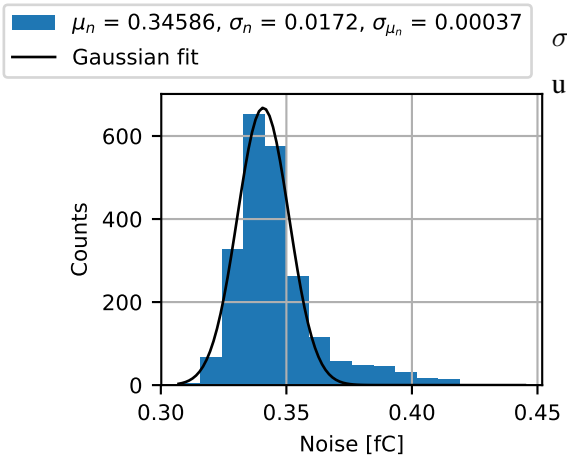


Figure D.46: Distribution of noise values (*1mV20ns*) for all (2216) channels.

Table D.16: Statistical parameters (μ_{nch}, σ_{nch}, $\sigma_{\mu_{nch}}$) of noise values for the groups of individual ASIC channels (*1mV20ns*).

ASIC channel	μ_{nch} [fC]	σ_{nch} [fC]	$\sigma_{\mu_{nch}}$ [fC]
ch0	0.33356	0.0095	0.00057
ch1	0.33389	0.0103	0.00062
ch2	0.33375	0.0096	0.00057
ch3	0.33633	0.0097	0.00058
ch4	0.33565	0.0087	0.00052
ch5	0.33551	0.0097	0.00059
ch6	0.33397	0.0092	0.00055
ch7	0.33704	0.0101	0.00061

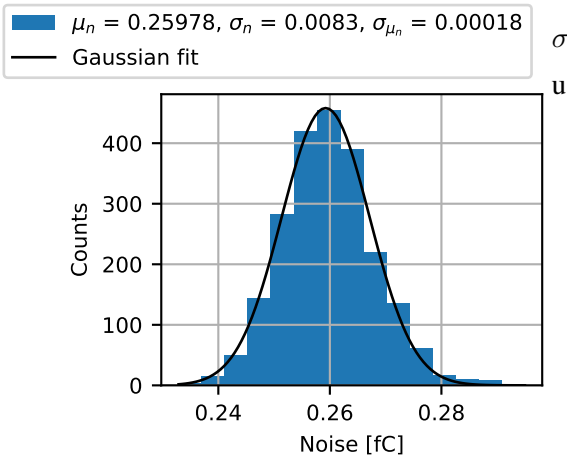


Figure D.47: Distribution of noise values (*2mV15ns*) for all (2216) channels.

Table D.17: Statistical parameters (μ_{nch}, σ_{nch}, $\sigma_{\mu_{nch}}$) of noise values for the groups of individual ASIC channels (*2mV15ns*).

ASIC channel	μ_{nch} [fC]	σ_{nch} [fC]	$\sigma_{\mu_{nch}}$ [fC]
ch0	0.25532	0.0083	0.00050
ch1	0.25739	0.0083	0.00050
ch2	0.25922	0.0079	0.00048
ch3	0.26337	0.0074	0.00045
ch4	0.26278	0.0075	0.00045
ch5	0.26012	0.0084	0.00050
ch6	0.25837	0.0078	0.00047
ch7	0.26167	0.0073	0.00044

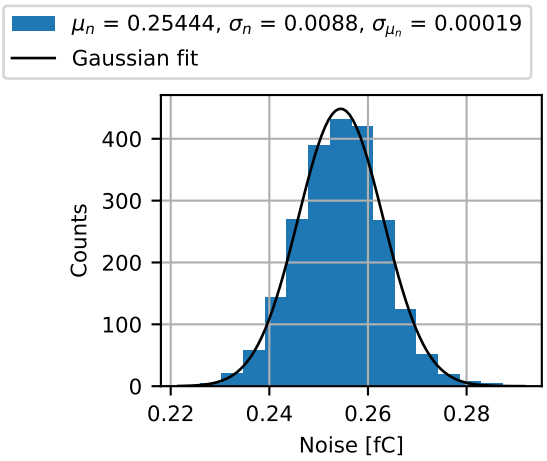


Figure D.48: Distribution of noise values (*2mV20ns*) for all (2216) channels.

Table D.18: Statistical parameters (μ_{nch}, σ_{nch}, $\sigma_{\mu_{nch}}$) of noise values for the groups of individual ASIC channels (*2mV20ns*).

ASIC channel	μ_{nch} [fC]	σ_{nch} [fC]	$\sigma_{\mu_{nch}}$ [fC]
ch0	0.25065	0.0088	0.00053
ch1	0.25280	0.0085	0.00051
ch2	0.25362	0.0093	0.00056
ch3	0.25731	0.0084	0.00051
ch4	0.25682	0.0080	0.00048
ch5	0.25515	0.0085	0.00051
ch6	0.25301	0.0084	0.00050
ch7	0.25612	0.0082	0.00050

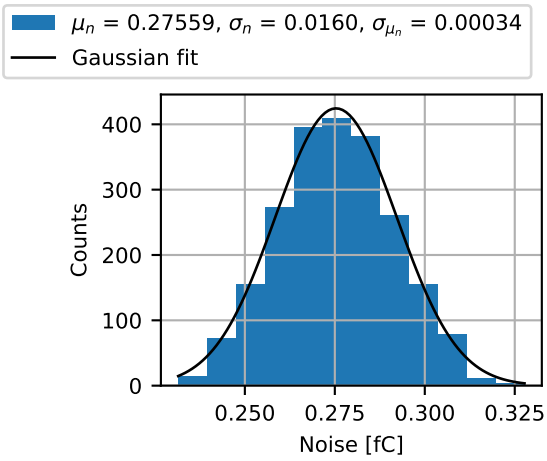


Figure D.49: Distribution of noise values (*4mV15ns*) for all (2216) channels.

Table D.19: Statistical parameters (μ_{nch}, σ_{nch}, $\sigma_{\mu_{nch}}$) of noise values for the groups of individual ASIC channels (*4mV15ns*).

ASIC channel	μ_{nch} [fC]	σ_{nch} [fC]	$\sigma_{\mu_{nch}}$ [fC]
ch0	0.25622	0.011	0.00064
ch1	0.26828	0.012	0.00072
ch2	0.27655	0.013	0.00080
ch3	0.28851	0.012	0.00075
ch4	0.28755	0.013	0.00080
ch5	0.27595	0.015	0.00089
ch6	0.27116	0.012	0.00071
ch7	0.28047	0.012	0.00075

TDC

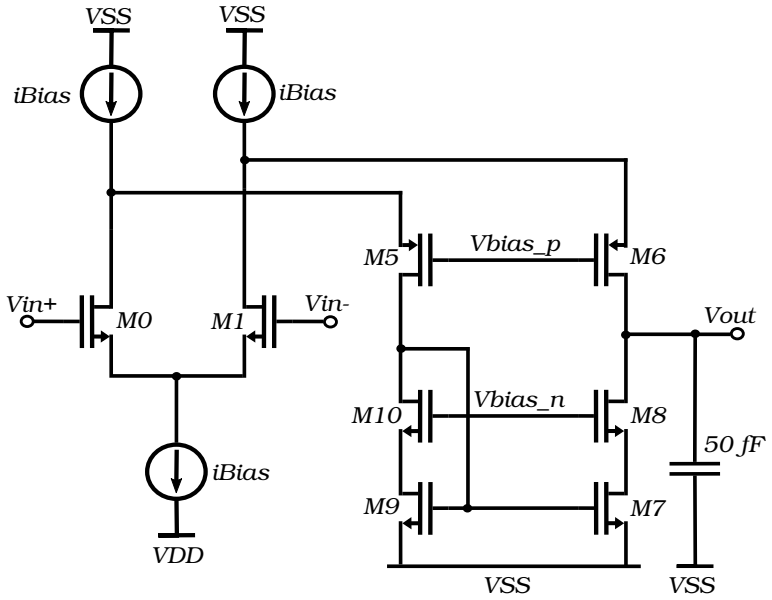


Figure D.50: Block diagram of OTAn (CP).

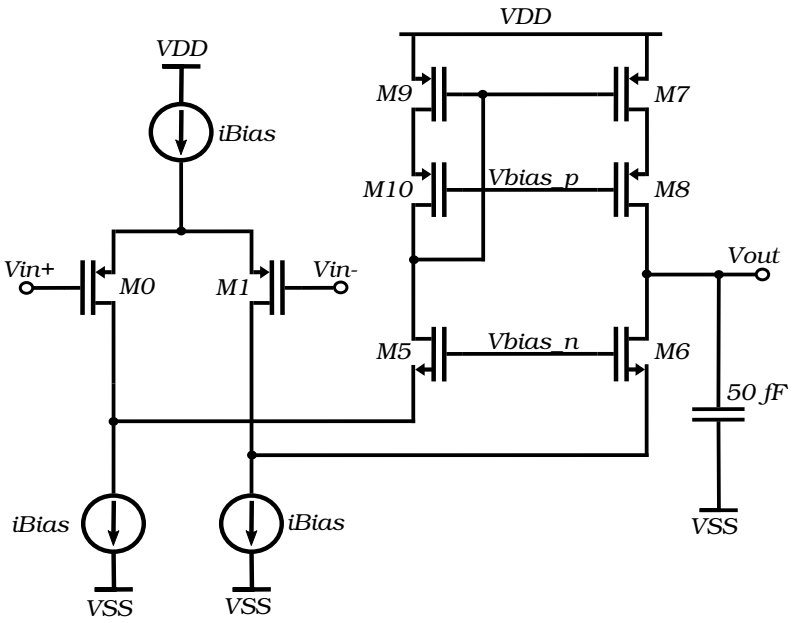


Figure D.51: Block diagram of OTAp (CP).

Table D.20: OTA parameters in post-layout simulations.

	Phase Margin [°]	K [dB]	f_{3dB} [kHz]
OTAn0	72.45	43.25	817.375
OTAn1	72.6	43.25	823.938
OTAp0	72.54	42.94	908.508
OTAp1	72.59	42.94	902.283

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