Chapter 7
Performance testing

7.1 LVDS signal quality

Signal quality may be measured by a variety of means. Common methods are:

- Measuring rise time at the load
- Measuring jitter in an eye pattern
- Bit error rate testing
- Other means

Eye patterns and Bit Error Rate Testing (BERT) are commonly used to determine signal quality. These two methods are described next.

7.1.1 LVDS signal quality: jitter measurements using eye patterns

This report provides an example of a data rate vs. cable length curve for LVDS drivers and receivers in a typical application for a particular twisted pair cable. The questions of: "How far?" and "How fast?" seem simple to answer at first, but after detailed study, the answers become quite complex.

This is not a simple device parameter specification. But rather, a system level question where a number of other parameters besides the switching characteristics of the drivers and receivers must be known. This includes the measurement criteria for signal quality that has been selected, and also the pulse coding that will be used (NRZ for example). Additionally, other system level components should be known too. This includes details about cables, connectors, and the PCB.

Since the purpose is to measure signal quality, it should be done in a test fixture that closely matches the end environment – or even better – in the actual application. Eye pattern measurements are useful in measuring the amount of jitter vs. the unit interval to establish the data rate vs. cable length curves and therefore are a very accurate way to measure the expected signal quality in the end application.

7.1.2 Why eye patterns?

The eye pattern is used to measure the effects of inter-symbol interference on random data being transmitted through a particular medium. The prior data bits effect the transition time of the signal. This is especially true for NRZ data that does not guarantee transitions on the line. For example, in NRZ coding, a transition high after a long series of lows has a slower rise time than the rise time of a periodic (010101) waveform. This is due to the low pass filter effects of the cable.

Figure 7.1 illustrates the superposition of six different data patterns. Overlaid, they form the eye pattern that is the input to the cable. The right hand side of this figure illustrates the same pattern at the end of the cable. Note the rounding of the formerly sharp transitions. The width of the crossing point is now wider and the opening of the eye is also now smaller (see Application Note AN-808 for an extensive discussion on eye patterns).

When line drivers (generators) are supplying symmetrical signals to clock leads, the period of the clock, rather than the unit interval of the clock waveform, should be used to determine the maximum cable lengths (e.g., though the clock rate is twice the data rate, the same maximum cable length limits apply). This is due to the fact that a periodic waveform is not prone to distortion from inter-symbol distortion as is a data line.

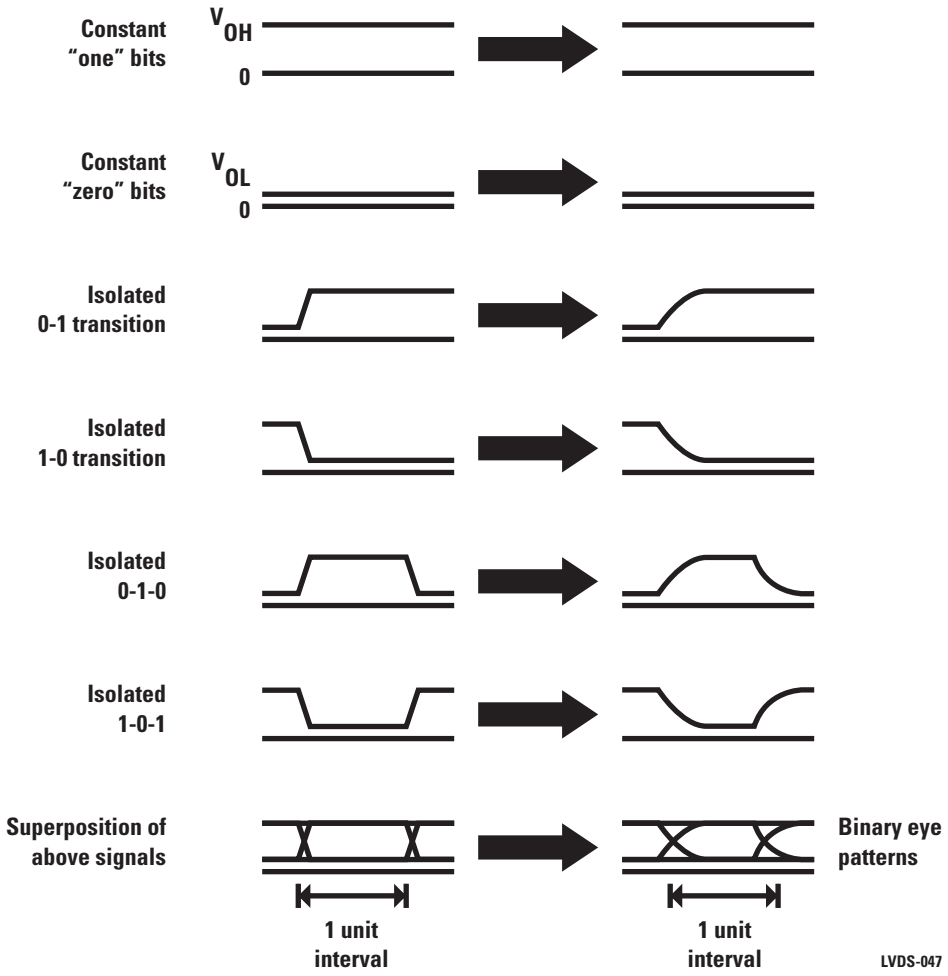

Figure 7.1. Formation of an eye pattern by superposition

Figure 7.2 describes the measurement locations for minimum jitter. Peak-to-peak jitter is the width of the signal crossing the optimal receiver thresholds. For a differential receiver, that would correspond to 0V (differential). However, the receiver is specified to switch between -100 mV and +100 mV. Therefore for a worse case jitter measurement, a box should be drawn between ±100 mV and the jitter measured between the first and last crossing at ±100 mV. If the vertical axis units in Figure 7.2 were 100 mV/div, the worse case jitter is at ±100 mV levels.

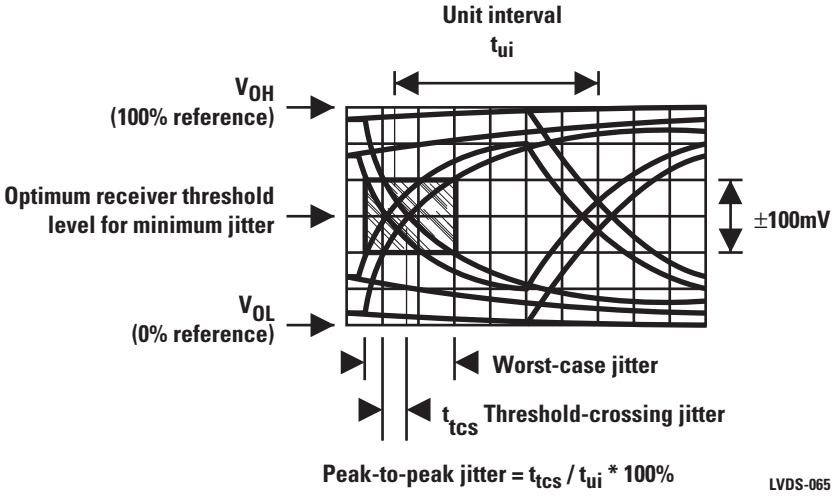

Figure 7.2. NRZ data eye pattern

7.1.3. Eye pattern test circuit

LVDS drivers and receivers are typically used in an uncomplicated point-to-point configuration as shown in Figure 7.3. It details the test circuit that was used to acquire the eye pattern measurements. It includes the following components:

PCB#1 – DS90C031 LVDS quad driver soldered to the PCB with matched PCB traces between the device (located near the edge of the PCB) to the connector. The connector is an AMP AMPLIMITE™ .050 series connector.

Cable – The cable used for this testing was Berk-Tek part number 271211. This is a CAT3 105Ω (differential-mode) 28 AWG stranded twisted pair cable (25 pair with overall shield) commonly used on SCSI applications. This cable represents a common data interface cable. For this test report, the following cable lengths were tested: 1, 2, 3, 5, and 10m. Cables longer that 10m were not tested, but may be employed at lower data rates. Berk-Tek no longer manufactures this cable. Similar cable is available through other vendors such as Hitachi Cable Manchester. (Part # 49251)

PCB#2 – DS90C032 LVDS quad receiver soldered to the PCB with matched PCB traces between the device (located near the edge of the PCB) to the connector. The connector is an AMPLIMITE .050 series connector. A 100Ω surface mount resistor was used to terminate the cable at the receiver input pins.

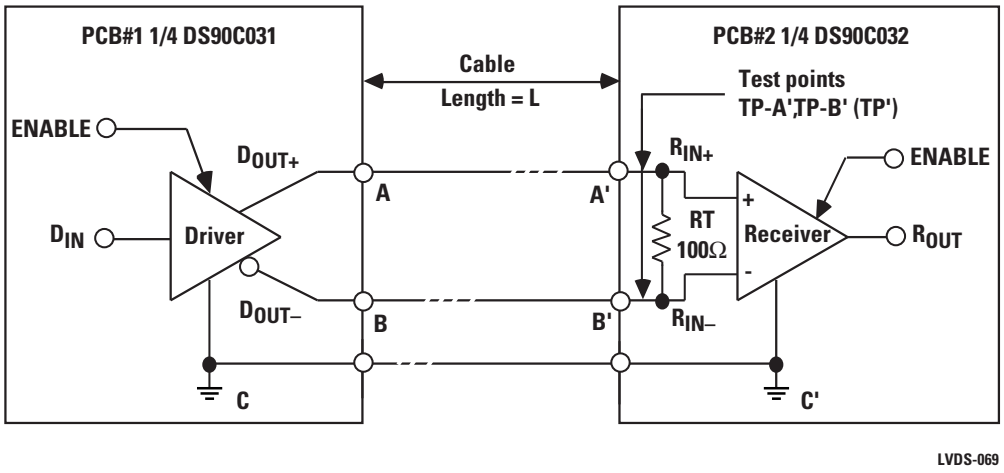

Figure 7.3. LVDS signal quality test circuit

7.1.4 Test procedure

A pseudo random bit sequence (PRBS) generator was connected to the driver input, and the resulting eye pattern (measured differentially at TP') was observed on the oscilloscope. Different cable lengths (L) were tested, and the frequency of the input signal was increased until the measured jitter equaled 20% with respect to the unit interval for the particular cable length. The coding scheme used was NRZ. Jitter was measured twice at two different voltage points. Jitter was first measured at the 0V differential voltage (optimal receiver threshold point) for minimum jitter, and second at the maximum receiver threshold points (±100 mV) to obtain the worst case or maximum jitter at the receiver thresholds. Occasionally jitter is measured at the crossing point alone and although this will result in a much lower jitter point, it ignores the fact that the receivers may not switch at that very point. For this reason, this signal quality test report measured jitter at both points.

7.1.5 Using differential probes

The use of differential probes is usually recommended when testing any differential signal, whether it be LVDS, ECL, or CML. The same effects that a differential receiver in a real system benefits from, apply to oscilloscopes and other forms of test equipment.

Differential probing leads to more accurate measurements and better noise rejection than single ended probing, but the results need to be interpreted with care. The definition and use of the term 'Differential swing' is not consistent across the industry. Many data-sheets and the LVDS specification define it as $(D_{O+}) - (D_{O-})$. This is not the same amplitude that would be measured by a differential probe. The output of such a probe will typically be $2 \times [(D_{O+}) - (D_{O-})]$.

7.1.6 Results and data points

Table 7.1. 20% jitter table @ 0V differential (minimum jitter)

Cable length (m)	Data rate (Mbps)	Unit interval (ns)	Jitter (ns)
1	400	2.500	0.490
2	391	2.555	0.520
3	370	2.703	0.524
5	295	3.390	0.680
10	180	5.550	1.160

As described above, jitter was measured at the 0V differential point. For the case with the 1m cable, 490 ps of jitter at 400 Mbps was measured, and with the 10m cable, 1.160 ns of jitter at 180 Mbps was measured.

Table 7.2. 20% Jitter table @ ±100 mV (maximum Jitter)

Cable length (m)	Data rate (Mbps)	Unit interval (ns)	Jitter (ns)
1	200	5.000	1.000
2	190	5.263	1.053
3	170	5.882	1.176
5	155.5	6.431	1.286
10	100	10.000	2.000

The second case measured jitter between ±100 mV levels. For the 1m cable, 1 ns of jitter was measured at 200 Mbps, and for the 10m cable, 2 ns of jitter occurred at 100 Mbps.

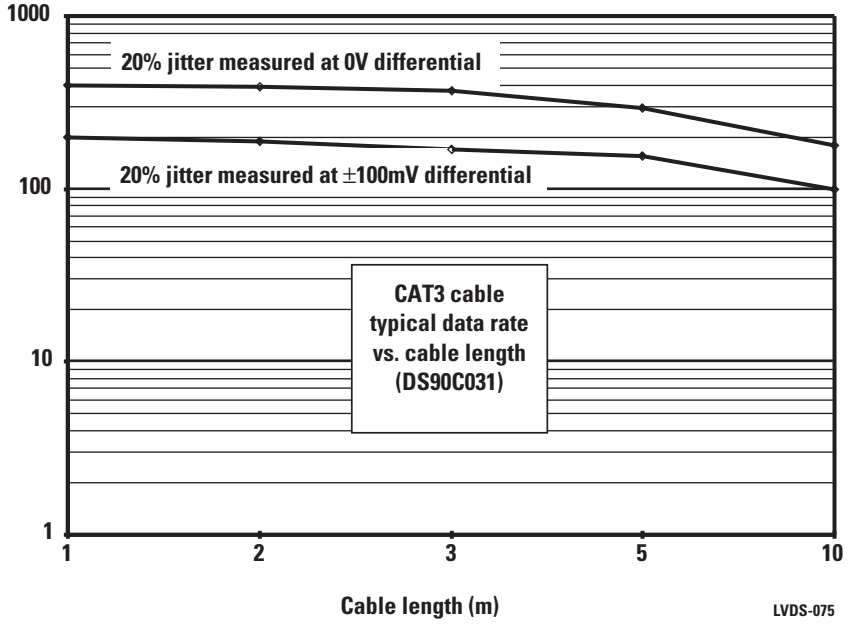

Figure 7.4. Typical data rate vs. cable length for 0m to 10m CAT3 cable

Care should be taken in long cable applications using LVDS. When directly coupled, LVDS provides up to ±1V common-mode rejection. Long cable applications may require larger common-mode support. If this is the case, transformer coupling or alternate technologies (such as RS-485) should be considered.

Figure 7.4 is a graphical representation of the relationship between data rate and cable length for the application under test. Both curves assume a maximum allotment of 20% jitter with respect to the unit interval. Basically, data rates between 200 Mbps to 400 Mbps are possible at shorter lengths, and rates of 100 Mbps to 200 Mbps are possible at 10m. Note that employing a different coding scheme, cable, or wire gauge (AWG) will create a different relationship between maximum data rate vs. cable length. Designers are greatly encouraged to experiment on their own.

7.1.7 Additional data on jitter and eye patterns

For additional information on LVDS "data rate vs. cable length" please consult the list of LVDS application notes on the LVDS webstie at: LVDS.national.com

At this time of this printing the following application notes were available:

Application note #	Devices tested
AN-977	DS90C031/032
AN-1088	DS90LV017/027, DS92LV010A

7.1.8 Conclusions – eye pattern testing

Eye patterns provide a useful tool to analyze jitter and the resulting signal quality as it captures the effects of a random data pattern. They provide a method to determine the maximum cable length for a given data rate or vice versa. Different systems, however, can tolerate different levels of jitter. Commonly 5%, 10%, or 20% is acceptable with 20% jitter usually being an upper practical limit. More than 20% jitter tends to close down the eye opening, making error-free recovery of NRZ data more difficult. This report illustrates data rate vs. distance for a common, inexpensive type of cable.

7.2 BERT

Bit error ratio testing is another approach to determine signal quality. This test method is described next.

7.2.1 LVDS cable driving performance using BERT

The questions of: "How far?" and "How fast?" seem simple to answer at first, but after detailed study, their answers become quite complex. This is not a simple device parameter specification. But rather, a system level question, and to be answered correctly a number of other parameters besides the switching characteristics of the drivers and receivers must be known. This includes the measurement criteria for signal quality that has been selected, and the pulse coding that will be used (Non-Return to Zero (NRZ) for example – see Application Note AN-808 for more information about coding). Additionally, other system level components should be known too. This includes details about the cable, connector and information about the printed circuit boards (PCB). Since the purpose is to measure signal quality/performance, it should be done in a test fixture that matches the end environment precisely if possible. The actual application would be best if possible. There are numerous methods to measure signal quality, including eye pattern (jitter) measurements and BER tests.

This report provides the results of a series of BER tests performed on the DS90C031/032 LVDS quad line driver/receiver devices. The results can be generalized to other National LVDS products. Four drivers were used to drive 1m to 5m of standard twisted pair cables at selected data rates. Four receivers were used to recover the data at the load end of the cable.

7.2.2 What is a BERT?

Bit rror eatio testing is one way to measure the performance of a communications system. The standard equation for a bit error rate measurement is:

BER = (number of bit errors)/(total number of bits)

Common measurement points are bit error rates of:
$1^3 \times 10^{-12}$ => one or less errors in 1 trillion bits sent
1×10^{-14} => one or less errors in 100 trillion bits sent

Note that BERT is time intensive. The time length of the test is determined by the data rate and also the desired performance benchmark. For example, if the data rate is 50 Mbps, and the benchmark is an error rate of 1×10^{-14} or better, a run time of 2,000,000 seconds is required for a serial channel. 2,000,000 seconds equates to 555.6 hours or 23.15 days!

7.2.3 BERT circuit

LVDS drivers and receivers are typically used in an uncomplicated point-to-point configuration as shown in Figure 7.2. This figure details the test circuit that was used. It includes the following components:

PCB#1 – DS90C031 LVDS quad driver soldered to the PCB with matched PCB traces between the device (located near the edge of the PCB) to the connector. The connector is an AMPLIMITE .050 series connector.

Cable – Cable used for this testing was Berk-Tek part number 271211. This is a CAT3 105Ω (differential-mode) 28 AWG stranded twisted pair cable (25 pair with overall shied) commonly used in SCSI applications. This cable represents a common data interface cable. For this test report, cable lengths of 1m and 5m were tested. Berk-Tek no longer manufactures this cable. Similar cable is available through other vendors such as Hitachi Cable Manchester. (Part # 49251)

PCB#2 – DS90C032 LVDS Quad Receiver soldered to the PCB with matched PCB traces between the device (located near the edge of the PCB) to the connector. The connector is an AMPLIMITE .050 series connector. A 100Ω surface mount resistor was used to terminate the cable at the receiver input pins.

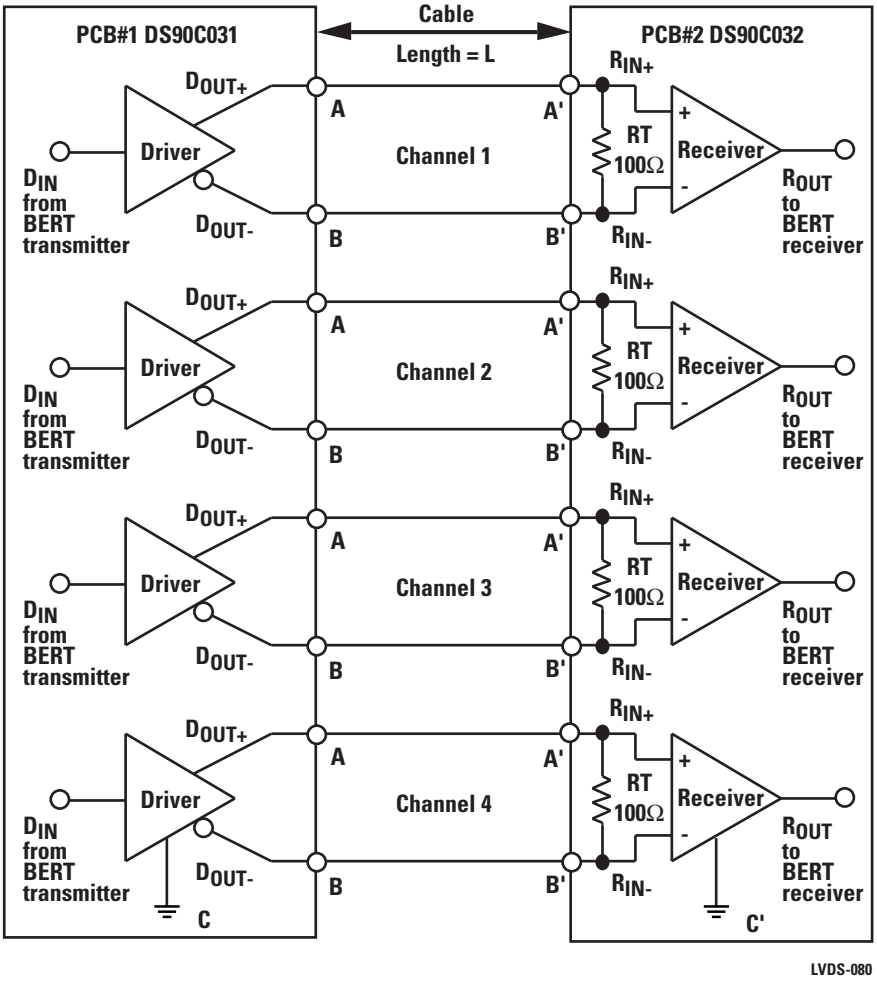

Figure 7.5. LVDS BERT circuit

7.2.4 Test procedure

A parallel high-speed bit error ratio transmitter/receiver set (Tektronix MultiBERT-100) was employed for the tests. The transmitter was connected to the driver inputs, and the receiver outputs were connected to the BERT receiver inputs. Different cable lengths and data rates were tested. The tester was configured to provide a PRBS of 2^{15}- 1 (32,767 bit long sequence). In the first test, the same input signal was applied to all four of the LVDS channels under test. For the other tests, the PRBS was offset by 4 bits, thus providing a random sequence between channels. The coding scheme used was NRZ. Upon system test configuration, the test was allowed to run uninterrupted for a set amount of time. At completion of the time block, the results were recorded which included: elapsed seconds, total bits transmitted and number of bit errors recorded. For the three tests documented next, a power supply voltage of +5.0V was used and the tests were conducted at room temperature.

7.2.5 Tests and results

The goal of the tests was to demonstrate errors ratios of less than 1×10^{-12} are obtainable.

Test 1
Conditions

- Data rate = 50 Mbps
- Cable length = 1m
- PRBS code = 2^{15}- 1 NRZ

For this test, the PRBS code applied to the four driver inputs was identical. This created a "simultaneous output switching" condition on the device.

Results

- Total seconds: 87,085 (1 day)
- Total bits: $1{,}723 \times 10^{13}$
- Errors = 0
- Error ratio = $< 1 \times 10^{-12}$

Test 2
Conditions

- Data rate = 100 Mbps
- Cable length = 1m
- PRBS code = 2^{15}- 1 NRZ

For this test, the PRBS code applied to the four driver inputs was offset by four bits. This creates a random pattern between channels.

Results

- Total seconds: 10,717 (~3 hr)
- Total bits: 4.38×10^{12}
- Errors = 0
- Error ratio = $< 1 \times 10^{-12}$

Test 3
Conditions

- Data rate = 100 Mbps
- Cable length = 5m
- PRBS code = 2^{15}- 1 NRZ

For this test, the PRBS code applied to the four driver inputs was offset by four bits. This creates a random pattern between channels.

Results

- Total seconds: 10,050 (~2.8 hr)
- Total bits: 4×10^{12}
- Errors = 0
- Error ratio = $< 1 \times 10^{-12}$

7.2.6 Conclusions – BERT

All three of the tests ran error free and demonstrate extremely low bit error ratios using LVDS technology. The tests concluded that error ratios of < 1 x 10^{15}- 1 can be obtained at 100 Mbps operation across 5m of twisted pair cable.

BER tests only provide a "go/no go" data point if zero errors are detected. It is recommended to conduct further tests to determine the point of failure (data errors). This will yield important data that indicates the amount of margin in the system. This was done in tests conducted by increasing the cable length from 1m to 5m, and also adjusting the data rate from 50 Mbps to 100 Mbps.

Additionally, bench checks were made while adjusting the power supply voltage from 5.0V to 4.5V and 5.5V, adjusting clock frequency, and applying hot/cold temperatures to the device under test (DUT). No errors were detected during these checks (tests were checks only and were not conducted over time, i.e., 24 hr). BERTs conclude that the PRBS patterns were transmitted error free across the link. This was concluded by applying a pattern to the input and monitoring the receiver output signal.