

Matching Model for Planar Bulk Transistors With Halo Implantation

Ulrich Schaper, *Senior Member, IEEE*, and Jan Einfeld

Abstract—Threshold voltage matching of long-channel planar bulk transistors deteriorates strongly by halo implantations compared to the matching of nonhalo devices which follow a gate area dependence (Pelgrom's model). A new compact matching model explains the observations and extends Pelgrom's model to halo transistors using the $V_t(L)$ behavior of the device. The new model is generally valid for halo and nonhalo transistors. It has been tested for several transistor types and technology nodes, showing a significantly increased accuracy. A measure for the halo impact on matching is given.

Index Terms—Doping density, halo implantation, matching model, threshold voltage, threshold voltage mismatch, transistor matching.

I. INTRODUCTION

TRANSISTOR matching is one of the key parameters for the design of high-precision circuits since parameter variations limit circuit performance in modern technologies. Matching is characterized by the standard deviation $\sigma_{\Delta V_t}$ of the distribution of threshold voltage differences ΔV_t derived from closely spaced identical devices. Assuming that the devices of a pair are independent from each other, the standard deviation for single devices is $\sigma_{V_t} = \sigma_{\Delta V_t} / \sqrt{2}$.

Causes of the V_t matching are random dopant fluctuations, fixed trapped charges, granularity of the gate electrode, and line edge roughness [1]. Planar bulk devices of mainstream technologies are considered here to be used for digital (minimum-gate-length) and mixed signal (medium- to long-gate-length) applications. For these transistors, the main part of the V_t matching originates from the random dopant fluctuations for current technologies [1]. SOI devices or FinFETs [2] are not taken into account.

Transistors with a homogeneously doped channel follow the widely used Pelgrom matching model [3], [4] predicting better matching for larger gate geometry

$$\sigma_{V_t}^2 = \frac{A_{V_t}^2}{W \cdot L} \quad (1)$$

where W and L are the gate width and length, respectively, and A_{V_t} is the matching parameter.

For planar bulk transistors with strong halo implantations, this model fails for long gate lengths. A warning has to be

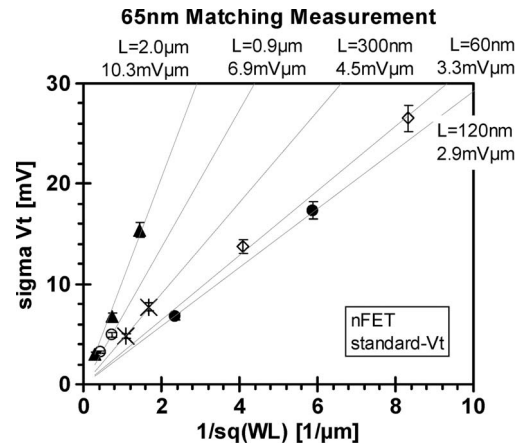


Fig. 1. Measured threshold voltage matching σ_{V_t} versus $1/\sqrt{WL}$. The matching parameter increases strongly ($2.9 \rightarrow 10.3 \text{ mV} \cdot \mu\text{m}$) with increasing gate length [(•) $0.12 \mu\text{m} \rightarrow$ ($\blacktriangle$) $2.0 \mu\text{m}$] as indicated by the labels of the regression lines. The error bars indicate a $\pm 5\%$ confidence interval for σ_{V_t} . Further symbols for gate lengths: ($\diamond$) $0.06 \mu\text{m}$, ($*$) $0.30 \mu\text{m}$, and ($\circ$) $0.90 \mu\text{m}$.

addressed to circuit designers since the matching can be worse by factors than predicted by (1) for long-channel transistors.

II. EXPERIMENTAL OBSERVATIONS

The threshold voltage V_t of planar bulk transistors is controlled by well implants and often additionally by halo implants. Transistors with V_t almost independent of gate length show a matching behavior according to (1). For transistors with dominating halo implantations, this matching behavior is superimposed by a gate length dependence which deteriorates the matching (Fig. 1). The 65-nm node measurements are based on 1000 transistor pairs per transistor geometry. Error bars indicate a $\pm 5\%$ uncertainty assuming a 95% probability. Similar observations were reported by NXP [5] and Chartered [6].

A measure for the halo impact on matching is defined by the $V_t(L)$ behavior. The short-channel effect of nonhalo FETs results in a V_t roll-off for short lengths; the halo implant produces an opposite behavior (Fig. 2). The V_t swing from long to short channel relative to the long-channel value gives a measure for the halo impact on matching. For relative V_t swings larger than 20%, a significant matching channel length dependence is expected.

III. DERIVATION OF THE MATCHING MODEL

Some transistor models divide the channel into parts [7], [8]. However, threshold voltage V_t and matching σ_{V_t} characterize

Manuscript received April 4, 2011; accepted April 14, 2011. Date of publication May 23, 2011; date of current version June 29, 2011. The review of this letter was arranged by Editor X. Zhou.

U. Schaper is with Infineon Technologies AG, 81726 Munich, Germany (e-mail: ulrich.schaper@infineon.com).

J. Einfeld is with Intel Mobile Communications, 85579 Neubiberg, Germany (e-mail: jan.christof.einfeld@intel.com).

Digital Object Identifier 10.1109/LED.2011.2150194

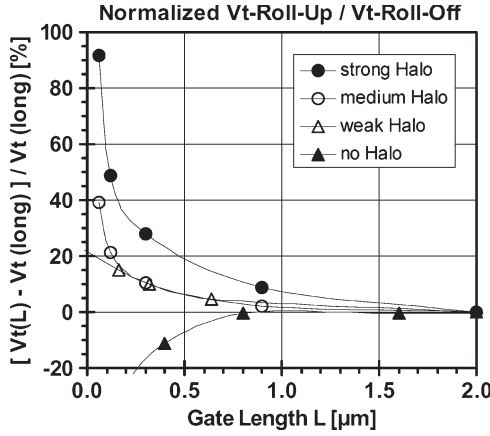


Fig. 2. V_t as a function of the gate length L normalized to the corresponding long-channel value. For relative V_t swings larger than 20%, a length-dependent matching is expected.

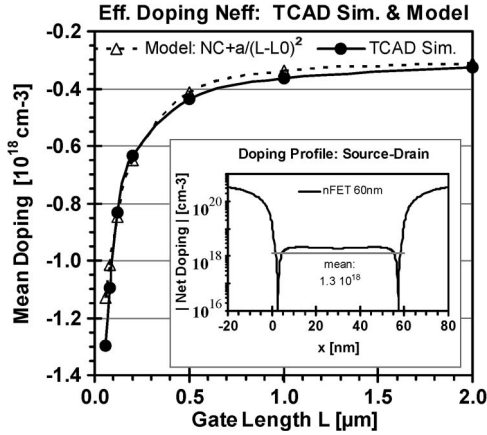


Fig. 3. Effective doping density N_{eff} for different gate lengths L for nFETs in 65-nm technology. A (Δ) simple analytical model describes the ($\bullet$) results of a process and device simulation (TCAD) very well in the range considered. The TCAD data are derived from mean values of net doping profiles. One example for an nFET with $L = 60$ nm is shown in the inset. The model parameter a abbreviates $(N_H - N_C)L_0^2$ (4).

the whole device; therefore, a compact model approach has been chosen. The physical V_t equation [9] is modified by an effective doping density $N_{\text{eff}}(L)$ that is dependent on gate length L

$$V_t = V_{\text{FB}} + 2\psi_B + \frac{t_{\text{ox}}}{\epsilon_{\text{ox}}} \sqrt{2q\epsilon_{\text{si}}2\psi_B N_{\text{eff}}(L)} \quad (2)$$

where V_{FB} is the flatband voltage, ψ_B is the bulk potential, t_{ox} is the electrical oxide thickness, ϵ_{ox} is the permittivity of oxide, q is the elementary charge, and ϵ_{si} is the permittivity of silicon.

The effective doping density N_{eff} is calculated with process and device simulations for different channel lengths L . These simulations result in 2-D transistor cross sections with contours of net doping density. The net doping profile (inset of Fig. 3) is determined from a cut along the channel from source to drain. These profiles are used to calculate the effective doping density as a mean value by integration over the channel length

$$N_{\text{eff}}(L) = \frac{1}{L} \int_0^L \text{NetDoping}(x) dx. \quad (3)$$

For different transistor types and different oxide thicknesses, $N_{\text{eff}}(L)$ follows a simple relation

$$N_{\text{eff}}(L) = N_C + \frac{(N_H - N_C) \cdot L_0^2}{(L - L_0)^2} \quad (4)$$

with a good accuracy (Fig. 3) in the range considered, where N_C denotes the long-channel concentration, N_H denotes the halo concentration, and L_0 is the halo length (≈ 10 nm). In the case of nonhalo transistors, an equivalent relation was derived for the short-channel effect using the voltage doping transformation [10]. Inserting (4) into (2) with $V_0 = V_{\text{FB}} + 2\psi_B$ and $V_1 = 2q\epsilon_{\text{si}}2\psi_B$ results in

$$V_t = V_0 + \frac{t_{\text{ox}}}{\epsilon_{\text{ox}}} \sqrt{V_1} \sqrt{N_C \left[1 - \frac{L_0^2}{(L - L_0)^2} \right] + N_H \frac{L_0^2}{(L - L_0)^2}}. \quad (5)$$

The concentrations N_H and N_C contribute to the variance $\sigma_{V_t}^2$

$$\sigma_{V_t}^2 = \left(\frac{t_{\text{ox}}}{\epsilon_{\text{ox}}} \right)^2 \frac{V_1}{4N_{\text{eff}}} \left\{ \left[1 - \frac{L_0^2}{(L - L_0)^2} \right]^2 \sigma_{N_C}^2 + \frac{L_0^4}{(L - L_0)^4} \sigma_{N_H}^2 \right\}. \quad (6)$$

Using the Poisson distributions for the dopant variances $\sigma_{N_C}^2$ and $\sigma_{N_H}^2$ as done in [4], a compact model for the matching variance $\sigma_{V_t}^2$ results

$$\sigma_{V_t}^2 = \frac{A^2}{W \cdot L} \cdot \frac{1}{V_t(L) - V_0} \cdot C(L) \quad (7)$$

with

$$A^2 = \left(\frac{t_{\text{ox}}}{\epsilon_{\text{ox}}} \right)^3 \frac{qV_1 N_C}{4} \quad (8)$$

$$C(L) = \left[1 - \frac{L_0^2}{(L - L_0)^2} \right]^2 \frac{1}{1 - 2L_0/L} + \frac{L_0^4}{(L - L_0)^4} \frac{N_H}{N_C} \frac{1}{2L_0/L}. \quad (9)$$

The compact matching model (7) is an extension of the Pelgrom model (1) which is recovered for constant threshold voltage ($V_t = \text{const.}$) and no halo ($L_0 = 0$ nm). There is still a matching decrease with increasing gate area; matching also decreases with oxide thickness. The additional length dependence for long channels is described by $V_t(L)$ in a very compact way, thereby extending published models [11], [12]. The explicit form of $N_{\text{eff}}(L)$ (3) is not needed. One additional parameter V_0 is needed to describe the spread in the matching with respect to the gate length; the parameter A describes the overall scaling as in the Pelgrom model. The correction function $C(L)$ has values in the range of 1.0–1.3 and contains the process parameters halo length L_0 and doping ratio N_H/N_C of the halo-to-channel implantations; $C(L)$ is effective only for minimum gate lengths.

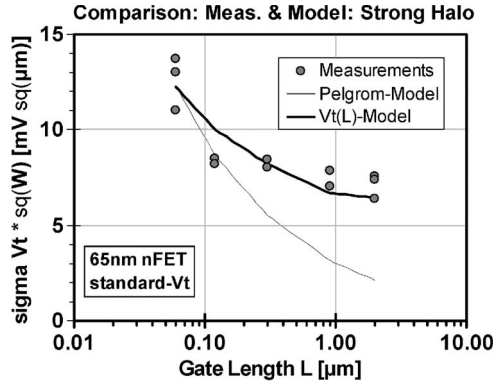


Fig. 4. Transistor matching σ_{V_t} normalized with $\sqrt{W}$ versus gate length L . For standard- V_t nFETs of 65-nm node having strong halo implants, (thin line) the Pelgrom model and (thick line) the compact $V_t(L)$ matching model are compared with measurements. The compact $V_t(L)$ model describes the matching of long channels very well.

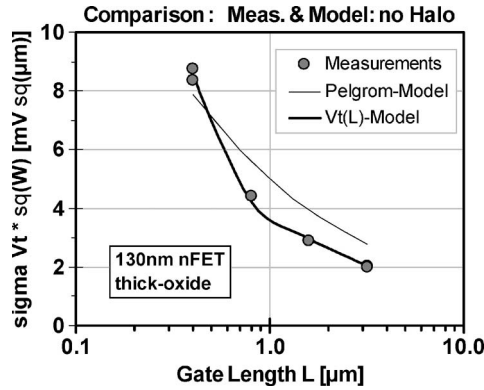


Fig. 5. Transistor matching σ_{V_t} normalized with $\sqrt{W}$ versus gate length L . For thick oxide nFETs of 130-nm node having no halo implants, (thin line) the Pelgrom model and (thick line) the compact $V_t(L)$ matching model are compared with measurements. The compact $V_t(L)$ model improves the matching description of long-channel FETs.

IV. RESULTS

The compact matching model (7) is applied to measured data of several transistor types of 65-, 90-, and 130-nm nodes. In the cases with medium to strong halo, a considerable improvement is achieved. For weak or no halo, the new model still shows an improved accuracy. Two examples are given (Figs. 4 and 5) for a thin oxide nFET in 65 nm with a strong halo implant (parameters: $A = 43 \text{ mV} \cdot \mu\text{m}$, $V_0 = 240 \text{ mV}$, $L_0 = 8 \text{ nm}$, and $N_H/N_C = 10$) and for a thick oxide nFET in 130 nm having no halo implant (parameters: $A = 42.7 \text{ mV} \cdot \mu\text{m}$, $V_0 = 433 \text{ mV}$, $L_0 = 0 \text{ nm}$, and $N_H/N_C = 0$). The matching σ_{V_t} scaled by $\sqrt{W}$ is shown versus the gate length. The Pelgrom model and the new compact model are compared with the measured data. A clear improvement is achieved, particularly for large gate lengths.

V. CONCLUSION

A compact matching model has been derived and successfully applied to measured data for several transistor types and different technology nodes. The new model is an extension of the Pelgrom model and utilizes the $V_t(L)$ behavior to describe the matching deterioration for long-channel halo devices. Only two model parameters are needed to cover the matching over the whole geometry range since the detailed length dependence is already contained in $V_t(L)$ and the correction function $C(L)$ which uses only fixed technology parameters. Showing a significantly increased accuracy, the compact matching model is particularly suitable for high-precision circuit designs where also long-channel devices are frequently used.

REFERENCES

- [1] A. Asenov, A. R. Brown, G. Roy, B. Cheng, C. Alexander, C. Riddet, U. Kovac, A. Martinez, and S. Roy, "Simulation of statistical variability in nano-CMOS transistors using drift-diffusion, Monte Carlo and non-equilibrium Green's function techniques," *J. Comput. Electron.*, vol. 8, no. 3/4, pp. 349–373, Oct. 2009.
- [2] O. Faynot, F. Andrieux, O. Weber, C. Fenoillet-Béranger, P. Perreux, J. Mazurier, T. Benoist, O. Rozeau, T. Poiroux, M. Vinet, L. Grenollet, J.-P. Noel, N. Posseme, S. Barnola, F. Martin, C. Lapeyre, M. Cassé, X. Garros, M.-A. Jaud, O. Thomas, G. Cibrario, L. Tosti, L. Brévard, C. Tabone, P. Gaud, S. Barraud, T. Ernst, and S. Deleonibus, "Planar fully depleted SOI technology: A powerful architecture for the 20 nm node and beyond," in *IEDM Tech. Dig.*, 2010, pp. 50–53.
- [3] M. J. M. Pelgrom, A. C. J. Duinmaijer, and A. P. G. Welbers, "Matching properties of MOS transistors," *IEEE J. Solid-State Circuits*, vol. 24, no. 5, pp. 1433–1439, Oct. 1989.
- [4] K. R. Lakshmikummar, R. A. Hadaway, and M. A. Copeland, "Characterization and modeling of mismatch in MOS transistors for precision analog design," *IEEE J. Solid-State Circuits*, vol. SSC-21, no. 6, pp. 1057–1066, Dec. 1986.
- [5] H. Tuinhout, N. Wils, M. Meijer, and P. Andricciola, "Methodology to evaluate the impact of segmentation on MOSFET matching," in *Proc. IEEE Int. Conf. Microelectron. Test Struct.*, 2010, pp. 176–181.
- [6] B. P. Wong, "Bridging the gap between dreams and nano-scale reality," in *Proc. DAC, Tutorial 3 'Real DFM Solutions, Tools, Methodologies, and Successes'*, Jul. 28, 2006, Part 3, pp. 1–23.
- [7] R. Rios, W.-K. Shih, A. Shah, S. Mudanai, P. Packan, T. Sandford, and K. Mistry, "A three-transistor threshold voltage model for halo processes," in *IEDM Tech. Dig.*, 2002, pp. 113–116.
- [8] C. M. Mezzomo, A. Bajolet, A. Cathignol, E. Josse, and G. Ghibaudo, "Modeling local electrical fluctuations in 45 nm heavily pocket-implanted bulk MOSFET," *Solid State Electron.*, vol. 54, no. 11, pp. 1359–1366, Nov. 2010.
- [9] Y. Taur and T. H. Ning, *Fundamentals of Modern VLSI Devices*. Cambridge, U.K.: Cambridge Univ. Press, 2001.
- [10] T. Skotnicki, G. Merckel, and T. Pedron, "The voltage-doping transformation: A new approach to the modeling of MOSFET short-channel effects," *IEEE Electron Device Lett.*, vol. 9, no. 3, pp. 109–112, Mar. 1988.
- [11] S. Bordez, A. Cathignol, and K. Rochereau, "A continuous model for MOSFET V_T matching considering additional length effects," in *Proc. IEEE Int. Conf. Microelectron. Test Struct.*, 2007, pp. 226–229.
- [12] K. Takeuchi, T. Fukai, T. Tsunomura, A. T. Putra, A. Nishida, S. Kamohara, and T. Hiramoto, "Understanding random threshold voltage fluctuation by comparing multiple fabs and technologies," in *IEDM Tech. Dig.*, 2010, pp. 50–53.